

ARM[®] Cortex™-M1 Embedded Processor Hardware Development Tutorial

for Fusion Mixed-Signal FPGAs



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Introduction

This document shows you how to create a Cortex[™]-M1 processor system that runs on one of the Actel Fusion embedded development kit boards. This design can be used as a starting point for developing your Cortex-M1 embedded system targeting Actel's Fusion FPGA devices.

Because this tutorial targets one of Actel's Fusion devices, you need to become familiar with Fusion features and architecture. The Fusion datasheet and user's guide are on the Actel website:

http://www.actel.com/documents/Fusion_DS.pdf

http://www.actel.com/documents/Fusion_UG.pdf

After completing this tutorial, you will know the hardware design flow for creating a Cortex-M1 embedded system using Libero[®] Integrated Design Environment (IDE) and SmartDesign tools. This includes the following design steps:

- Instantiating and configuring the Cortex-M1 processor, memory, and peripherals in SmartDesign
- Connecting peripherals and defining the address map in SmartDesign
- Automated generation of the DirectCore RTL
- Functional simulation using a bus functional model (BFM)
- Synthesis, place-and-route of hardware design, and generating FPGA programming image
- Programming an Actel FPGA with Cortex-M1 system ready for software design

For this tutorial, we will use the binary file from previously developed software. The binaries will be written into the memory on the target development kit, along with the programming bit files for the hardware designed in this tutorial. If you want to learn about the software development flow for the Cortex-M1 processor, you can study the ARM Cortex-M1 Embedded Processor Software Development Tutorial:

http://www.actel.com/documents/CortexM1_Proc_SW_Tutorial_UG.pdf.

Requirements for this Tutorial

Hardware

To complete this tutorial, you need one of the following boards with the corresponding hardware:

- Fusion Embedded Development Kit Board (M1AFS-EMBEDDED-KIT board)
 - Low-cost programming stick
 - 2 USB cables (USB to mini-USB)
 - PC with 2 USB ports
- Fusion Advanced Development Kit Board (M1AFS-ADV-DEV-KIT board)
 - Low-cost programming stick
 - 2 USB cables (USB to mini-USB)
 - 9 V power supply (provided with kit)
 - PC with 2 USB ports

Everything you need (except the PC) is provided with the development kit. For more information about the development boards, refer to Design Hardware page:

www.actel.com/products/hardware/default.aspx



Software

The instructions are based on the Actel Libero IDE v8.6 SPA software along with the corresponding Synplify[®] and ModelSim[®] OEM software installed on your PC. If you are using a different version, some steps and screen shots may be different.

Intellectual Property (IP)

This tutorial is based on the DirectCore IP listed below. If you do not have these DirectCore IP versions in your SmartDesign Catalog, you may observe different behavior from what is described in this tutorial.

- Cortex-M1 version 2.7.103
- CoreAHBLite version 2.0.140
- CoreAPB version 1.1.101
- CoreAHB2APB version 1.1.101
- CoreAhbNvm version 1.3.135
- CoreAhbSram version 1.3.103
- CoreMemCtrl version 2.0.105
- CoreUARTapb version 4.0.120
- CoreGPIO version 1.2.103
- CoreAl version 3.0.119

Licensing

You will need a license for these IP cores. If you do not have a license, go to the Customer Portal at https://www.actel.com/portal/, sign in and choose *Licenses & Registration* on the left navigation. Click the **Request Free License** button and choose the **Libero Gold** license. Follow the instructions in the email sent to you to set up the license on your machine.



1 – Design Overview

Cortex-M1 System Description

The design contains a Cortex-M1 processor system running on an Actel Fusion FPGA, which contains an analog block for monitoring analog signals. The system measures various voltages, currents, and temperatures on the target board, processes the sampled data, and sends the result over UART. There is a potentiometer on the board to change the analog voltage being sampled. In this tutorial you will communicate with the target using Hyper Terminal.

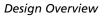
Cortex-M1 Hardware Design Description

The Cortex-M1 processor system uses CoreAI, which allows the processor to configure, control, and interact with the Analog Block inside the Actel Fusion FPGA. The UART in the system connects to an off-chip USB-to-UART chip, which allows you to communicate with the target system via a COM port on your machine (using HyperTerminal). Also included are 4 output bits to LEDs, and 2 input bits from push-buttons or DIP switches (depending on the target board).

The Fusion Advanced Development Kit and the Fusion Embedded Development Kit boards contain an Actel Fusion AFS1500 device that has 1 MByte of embedded flash memory (also referred to as nonvolatile memory, or NVM) and 30 KBytes of internal SRAM. The Fusion Embedded Development Kit board has 1 Mbyte of SRAM, comprised of two 4 Mbit × 16 bit chips. The Fusion Advanced Development Kit board has 2 Mbytes of SRAM, comprised of two 1 Mbit x 16 bit chips. This hardware design connects to all of these memories, not necessarily using the entire memory space of each device.

Actel's Fusion devices have an on-chip 100 MHz RC oscillator. You will feed this clock source to a PLL inside the Fusion device that modifies the clock frequency. The output of the PLL is the system clock.

This design enables the JTAG debug interface of the Cortex-M1 processor for software debugging. The debug interface will not be used in this hardware design tutorial. However, it is required for the ARM Cortex-M1 Embedded Processor Software Development Tutorial for Fusion Mixed-Signal FPGAs (www.actel.com/documents/CortexM1_Proc_SW_Tutorial_UG.pdf), which uses hardware created in this design tutorial.





A block diagram of the design is shown in Figure 1-1.

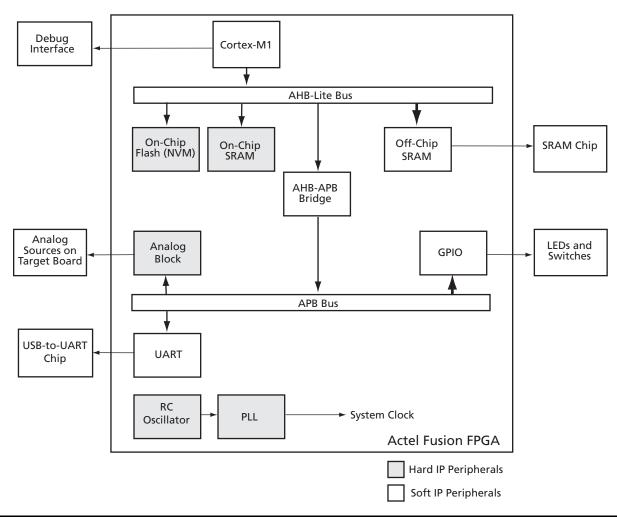


Figure 1-1 • Block Diagram



2 – Before You Get Started

Download Tutorial Files

Before starting the tutorial, you need to download the tutorial files from the website for the board you are targeting. Go to Actel's Design Hardware web page and click the link for the board you are targeting (http://www.actel.com/products/hardware/default.aspx). On the web page of the target board, click on the zip file under the ARM Cortex-M1 Embedded Processor Hardware Development Tutorial document.

The files are placed in a folder called CortexM1_Fusion_HW_Tutorial.

If you browse the contents of the zip file, you will see a subdirectory for every board this tutorial supports. The directory structure is similar for each board. As an example, Figure 2-1 shows a picture of the directory structure for the Fusion Embedded Development Kit board (M1AFS-EMBEDDED-KIT).

M1AFS_ADV_KIT		
File Edit View Favorites Tools Help		A
Folders		
🗆 🗀 M1AFS_ADV_KIT		
📄 Tutorial_Files		
📄 USB_Drivers		
📄 Verilog		
4 objects (Disk free space: 2.96 GB)	0 bytes	😡 My Computer 🛛 📈

Figure 2-1 • Tutorial Files

The Verilog and VHDL subdirectories contain the complete VHDL and Verilog projects for this tutorial design, for your reference. The *Tutorial_Files* subdirectory contains the source files you need to complete this tutorial. Table 2-1 gives a description of these files. The names of the files will be slightly different depending on the board you are targeting.

Table 2-1 • Description of Tutorial Files

File Name	Description
M1AFS_EMB_TUT	Pin constraints for the Fusion Embedded Development Kit board
TUTORIAL.HEX	Intel-Hex file which contains Cortex-M1 software code
M1AFS_EMB_TUT_ <verilog vhdl="">.PDC</verilog>	Constraint to put JTAG reset and clock net on global

The USB_Drivers subdirectory contains the driver for the USB-to-UART chip on the target board. This driver allows you to communicate with the target board over USB by treating the USB port as a COM port. Therefore, you can use HyperTerminal to connect to a UART in the design running on the board.



Install USB-to-UART Driver

At the end of the tutorial, you program the Fusion FPGA and communicate with the target board. To complete the tutorial, you need to make sure that the USB-to-UART drivers are installed on your machine and identify which COM port the USB port is associated with. Follow the steps below before starting the tutorial to make sure your machine is properly configured and connected to the target board.

Setting Up the USB-to-UART Driver

- 1. Make sure that a terminal emulation program such as HyperTerminal, which is included with Windows,[®] is installed on your PC.
- 2. Install the drivers for the USB to RS-232 Bridge by double-clicking on the **Preinstaller.exe** executable located in the USB_Drivers subfolder. Accept the default installation folder and press the **Install** button. Press the **Continue Anyway** button if prompted.
- 3. Connect USB and power cables according to Table 2-2.

Table 2-2 •Power and USB Connections

Board	Power and USB Connections
M1AFS-EMBEDDED-KIT	Make sure you have J40 set to use USB power (not V5IN). Connect a USB cable to J2, which provides power and the USB-to-UART communication. Make sure JP10 is set to use the 1.5 V external regulator (connect pins 2 and 3).
M1AFS-ADV-DEV-KIT	Connect the 9 V power supply provided with the kit to J3 on the board. Connect a USB cable to J2, this provides the USB-to-UART communication and make sure SW7 is in the ON position to supply power to the board.

If Windows prompts you to connect to Windows Update, select No, not at this time and press Next.

- 4. Select **Install the software automatically** (recommended) and press **Next**. Once installation has completed, press **Finish**. Repeat the driver installation steps a second time (if prompted). Press the **Continue Anyway** button if prompted.
- Open the Windows Device Manager by selecting Start > Control Panel > System > Hardware > Device Manager. Expand the Ports (COM and LPT) section and take note of the COM port assignment for the SFE USB to RS232 Controller (in Figure 2-2 it is assigned to COM8).



If you do not see SFE USB to RS232 Controller in the Device Manager (Figure 2-2), you may need to reboot your machine.

Bevice Manager	X
<u>File Action View Help</u>	
\leftarrow \rightarrow \square \blacksquare \blacksquare \blacksquare \blacksquare	
Batteries Computer Disk drives Display adapters Mice and other pointing devices Modems Modems Monitors Monitors POrtCIA adapters POrts (COM & LPT) Ports (COM & LPT) Communications Port (COM1) ECP Printer Port (LPT1) SFE USB to R5232 Controller (COM8) Toshiba BT Port (COM10) Toshiba BT Port (COM11) Toshiba BT Port (COM12) Toshiba BT Port (COM13)	
Toshiba BT Port (COM14)	~

Figure 2-2 • Windows Device Manager

1. Connect the FlashPro3 programming interface according to Table 2-3.

Table 2-3 • Programming Interface Connections

Board	FlashPro3 Programming Interface Connection
M1AFS-EMBEDDED-KIT	Connect the FlashPro3 Low-Cost Programming Stick (LCPS) to J1.
M1AFS-ADV-DEV-KIT	Connect a USB cable between the LCPS and the host machine.

2. If you are prompted to install drivers for the FlashPro3 hardware, refer to the FlashPro User's Guide at http://www.actel.com/documents/flashpro_ug.pdf.



3 – Tutorial – Create Design

Step 1 – Create an Actel Libero IDE Project

Open the Libero IDE tool and complete the following steps to create a Libero IDE project.

- 1. Go to Project > New Project. The New Project Wizard window opens.
- Type M1AFS_EMB_TUT (for M1AFS-EMBEDDED-KIT) or M1AFS_EMB_TUT (for M1AFS-ADV-DEV-KIT) in the Project name field.
- 3. Click the Browse button and choose a location on your machine for the project.
- 4. Select your preferred HDL language. Your window should look similar to Figure 3-1.

New Project Wizard			×
	e to the New Pr creates a new Liber		
Start Select Device	Project <u>n</u> ame:	M1AFS_EMB_M1_TUT	
Select Tools	Project Jocation:	D:\Actelprj\M1AFS_EMB_M1_	Browse
Finish	Preferred HDL ty	<u>pe:</u> ⊙ V <u>e</u> rilog	
		© V <u>H</u> DL	Help
	< Back	Next >	Cancel

Figure 3-1 • New Project Wizard

- 5. Click Next. The Family, Die and Package options appear (Figure 3-2 on page 3-14).
- 6. Select Fusion for the Family.
- 7. Select M1AFS1500 for the Die.



8. Select 484 FBGA for the Package

	Die and Package amily, die and package of your new project.	×
Start Select Device Select Tools Add Files Finish	Family: Help Fusion ▼ Die: Package: M1AFS600 ▲ U1AFS600 ▲ P1AFS600 ▲ M1AFS1500 ● P1AFS1500 ●	
	< Back Next > Finish Canc	el

Figure 3-2 • Select Family, Die, and Package

- 9. Click Next two times. The Add files to your project options appear.
- 10. Click the **Add Files** button.
- 11. Select Physical Design Constraint Files (*.pdc) for the Files of type box.
- 12. Browse to the following directory: CortexM1_Fusion_Tutorial

board><Tutorial_Files
- 13. Select M1AFS_EMB_TUT.PDC and M1AFS_EMB_TUT_<VERILOG/VHDL>.PDC or M1AFS_ADV_TUT.PDC and M1AFS_ADV_TUT_<VERILOG/VHDL>.PDC, depending on the board you are targeting and the project language used (Verilog or VHDL).
- Note: These PDC files contain pin assignments for the FPGA design and are specific to this board. This design does not need a timing constraints file (SDC) because the internal clock source from the RC oscillator is constrained automatically by SmartTime.
 - 14. Click Add. You should see the file you selected under the Constraint Files section.
 - 15. Click Finish to create the Libero IDE project.

Step 2 – Create a SmartDesign Component within Actel Libero IDE

Follow the steps below to create a SmartDesign component for your hardware design.

1. Click the SmartDesign icon in the Design Entry Tools area (in the Project Flow tab, as shown in Figure 3-3.

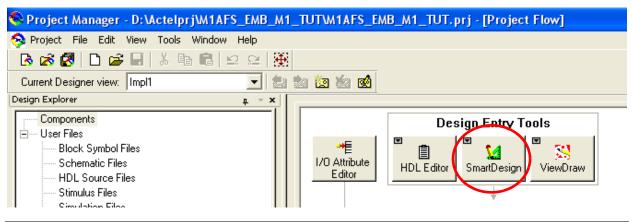


Figure 3-3 • SmartDesign Icon

2. Type M1AFS_TUT_TOP in the Name field, as shown in Figure 3-3.

Select a Type:	SmartDesign Component
Schematic SmartDesign Component CoreConsole Component P Component VHDL Source File Verilog Source File WaveFormer Stimulus File HDL Stimulus File SDC File (sdc) Physical Design Constraint File (pdc) DO File VHDL Template Verilog Template	Name: M1AFS_TUT_TOP

Figure 3-4 • Select SmartDesign Component



Tutorial – Create Design

 Click OK. A blank canvas opens in SmartDesign, which looks like Figure 3-5. Notice the new M1AFS_TUT_TOP tab (next to the Project Flow tab) which contains a Canvas tab. This is your new SmartDesign canvas window.

	or_Platform\CortexM1_Fusion_FPGA_Design_Tutorial_Files_v1.0W1AFS_EMBEDDED_KIT\Completed_Design\Verilog\W1AFS_EMB_M1_TUTW	
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ow: Components		Filter: • Add Core Optic
work.		△ Function, Name: Version ✓ Actel Macros
		Actel Macros Basic Blocks
		Bus Interfaces
		Clock & Management
		Fusion Peripherals
		Memory & Controllers
		Peripherals
		Processors
		<u> </u>
		Gares Templates Dus Definitions
		Information Window
		Project Manager New Features
	-	I/O Attribute Editor Tool Profiles Enhancements
	8	IP-Cores Undates CoreConsole Project Conversion SmartDesign Save As
	No. Canvar	SmartDesign Save As
	Project Row MTAFS_TU	Properties
	X M Ports Print M- Options	riopenaes
	The MiAF5_EMD_Mi_TUT project was created.	
	8	
Hierarchy 💽 Files		

Figure 3-5 • SmartDesign Canvas Window

In the following steps you use SmartDesign to create a Cortex-M1 system, as shown Figure 3-7 on page 3-18. When the instructions tell you to instantiate a component, instantiate it in the SmartDesign Canvas.

As you are instantiating the components, Actel recommends you use the same version of DirectCore IP. Otherwise, you may receive different results.



Obtaining a Different Version of DirectCore IP

1. Click the **Options** button in the Catalog. You will see the Catalog Display Options window (Figure 3-6).

Catalog Display Options	
Display	Filters
Organize the cores displayed in your Catalog.	Select which cores to display in the Catalog.
Group cores by function	Name: *
C List cores alphabetically	Function: *
Sort order: Ascending	Market Segment: All
Show filters fields in catalog	Display only the latest version of a core
	Show all local and remote cores Show local cores only
Default Change Vault Location	○ Show remote cores that are not in my vault
Help	OK Cancel

Figure 3-6 • Catalog Display Options

- 2. Clear the check box for **Display only the latest version of a core**. Make sure you have selected both **Show core version** and **Show all local and remote cores**.
- 3. Click **OK**. If you still do not see the version you need in the Catalog, then proceed to the next step.
- 4. Click the Add Core button and choose From Web Repository. The Add Cores to Vault window appears.
- 5. Select the core(s) that you need and click Add.
- 6. Click **Done** once the new cores have been downloaded.

Instantiate Cortex-M1 Processor

The Cortex-M1 processor is a 32-bit soft ARM® processor designed to be implemented in an FPGA. Follow the steps below to instantiate the Cortex-M1 processor.

- 1. Go to the Catalog and expand the Processors category.
- 2. Instantiate by clicking and dragging Cortex-M1 version 2.7.103 onto the SmartDesign canvas.
- 3. Select FlashPro3 as the Debug Interface. This allows software debugging over JTAG using Actel's SoftConsole[®] development tool.
- Note: If you are planning to use third-party tools (Keil MDK-ARM, IAR Embedded Workbench, ARM RealView, etc.), select RealView JTAG as the Debug Interface. However, keep in mind that this



Tutorial – Create Design

document assumes you are using Actel's SoftConsole development tool. Also, the succeeding Cortex-M1 Software Design Tutorial requires the FlashPro3 debug interface.

- Debugging
Debug Interface: FlashPro3
Target FPGA
Die: M1AF51500
Speed grade: -2
Tightly Coupled Memory
Instruction TCM: 0 Kbytes
Data TCM: 0 Kbytes 👻
Other
Number of Interrupts: 1
Multiplier: Small
Enable OS Extensions:
License: Obfuscated

Figure 3-7 • Configuring Cortex-M1 Processor

4. Click OK. You should see an instance of the Cortex-M1 processor on the SmartDesign canvas.

Instantiate CoreAHBLite Bus

The AHB-Lite bus is a multimaster 32-bit bus (data and address) which allows you to connect up to 2 masters and 16 slave peripherals, where each peripheral consumes one slot (numbered 0 through 15). Each slot is 256 MBytes in the processor's memory space (for a total of 4 GBytes).

- 1. Go to the Catalog and expand the Bus Interfaces category.
- 2. Instantiate CoreAHBLite version 2.0.140 with the default settings (all slots enabled).

Note that the configuration window allows you to disable slots that you are not using. For this tutorial design, leave all slots enabled (the default).

Instantiate CoreAhbNvm

CoreAhbNvm provides the processor with an AHB interface to access the internal NVM (nonvolatile memory, also known as embedded flash memory) of the Fusion device. The M1AFS1500 device has 1 MByte of internal NVM composed of 4 embedded flash memory blocks, each 256 Kbytes in size. However, for this design you will use only 1 embedded flash memory block, 256 Kbytes. Follow the steps below to instantiate the CoreAhbNvm.



- 1. Go to the Catalog and expand the Memory & Controllers category.
- 2. Instantiate and configure **CoreAhbNvm version 1.3.135** with a size of 256 Kbytes. The CoreAhbNvm settings are shown in Figure 3-8.

Configuring CoreAhbN	vm_0 (CoreAhbl	lvm - 1.3.135)	
onfiguration			
-Amount of internal FLA	SH required:		
⊙ 256KBytes	◯ 512KBytes	🔘 1MBytes	
License:	Obfusca	ted	
		ОК	Cancel

Figure 3-8 • Configuring CoreAhbNvm

Instantiate CoreMemCtrl

CoreMemCtrl creates an interface to off-chip SRAM and/or flash with shared data and address busses. The AHB slot is divided in half with the flash at the bottom half and SRAM at the upper half of the slot. By setting the Remap input to '1', you can swap the flash and SRAM locations. For this design, you will use the SRAM interface only. The system clock in this design is 20 MHz, which has a period of 50 ns. The asynchronous SRAM has a 10 ns access time. Therefore, you can set the wait states to their minimum values: 0 for read wait states and 1 for write wait states.

- 1. Go to the Catalog and expand the Memory & Controllers category.
- 2. Instantiate **CoreMemCtrl version 2.0.105** to interface to the off-chip asynchronous SRAM on the development board.
- 3. Take the following selections in the CoreMemCtrl configuration window:
 - SRAM mode: Asynchronous
 - Number of wait states for SRAM read: 0
 - Number of wait states for SRAM write: 1
 - Read and write enables shared for Flash and SRAM: No

The flash and SRAM addressing options determine which bit of the AHB-Lite bus is connected to bit 0 of the off-chip memory. The default value of "0, 0, HADDR[27:2]" means the off-chip memory address is word addressed (32-bit word). The other settings refer to half-word and byte addressing. You can leave the other options at their default setting since this design does not use this flash interface.



Tutorial – Create Design

guration ——			
SRAM mode			
C) Synchronous	 Asynchronous 	
-Configuratio	on of SRAM device - s	ynchronous SRAM only	
	O Flow-through	Pipeline	
Flash data t	ous width		
	🔘 16 bit	 32 bit 	
-Flash wait s	tates		
	Number of wait s	tates for Flash read: 📘 💌	
	Number of wait s	tates for Flash write: 👖 💙	
-SRAM wait :	states - asynchronou	s SRAM only	
	Number of wait s	tates for SRAM read: 0 💌	
	Number of wait s	tates for SRAM write: 1 💌	
-Read and w	rite enables shared f	or Flash and SRAM?	
	💿 No	O Yes	
Flash addre	ssing		
For Fla	sh access, MEMADDR	[27:0] driven by: 0, 0, HADDR[27:2]	*
SRAM addre	essing		
For SR/	AM access, MEMADDF	2[27:0] driven by: 0, 0, HADDR[27:2]	~
Testbench:		User	~
License:			
	 Obfuscated 	O RTL	

The corresponding CoreMemCtrl settings are shown in Figure 3-9.

Figure 3-9 • Configuring CoreMemCtrl

Instantiate CoreAhbSram

CoreAhbSram provides the processor with an AHB interface to access the internal SRAM of the Fusion device. The Fusion M1AFS1500 device has 30 Kbytes of internal SRAM consisting of 60 RAM blocks each 0.5 Kbyte in size. The Cortex-M1 uses 2 Kbytes and the CoreUARTApb (which you instantiate later) uses 1 Kbyte in FIFO mode. Therefore, CoreAHBSram must use no more than 27 Kbytes. You will configure it for 14 Kbytes. Follow the steps below to instantiate the CoreAhbSram.

- 1. Go to the Catalog and expand the Memory & Controllers category.
- 2. Instantiate and configure **CoreAhbSram version 1.3.103** with a size of 14 Kbytes. The CoreAhbSram settings window is shown in Figure 3-10.

Amount of interna	al SRAM re	quired: 14K	Bytes 💌	
License:				
 Obfuse 	cated	🔘 RTL		

Figure 3-10 • Configuring CoreAhbSram

Instantiate CoreAHB2APB

The CoreAHB2APB is a bridge from the AHB bus to APB bus. It has an AHB slave which consumes one AHB slot and an APB master which can master an APB bus. Read and write transfers on the AHB bus are converted to APB transfers to the APB bus. Follow the steps below to instantiate the CoreAHB2APB.

- 1. Go to the Catalog and expand the Bus Interfaces category.
- 2. Instantiate the CoreAHB2APB version 1.1.101 to bridge to the APB bus.

Instantiate CoreAPB

The CoreAPB bus is a 32-bit bus (data and address) which allows you to connect up to 16 slave peripherals where each peripheral consumes one slot (numbered 0 through 15). Each slot is 16 MBytes in the processor's memory space for a total of 256 MBytes. Due to the performance, typically slower, low priority peripherals are placed in the APB bus. Follow the steps below to instantiate the CoreAPB.

- 1. Go to the Catalog and expand the Bus Interfaces category.
- 2. Instantiate the CoreAPB version 1.1.101 bus with the default settings (all slots enabled).

Note that you can disable slots that you are not using. For this tutorial, leave them all enabled.



Instantiate CoreAl

CoreAI allows the Cortex-M1 processor to access and control the Analog Block in the Fusion device. You will configure this instance of CoreAI to interface with the analog features on the target development board. The frequency of the ACM clock in the Analog Block must be 10 MHz or less. The PCLK (clock of the APB bus) is divided down to create the ACM clock. The appropriate divider value is calculated based on the PCLK frequency parameter. For this design, the PCLK frequency is 20 MHz.

- 1. Go to the Catalog and expand the Peripherals category.
- 2. Instantiate **CoreAl version 3.0.119** to give the Cortex-M1 processor access to the Analog Block in the Fusion device.
- 3. Configure CoreAI according to the list of settings below and leave the other settings at their default values.
- APB data bus width (in bits): 32
- PCLK frequency (up to nearest MHz): 20
- Interrupt output: Disabled (tied low)
- Analog Quad 0
 - AV0 input: Voltage Monitor: 0 V to 4 V
 - AC0 input: Current Monitor
- Analog Quad 1
 - AV1 input: Voltage Monitor: 0 V to 2 V
 - AC1 input: Current Monitor
- Analog Quad 2
 - AT2 input: Temperature Monitor
- Analog Quad 4
 - AC4 input: Voltage Monitor: 0 V to 4 V

Figure 3-11 through Figure 3-14 on page 3-25 show the instance of CoreAI with the corresponding parameters set.

🕵 Cor	nfiguring COREAI_0 (COREAI - 3.0.119)		
Co	nfiguration		A
	Fusion Specific		
	Fusion Device:	arger than AF5250	
	Shift RESULT[11:0] right in ADC_STAT reg by: 0) bits (no shift)	•
	AB macro enable/disable logic:	Add AB enable/disable logic, ADCRESET starts inactive	✓
	Processor Interface		
	APB data bus width (in bits):	32	
	PCLK frequency (up to nearest MHz):	20	
	Interrupt output:	Disabled (tied low)	
	Interrupt status register logic:	All interrupt status register bits used	·
			OK Cancel

Figure 3-11 • Configuring CoreAI (part 1)



	COREAI - 3.0.119)					
Analog Quad 0						
AV0 input:	Voltage Monitor: OV to 4V	*	AC0 input:	Current Monitor	*	
AT0 input:	Disabled	~	AG0 output:	Disabled	~	
Analog Quad 1						
AV1 input:	Voltage Monitor: 0V to 2V	*	AC1 input:	Current Monitor	~	
AT1 input:	Disabled	*	AG1 output:	Disabled	~	
Analog Quad 2						
AV2 input:	Disabled	*	AC2 input:	Disabled	~	
AT2 input:	Temperature Monitor	~	AG2 output:	Disabled	~	
Analog Quad 3						
AV3 input:	Disabled	*	AC3 input:	Disabled	~	
AT3 input:	Disabled	*	AG3 output:	Disabled	~	
Analog Quad 4						
AV4 input:	Disabled	*	AC4 input:	Voltage Monitor: OV to 4V	~	
AT4 input:	Disabled	*	AG4 output:	Disabled	~	
Analog Quad 5						
AV5 input:	Disabled	~	AC5 input:	Disabled	~	
AT5 input:	Disabled	*	AG5 output:	Disabled	~	
Analog Quad 6						
AV6 input:	Disabled	~	AC6 input:	Disabled	~	
AT6 input:		~	AG6 output:	Disabled	~	
-Analog Quad 7	L					
AV7 input:	Disabled	*	AC7 input:	Disabled	~	
AT7 input:		~	AG7 output:		~	
Analog Quad 8	L					
Avaiog Quad o	Disabled	~	AC8 input:	Disabled	~	
AT8 input:		~	AG8 output:		~	
Analog Quad 9			. nac catpaci			
Arialog Quau 9 AV9 input:	Disabled	~	AC9 input:	Disabled	~	
AT9 input:	Disabled	*	AG9 output:	Disabled	×	

Figure 3-12 • Configuring CoreAI (part 2)



-Software/Hardwa	re-Driven Control of Various AB (Analog Bloc	:k) Inputs		
VAREFSEL:	Statically fixed Internal VAREF	ADCRESET:	Software-Driven via internal register	~
PWRDWN:	Software-Driven via internal register 🛛 💌	ADCSTART:	Software-Driven via internal register	~
CHNUMBER:	Software-Driven via internal register 💌	MODE:	Software-Driven via internal register	~
TVC:	Software-Driven via internal register 💌	STC:	Software-Driven via internal register	~
Software/Hardwa	re-Driven Control of CMSTB* AB (Analog Blo	ck) Inputs		
CMSTB0:	Software-Driven via internal register 💉	CMST	31: Software-Driven via internal register 💉	•
CMSTB2:	Software-Driven via internal register 💉	CMST	33: Software-Driven via internal register	2
CMSTB4:	Software-Driven via internal register 💽	CMST	85: Software-Driven via internal register	2
CMSTB6:	Software-Driven via internal register 💽	CMST	87: Software-Driven via internal register	2
CMSTB8:	Software-Driven via internal register 💉	CMST	89: Software-Driven via internal register	2
Software/Hardwa	re-Driven Control of TMSTB* AB (Analog Blo	ck) Inputs		
TMSTB0:	Software-Driven via internal register 💉	TMST	B1: Software-Driven via internal register	-
TMSTB2:	Software-Driven via internal register 💌	TMST	B3: Software-Driven via internal register	-
TMSTB4:	Software-Driven via internal register 💉	TMST	B5: Software-Driven via internal register	-
TMSTB6:	Software-Driven via internal register 💽	TMST	B7: Software-Driven via internal register	-
TMSTB8:	Software-Driven via internal register 💽	TMST	B9: Software-Driven via internal register	-
TMSTBINT:	Software-Driven via internal register 🛛 👻			

Figure 3-13 • Configuring CoreAl (part 3)

Note that many of the parameters are software driven, which means that the Cortex-M1 processor can change these parameters by writing to registers.



Step 2 – Create a SmartDesign Component within Actel Libero IDE

-Real Time Cloc	k		
	Use Real Time Clock:	No	
	RTC_COUNTER4 (byte 4) initial value (0 to 255):	0]
	RTC_COUNTER3 (byte 3) initial value (0 to 255):	0]
	RTC_COUNTER2 (byte 2) initial value (0 to 255):	0]
	RTC_COUNTER1 (byte 1) initial value (0 to 255):	0]
	RTC_COUNTER0 (byte 0) initial value (0 to 255):	0]
	RTC_MATCHREG4 (byte 4) initial value (0 to 255):	0]
	RTC_MATCHREG3 (byte 3) initial value (0 to 255):	0]
	RTC_MATCHREG2 (byte 2) initial value (0 to 255):	0]
	RTC_MATCHREG1 (byte 1) initial value (0 to 255):	0]
	RTC_MATCHREG0 (byte 0) initial value (0 to 255):	0]
	RTC_CTRL_STAT initial value (0 to 255):	0]
Testbench:	N	one	
License:			
	Obfuscated	⊙ RTL	

Figure 3-14 • Configuring CoreAl (part 4)





Instantiate CoreUARTapb

CoreUARTapb is a configurable UART peripheral with an APB slave interface. Follow the steps below to instantiate the CoreUARTapb.

- 1. Go to the Catalog and expand the Peripherals category.
- 2. Instantiate and configure CoreUARTapb version 4.0.120 with the following selections:
 - TX FIFO: Enable TX FIFO
 - RX FIFO: Enable RX FIFO
 - Configuration: Programmable

The CoreUARTapb configuration is shown in Figure 3-15.

🕵 Configur	ing CoreUARTapb_0 (C	oreUARTapb - 4	.0.120)	
Configuration				
	Core Configuration			
	TX FIFO:	Enable TX FIFO	~	
	RX FIFO:	Enable RX FIFO	~	
	Configuration:	Programmable	*	
	Baud Value:	1		
	Character Size:	7 bits	~	
	Parity:	Parity Disabled	~	
	RX Legacy Mode:	Disabled	*	
	FIFO Implementation:	In RAM	~	
	Testbench:	User	~	
	-License:			1
	O Obfuscated	💿 RTL		
			ок	Cancel

Figure 3-15 • Configuring CoreUARTApb

The Baud value, Character Size and Parity parameters are greyed out since Configuration is set to Programmable. They can be modified by the processor when the UART is initialized. EQ 3-1 is used

to calculate the Baud Value parameter based on the desired baud rate (57600) and system clock frequency (20 MHz) in Hz:

Baud Value =
$$\frac{\text{clock}}{(16 \times \text{baud rate})} - 1 = \frac{20 \times 10^6}{(16 \times 57600)} - 1 = 21$$
 (rounded to the nearest integer)

EQ 3-1

Instantiate CoreGPIO

CoreGPIO allows you to access up to 32 general purpose inputs and 32 general purpose outputs. Follow the steps below to instantiate CoreGPIO.

- 1. Go to the Catalog and expand the Peripherals category.
- 2. Instantiate CoreGPIO version 1.2.103 with the default settings (32 inputs and 32 outputs).

Instantiate RC Oscillator

Actel Fusion devices have a 100 MHz on-chip RC oscillator which does not require any extra components. You will use this as an input to the PLL inside the FPGA. Follow the steps below to instantiate the RC Oscillator.

- 1. Go to the Catalog and expand the Fusion Peripherals category.
- 2. Instantiate Oscillator RC with Clock conditioning circuit selected.
- 3. Name it myRCOSC.

Instantiate PLL

The PLL inside of the FPGA can be used to generate new clock signals from a source clock. For this design, you will configure the PLL to use the RC Oscillator (from the previous step) as the input clock and generate a 20 MHz output clock (as the system clock). Follow the steps below to instantiate the PLL.

- 1. Go to the Catalog and expand the Clock & Management category.
- 2. Instantiate PLL Static with the following settings:
 - Clock input: RC Oscillator (on the left below the MHz text box)
 - GLA Output: 20 MHz (no delay)



Tutorial – Create Design

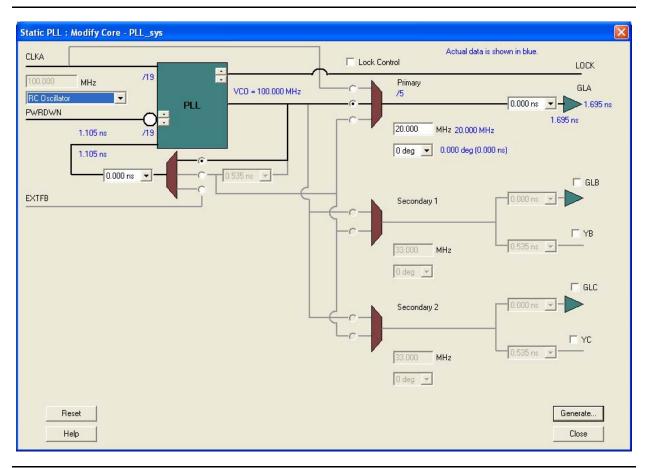




Figure 3-16 • Configuring the PLL

3. Name the PLL PLL_sys.

Instantiate AND2 Gate

Actel recommends that you hold the system in reset until the PLL has locked. You will use this AND2 gate to accomplish this. Later you will make the connections to other components. Follow the steps below to instantiate the AND2 gate.

- 1. Go to the Catalog and expand the Actel Macros category.
- 2. Instantiate AND2.

Connect Signals Automatically in SmartDesign

SmartDesign has the ability to automatically connect together standard interfaces for components with the *Auto Connect* feature. Many of the interfaces to standard components are well-defined and permit automatic connection. These include clock and reset signals, and Advanced Microcontroller Bus Architecture (AMBA) master/slave connections. Follow the steps to have SmartDesign automatically connect signals and to configure the memory maps.

- 1. Perform AutoConnect (right-click on canvas and choose **Auto Connect**). The Modify Memory Map window will open (Figure 3-17).
- 2. Click on **CoreAHBLite_0**. Configure the memory map for the CoreAHBLite bus as shown in Figure 3-17 by following the steps below for each peripheral that you need to move.
 - Click on the name of the peripheral in the Peripheral column.
 - Select the blank to remove this peripheral from this address.
 - Click on the Peripheral column next to the desired address of this peripheral.
 - Select the name of the peripheral from the list.

If you swap two peripherals, you must blank both address locations and then select each peripheral at the corresponding addresses. Note that you will have to remove the CoreMemCtrl_0:AHBslave_flash peripheral from the memory map, since it is not being used. Both SRAM and flash peripherals are added in automatically when using CoreMemCtrl.

Modify Memory Map		
Select Bus to View or Assign Peripheral(s):	Assign pe	ripherals to addresses on bus:
CoreAHBLite_0	Address	Peripheral
CoreAPB_0	0x00000000	CoreAhbNvm_0:AHBslave
	0x10000000	CoreMemCtrl_0:AHBslave_sram
	0x20000000	CoreAhbSram_0:AHBslave
	0x30000000	
	0x40000000	
	0x50000000	
	0x60000000	
	0x70000000	
	0x80000000	
	0x90000000	
	0xA0000000	
	0xB0000000	
	0xC0000000	CoreAHB2APB_0:AHBslave
	0xD0000000	
	0xE0000000	
	0xF0000000	
Help	·	OK Cancel

Figure 3-17 • Modify Memory Map for CoreAHBLite_0

3. Click on CoreAPB_0. Configure the memory map for the CoreAPB bus as shown in Figure 3-18 on page 3-30 using the same steps as above.



4. Click OK.

elect Bus to View or ssign Peripheral(s):	Assign p	eripherals to addresses on bus:
CoreAHBLite_0	Address	Peripheral
CoreAPB_0	0xc0000000	
	0xc1000000	
	0xc2000000	CoreGPIO_0:APBslave
	0xc3000000	CoreUARTapb_0:APBslave
	0xc4000000	
	0xc5000000	
	0xc6000000	COREAI_0:APBslave
	0xc7000000	_
	0xc8000000	
	0xc9000000	
	0xca000000	
	0xcb000000	
	0xcc000000	
	0xcd000000	
	0xce000000	
	0xcf000000	

Figure 3-18 • Configure Memory Map for CoreAPB_0

Take careful note to configure Memory Map dialog box as shown in Figure 3-17 on page 3-29 and Figure 3-18 as this directly defines the subsystem memory map and has a direct impact on the Cortex-M1 software code.

You may want to use the Auto Arrange Instances features in SmartDesign by right-clicking and choosing **Auto Arrange Instances**. This will place the peripherals in an orderly manner on the canvas.

Connect Signals Manually in SmartDesign

Some signals must be manually connected. There are two ways to manually connect signals in Smart Design. You can use the Canvas in a graphical manner or use the Grid in a spreadsheet manner. For this tutorial, use the Grid to connect the signals in Table 3-1 following the steps below.

- 1. Open the Grid by going to SmartDesign > Show Grid View.
- 2. Click the Lock signal cell from the PLL_sys_0 instance on the left column.
- 3. Scroll to the right to find the AND2_0 instance (on the top).
- 4. Click the cell which is the intersection of these two.
- 5. Select the B signal from the list box.
- 6. Follow steps 2-5 for the rest of the signals in Table 3-1.

Table 3-1 • N	anual Connections
---------------	-------------------

FROM				
Instance	Signal			
PLL_sys_0	LOCK			
(top level port)	NSYSRESET			
AND2_0	Y			

	то							
→	Instance	Signal						
→	AND2_0	В						
→	AND2_0	А						
→	CortexM1Top_0	NSYSRESET						

When making the last connection in the table, you will receive the message window shown in Figure 3-19.





- 7. Click **Yes.** You receive this message because you are changing the driver for NSYSRESET of the Cortex-M1 processor.
- 8. Some signals need to be connected to GND or V_{CC.} Follow the steps below to connect signals according to Table 3-2 on page 3-32 using the Smart Design Grid.
- 9. Right- click the dataln[31:0] signal from the CoreGPIO_0 instance and choose Add Slice.
- 10. Type 31 and 2 (for [31:2]), as shown in Figure 3-20.

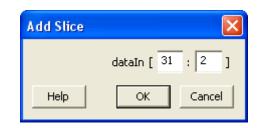


Figure 3-20 • Add Slice

- 11. Click OK.
- 12. Right-click on the [31:2] slice you just created and choose **Tie Low** because these bits are not being used in the design.
- 13. Left-click the cell in the Attribute column next to the EDBGRQ signal in the CortexM1Top_0 instance.
- 14. Choose Tie Low.
- 15. Follow steps 12-13 for the rest of the signals in Table 3-3, except remember to choose **Tie High** for the POWERDOWN signal of the PLL_sys_0 instance (as indicated in Table 3-2 on page 3-32).



Instance	Signal	Connection
CoreGPIO_0	dataln[31:2]	GND
CortexM1Top_0	EDBGRQ	GND
	NMI	GND
	lrq[031]	GND
	RV_TCK	GND
	RV_TDI	GND
	RV_TMS	GND
	WDOGRES	GND
PLL_sys_0	POWERDOWN	VCC
	OADIVRST	GND
CoreAHBLite_0	REMAP_M0	GND

Table 3-2 • VCC and GND Connections

Switch to the Smart Design Canvas, follow the steps below to change the clock source from the auto-generated SYSCLK top-level port to the output of the PLL.

- 1. Right-click the SYSCLK top level port and choose **Disconnect**.
- 2. Highlight the HCLK input of the Cortex-M1.
- 3. CTRL + Click to highlight the GLA output of the PLL.
- 4. Right-click on GLA and choose Connect.
- 5. Delete the SYSCLK port, since you do not need it in this design.

Now, the GLA output of the PLL should be the clock driver for the clock port of all peripherals. Your Canvas should look like Figure 3-21.

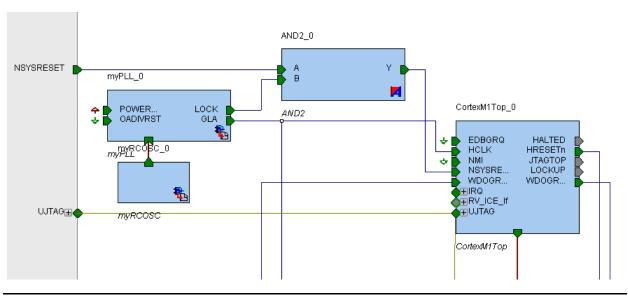


Figure 3-21 • SmartDesign Canvas

The naming of the groups, such as UJTAG, is not important, as the group names are not carried through during design generation.

Promote Signals to Top Level

This SmartDesign component is the top level of this design. Therefore, all of the signals connected to a pin of the FPGA must be at the top level of the SmartDesign canvas. Follow the steps below to promote the signals in Table 3-3 to the top level.

- 1. Go to the Canvas.
- 2. Right-click the UJTAG group of the CortexM1Top_0 instance and choose **Promote to Top** Level.
- 3. Right-click the dataIn[31:0] bus of CoreGPIO_0 instance and choose Add Slice.
- 4. Type 1 and 0 (for [1:0]), as shown in Figure 3-22.

Add Slice	\mathbf{X}
	dataIn [1] : 0]
Help	OK Cancel

Figure 3-22 • Add Slice Dialog Box

- 5. Click OK.
- 6. Right-click on dataln[1:0] and select Promote to Top Level.
- 7. Follow steps 3-6 to promote dataOut[3:0] of Core_GPIO_0 to the top.
- 8. Right-click and choose Promote to Top Level to promote the rest of the signals in Table 3-3

Table 3-3 •Signals to Promote to Top Level

Instance	Signal	Group
CortexM1Top_0	All signals	UJTAG
CoreGPIO_0	dataln[1:0]	dataln[31:0]
	dataOut[3:0]	dataOut[31:0]
CoreMemCtrl_0	MEMADDR[17:0] (requires slice), MEMDATA[31:0], SRAMBYTEN[3:0], SRAMCSN, SRAMOEN, SRAMWEN	ExternalMemoryInterface
CoreUARTapb_0	RX	
	ТХ	

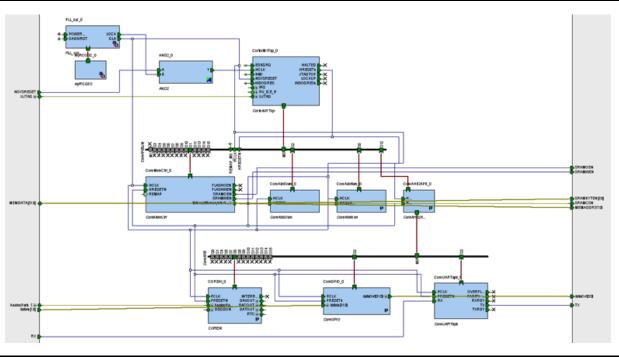
Now, your Smart Design Canvas should resemble the one shown in Figure 3-23 on page 3-34. If you are targeting the M1AFS-ADV-DEV-KIT board perform the following steps to add a second chip select signal for the off-chip SRAM device:

- Right-click to the right of the canvas and choose Add Port.
- Type SRAMCS in the Name field.
- Select **Output** for the direction.
- Click OK. The new SRAMCS port will be added to your canvas.
- Press CTRL and click to select SRAMCS and SRAMCSN.
- Right-click SRAMCS or SRAMCSN and choose Connect.
- Right-click SRAMCS only (not SRAMCSN) and choose Invert.

Note: Make sure SRAMCSN is not highlighted when doing this step.



Tutorial – Create Design



You should see an inverter placed near the SRAMCS port.

Figure 3-23 • SmartDesign Canvas

9. Go to SmartDesign > Show Memory Map / Data Sheet.

An HTML file opens which has the system memory map and register maps for the peripherals. Make sure this matches the memory map shown in Figure 3-24.

CortexM1Top_0 Subsystem

Master(s) on this bus:

• CortexM1Top_0

	Base Address					
	NoRemap	M0_SwapSlots0and1				
<u>CoreAhbN∨m_0 : NVM</u>	0x00000000	0x10000000				
CoreMemCtrl_0 : FLASH	0x10000000	0x0000000				
<u>CoreAhbSram_0 : IRAM</u>	0x20000000					
<u>CoreGPIO_0 : RegisterMap</u>	0xc2000000					
<u>CoreUARTapb_0 : RegisterMap</u>	0xc3000000					
<u>COREAL_0 : RegisterMap</u>	0xc6000000					

subsystem list, top of page

Figure 3-24 • Memory Map

Note: The memory map for CoreMemCtrl_0 is not complete. The SRAM interface for CoreMemCtrl_0 is at address 0x18000000.

Save and Generate the SmartDesign System

The final step within SmartDesign is saving and generating the HDL. Follow the steps below to generate the HDL for your design.

- 1. Right-click on the Canvas and choose Generate Design to generate the HDL design.
- 2. Click OK in the Information window after generation is complete (you receive warnings).

Prior to generating HDL code, SmartDesign checks the connectivity of the signals in the design and produces errors or warnings as appropriate. You should not receive any errors. However, you will receive warnings concerning some unconnected outputs. You can safely ignore these. If you want to see which signals the warnings are concerned with, you can go to the SmartDesign menu and choose **Check Design Rules**. This will launch a read-only Grid-like window which will show you the signals related to the warnings.

If you want to get rid of the warnings, you can mark the floating drivers and unconnected bus interfaces as unused. You will need to create slices for busses which have some bits connected and some floating. Then, you can go to the Design Rules Check grid, highlight all of the unconnected and floating drivers, right-click under the Port Name column, and choose **Mark as Unused**.



3. Close the SmartDesign by clicking on the small **x** in the upper right corner as in Figure 3-25.



Figure 3-25 • Close SmartDesign

Besides generating the HDL design, a testbench file is created along with all the necessary files to run a simulation, using the bus functional model (BFM) and AMBA transfers.

Step 3 – Create Flash Memory System

You are creating this Flash Memory System and Data Storage client to allow you to include software code, as an Intel-Hex file, in the FPGA programming file. This allows the Cortex-M1 processor to boot and run from the NVM.

- 1. Go to the Catalog and expand the Fusion Peripherals category.
- 2. Double-click Flash Memory System Builder. You will see the Flash Memory System window shown in Figure 3-26.

Value Client Type Client Name Address Vod dress Page Initialization Lock Statt Add to System Filena Read Image Image <t< th=""><th>Flash Memory System: C</th><th>reate core</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>X</th></t<>	Flash Memory System: C	reate core									X
Andresse Client Type Client Name Start Address (bex) Word Size Page Initialization Lock Start Address Add to System Add to System Fipelined Read	9 C 🛛 🗙										
Client Type Client Name Address Word Stat End Order Cost Address Kond Size Stat End Order Cost Address Add to System Add to System Pipelined Read End Order Cost Address Optimize Optimize Optimize Optimize Optimize Optimize Optimize	Available client types Clients used in the Flash Memory System										
Image: State in the interview of the interv			CT + T	Cr. IN		Word	Page		Initialization		Lock Start
RAM Initialization CFI Data Add to System. Pipelined Read Image:			Lilent Type			Size	Start	End	Order	Cost	Address
Add to System Pipelined Read Dptimize Generate	RAM Initialization										
Pipelined Read Image:											
<u>Optimize</u>	Add to System										
<u>Optimize</u>											
<u>Optimize</u>	Pipelined Read										
		J									
Help Close		Optimize	1								<u>G</u> enerate
Leip										-	
	Help										Close
Rearty	Ready										

Figure 3-26 • Flash Memory System Window

1ctal

3. Double-click on **Data Storage Client** in the Available client types list. You will see the Add Data Storage Client window shown in Figure 3-27.

NVM		
D:\Projects\2009\FA	DK_CortexM1_Tutorial\AP	_HW\CortexM1_
ent file: Intel-Hex	•	Browse
addressing		
	(hexadecimal only)	
32 💌	bits	
65536	(decimal)	
Prevent write		
	OK	Cancel
	ent file: Intel-Hex addressing 0 32 5536	addressing (hexadecimal only) 32 bits 65536 (decimal) Prevent write

Figure 3-27 • Add Data Storage Client

- 4. Enter NVM in the Client name text box.
- 5. Leave the Start address at 0.
- 6. Change the Size of word to 32 bits.
- 7. Enter the 65536 for the Number of words.
- 8. Click the **Browse** button and select the *CortexM1_Tutorial.hex* file from the *CortexM1_Fusion_HW_Tutorial*

Value of the cortexM1_Fusion_HW_Tutorial
Value of the cortexM1_Fusion_HW_Tutorial of the cortexM1_Fus
- 9. Make sure the Format of memory content file is Intel-Hex.



Tutorial – Create Design

Flash Memory System: I	Modify core - NVM_content	s*							×
<u>୭</u> ⊂ ⊥ X									
Available client types	1	Clier	nts used in the l	Flash Memo	iry System				
Analog System	Client Type	Client Name	Start Address	Word	Pa	ige	Initia	ization	Lock Start
Initialization Data Storage			(hex)	Size	Start	End	Order	Cost	Address
RAM Initialization CFI Data	1 🚺 Data Storage	NVM	0	32	0	2047	N/A	N/A	Γ
Add to System									
E Diselined Based									
Pipelined Read									
	<u>O</u> ptimize								<u>G</u> enerate
Help									Close
Ready									

10. Click **OK**. Now the Data Storage client you just created appears in the Flash Memory System window (Figure 3-28).

Figure 3-28 • Data Storage Client in Flash Memory System Window

11. Click **Generate** to generate the component. You will see the Generate Core window.

12. Enter NVM_contents in the Core name box.

13. Click **OK**.



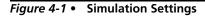
4 – Tutorial – Simulation, Synthesis, and Place-and-Route

Step 4 – Perform Pre-Synthesis Functional Simulation

In this section you will run a pre-synthesis functional simulation to exercise the Bus Functional Model (BFM) to verify AMBA transactions with the peripherals in your system. This step is not necessary, since the Actel cores have already been verified. However, running the BFM is useful when you want to verify the AMBA interface of peripherals you have created.

- 1. Go to **Project** > **Settings**.
- 2. Click on the Simulation tab.
- 3. Change the Value for Simulation runtime to **-all**. Make sure your simulation settings look like those in Figure 4-1.

M	ModelSim options 🔺 DO File	Name	Value
	- Waveforms - Vsim command	Use automatic DO File	N
	Libraries	User defined DO File	
	Fusion COREUARTAPB	Simulation runtime	-all
	- CoreAHBLite_L - COBFALLIB	Testbench module name	testbench
	Top level instance name in the testbench	<top>_0</top>	
		do command parameters	
		Generate VCD file	
		VCD file name	power.vcd



- 4. Click OK
- 5. Click on the **ModelSim** icon.



Tutorial – Simulation, Synthesis, and Place-and-Route

ModelSim is launched and the necessary source files are compiled, including the testbench and peripheral components. At the conclusion of the compilation, the Bus Functional Model (BFM) scripts will be executed to exercise and test the AMBA-based peripherals.

A sequence of reads and writes will occur to the peripherals and the results displayed in the ModelSim log window, as shown in Figure 4-2.

#	Execution of BFM Script Started
#	N-cycle: Write AABBCCDD to address 10000010
#	N-cycle: Read ZZZZZZZ from address 10000010
#	N-cycle: Write AABBCCDD to address 10000010
#	N-cycle: Read ZZZZZZZZ from address 10000010
#	N-cycle: Write 12345678 to address 20000000
#	N-cycle: Read 12345678 from address 20000000
#	N-cycle: Write 9A to address 20000000
#	N-cycle: Read 1234569A from address 20000000
#	N-cycle: Read 9A from address 20000000
#	N-cycle: Read 56 from address 20000001
#	N-cycle: Read 34 from address 20000002
#	N-cycle: Read 12 from address 20000003
#	N-cycle: Read 569A from address 20000000
#	N-cycle: Read 1234 from address 20000002
#	N-cycle: Write BC to address 20000001
#	N-cycle: Write DE to address 20000002
#	N-cycle: Write F0 to address 20000003
#	N-cycle: Read F0DEBC9A from address 20000000
#	N-cycle: Write AABBCCDD to address 20000004
#	N-cycle: Read AABB from address 20000006
#	N-cycle: Write 9876 to address C0000000
#	N-cycle: Read 9876 from address C0000004
#	N-cycle: Read 9876 from address C0000000
#	N-cycle: Write AB to address C1000000
#	N-cycle: Write FF to address C1000004
#	N-cycle: Write 87654321 to address C1000018
#	N-cycle: Write FFFFFFFF to address C100001C
#	N-cycle: Read 00 from address C1000000
	N-cycle: Read 00 from address C1000004
#	N-cycle: Read 00000000 from address C1000018
#	N-cycle: Read 00000000 from address C100001C
#	N-cycle: Write 99 to address C3000074
#	N-cycle: Read 00 from address C3000080
	N-cycle: Write 9876 to address C4000000
#	N-cycle: Read 9876 from address C4000004
#	N-cycle: Read 9876 from address C4000000
#	N-cycle: Write ABCD to address CC000000
	N-cycle: Read ABCD from address CC000004
#	N-cycle: Read ABCD from address CC000000
#	N-cycle: Write 01 to address CF000000
	N-cycle: Read 01 from address CF000000
	N-cycle: Read 01 from address CF000000
	N-cycle: Write 00 to address CF000000
	N-cycle: Read 00 from address CF000000
	Successful Execution of BFM Script Complete
	** Failure: Breakpoint encountered - normal completion of BFM-driven simulation

Figure 4-2 • ModelSim Log Window

If you receive some warnings, you can ignore them.

For more information about the BFM, refer to the Cortex-M1 Handbook on the Actel website:

http://www.actel.com/documents/CortexM1_HB.pdf.

Step 5 – Perform Synthesis

After the functional simulation has completed, synthesis can be performed. Perform the steps below to synthesize the design.

- 1. Launch the Synplicity[®] Synplify[®] tool by clicking on the **Synthesis** button in the Libero IDE Project Flow window. Synplify will launch and load your project. If you see the Organize constraints for Synthesis window, click **OK**.
- 2. Click on the Run button in Synplify to synthesize the design.

Once synthesis is complete you will see many warnings, which are safe to ignore. However, if any errors are present, those need to be corrected prior to continuing. A screenshot of the Synplify tool is shown in Figure 4-3.

	A-2 - [D:/Actelprji/ContexM1_Fusion_FPGA_Design_Tutorial_Files_v1_1/M1AFS_EMBEDDED_KIT/Completed ect [mport IP_gun_Agelyss_HCL-gaelyst_context_gadow_Tech-Support_Web_Heb			
	Ø < 0 B @ @ & 9 0 0 0 5 5 = 0 0 2 2 2 2 3 5 5 5 5 4	0. 0. 0.	9. 11 d b b	
Run	Synplify [®] Pro			
	Done: 0 errors, 258 warnings, 207 notes			
👌 Open Project	synthesis - Actel Fusion : MIAFS1500 : FBGA256 : -1 Synthesis - Actel Fusion : MIAFS1500 : FBGA256 : -1 MIAFS_TUT_TOP_syn] - D:\Actelpr\[CortextM1_Fusion_FPGA_Design_Tutorial_Files_v1_1\]MIAFS_EMEEDDED_KIT\[Coregi		synthesis	
Close Project	C = [101APUU_TOP_ym] - D:Actepr/(critexiti_Posion_ProA_Design_Uuonal_Pies_vi_1/MIAPS_Effections) Verlog O O and Acteprication of the second s	leted_Design(Name 🛆 Size Type Modified	
Add File	🥥 synthesis		Image: Construction Directory 16:48:39 18-Aug-2009 Image: Construction Directory 16:48:39 18-Aug-2009 Image: Construction Directory 16:48:39 18-Aug-2009	
	-		B- Directory 16:48:39 18-Aug-2009 B- Directory Directory 16:48:43 18-Aug-2009	
Change File	1		Image: Synthep Directory 16:48:43 18:40,9:2009 Image: MIAPS_TUT_TOP.areastr 67 kB areastr File 16:49:10 10:40,9:2009 Image: MIAPS_TUT_TOP.ach 216 areastr File 16:49:19 kB:40,9:2009	
Add Implementation			- MIAFS_TUT_TOP.fse 13.k8 fse File 16:49:10 10-Aug-2009	
Implementation Options			MIAFS_TUT_TOP.htm 356 bytes htm File 16:49:10 18-Aug-2009 MIAFS_TUT_TOP.map 28 bytes map File 16:49:10 18-Aug-2009	
Add PSR Implementation	1		M1AFS_TUT_TOP.pdc 129 bytes pdc File 16:49:09 18-Aug-2009	
	4		MIAP5_TUT_TOP.sap 64 k8 sap File 16:48:42 18-Aug-2009	
View Log			- MIAF5_TUT_TOP.so 316 bytes so File 16:49:09 18-Aug-2009	
equency(MHz):			→ ⊕ M1AP5_TUT_TOP.ord 374 k8 Netlist 16:49:08 18-Aug-2009 → → M1AP5_TUT_TOP.orm 2 M8 Netlist (Gate) 16:49:08 18-Aug-2009	
100			- M1AFS_TUT_TOP.srr 259.k8 srr File 16:49:00 18-Aug-2009	
Auto Constrain			MIAF5_TUT_TOP.srs 511 kB Netlist (RTL) 16:48:41 18-Aug-2009 MIAF5_TUT_TOP.sr 31 kB srr File 16:49:10 18-Aug-2009	
M Compiler			☐ M1AFS_TUT_TOP.say 31 k8 say File 16:49:10 18-Aug-2009 ☐ M1AFS_TUT_TOP.tig 70 k8 tig File 16:46:41 18-Aug-2009	
1Explorer			MIAFS_TUT_TOP_odc.sdc 382 bytes sdc File 16:49:09 18-Aug-2009 MIAFS_TUT_TOP_syn.pr) 81/8 pr) File 16:40:17 18-Aug-2009	
timing	-		MIAPS_TUT_TOP_syn.pr) 8 kB pr) File 16:48:17 18-Aug-2009 Image: Image and the synthesis of the synthesynthesis of the synthesis of the synthesis of the synthesis of the	
	-	1	Image: Strategy of the	
	1	4 Þ		
MIAPS_TUT_TOP_syn.prj				
	Information (B)X		Had	
warnings, 207 notes	Eind: global 💌 Set Filter 🗋 Apply Filter 🗹 GroupCommon 10's	Log Parameter	synthesis	
	Message Source Location Log Location Time			
3 CL190 CL157	Optimizing register bit overflow to a constant 0 <u>Rx_async.v</u> <u>MLAPS_TUT_TOP_</u> 16:48:41 T.			
A <u>CU157</u>	Optimizing register bit overflow to a constant 0 <u>Rx server.v.</u> MIAPS TUT TOP, 16:40-41 T. * Cotput APGLL has undriven bits - a simulation mismatch is (for 256x8 (usion v.(29)) MIAPS TUT TOP, 16:40-41 T. (4)			
Script Messages		og Watch		

Figure 4-3 • Synplify Pro

Note that if you are using Synplify (instead of Synplify Pro) your screen will look different. Close Synplify before continuing.



Step 6 – Perform Place-and-Route

Now that you have synthesized your design, you can place-and-route the design. Follow the steps below to place-and-route the design.

- 1. Open Designer by clicking on the **Place & Route** icon on the Libero IDE Design Flow manager.
- 2. The Organize Constraint dialog box comes up, as shown in Figure 4-4.

Organize Constraints for Designer				
Click to select a constraint file in the project, and us 'designer\impl1\M1AFS_TUT_TOP.adb'. Use the Remove button to remove constraint files fr Use the Up/Down arrow buttons to specify the orde	om Designer.			
	Add → Remove			
Designer only supports sdc and pdc as source files. Show this dialog before creating a new ADB				
Help	OK Cancel			

Figure 4-4 • Organize Constraints for Designer Window

3. We do not need the first two files created automatically by SmartDesign and Synplify. Highlight the files not needed and click **Remove**. We will need only the two PDF files we have imported. The constraints organizer should look like Figure 4-5. Click **OK**.

Organize Constraints for Designer	X				
Click to select a constraint file in the project, ar 'designer\impl1\M1AFS_TUT_TOP.adb'. Use the Remove button to remove constraint f Use the Up/Down arrow buttons to specify the	iles from Designer.				
Constraint files in the project: Origin M1AFS_TUT_TOP.pdc M1AFS_ M1AFS_TUT_TOP_sdc.sdc Synplify	Constraint files for Designer: M1AFS_ADV_TUT_VERILOG.PDC M1AFS_ADV_TUT.PDC				
	<u>A</u> dd → ← <u>R</u> emove				
Designer only supports sdc and pdc as source	files.				
Show this dialog before creating a new ADB					
Help	OK Cancel				

Figure 4-5 • Constraints Organizer Window



4. When the device selection wizard comes up (Figure 4-6), select Next twice and then Finish to set the default selection.

Device Selection Wizard		×
Family: Fusion		
Die	Package	
AFS090 AFS250 M1AFS250 U1AFS250 AFS600 M7AFS600 U1AFS600 U1AFS600 P1AFS600 AFS1500	▲ 256 FBGA 484 FBGA 676 FBGA	
Speed: -2	Die voltage:	
Cancel	< Back Next >	Help

Figure 4-6 • Device Selection Wizard

- 5. Click **Compile** and **OK** with default setting to compile the design.
- 6. Click the **Layout** icon in Designer and accept all default settings by clicking **OK** in the windows that appear. First Compile and then Layout will be performed. Once the Layout has finished, you can proceed to the next step. This will take longer than the compilation of the previous step.
- 7. Click the **Timing Analyzer** icon to analyze the timing of the design. Note that the timing requirement for the system clock (myPLL_0/Core:GLA) is automatically created because you are using a PLL. If any of the clocks in the design are not meeting the constraints set in the constraint files, you will see a red X next to the clock in the window in the left upper corner. Make sure that none of the clocks have a red X next to them. Close the Timing Analyzer window.



5 – Tutorial – Programming

Step 7 – Generate Programming File with Software Code in NVM

In this section, you will associate the Data Storage client you created earlier with the embedded flash memory inside the Fusion device. This will place the software code, an Intel-Hex file, into the embedded flash memory in the Fusion device and include it in the FPGA programming file. Complete the steps below.

Click the Programming File icon in the Designer window. You will see a window similar to the one in Figure 5-1.

FlashPoint - Programming File Generator - Step 1 of 1	
Silicon feature(s) to be programmed:	
C Security settings	
🔽 FPGA Array	
FlashROM	
Original FlashROM configuration file:	
Import	
Embedded Flash Memory Blocks (EFMB):	
Program Block Block Name Cocation Original Configuration File	
1 🔥 🔽 CoreAhbNvm_0/ 3 Modify	
Programming previously secured device(s)	
Specify I/O States During Programming	
Silicon signature (max length is 8 HEX chars):	
Help Back Finish Cancel	

Figure 5-1 • FlashPoint Programming File Generator

- 6. Click the Modify button. The Modify Embedded Flash Memory Block window appears.
- 7. Click the Import Configuration File button. The Import window appears.
- 8. Browse to <project directory>/smartgen/NVM_contents/NVM_contents.efc.
- 9. Click Import.
- 10. Click **OK**.
- 11. Click Finish. The Generate Programming Files window appears.





- 12. Make sure that Programming Data File (*.pdb) is checked.
- 13. Click Generate.

Once the Programming File icon in Designer turns green, the programming file for the Fusion device is generated and you are ready to program the device with your Cortex-M1 design. A completed Actel Designer desktop is shown in Figure 5-2.

14. Close Designer. Click **Yes** if prompted to save changes to M1AFS_TUT_TOP.adb.

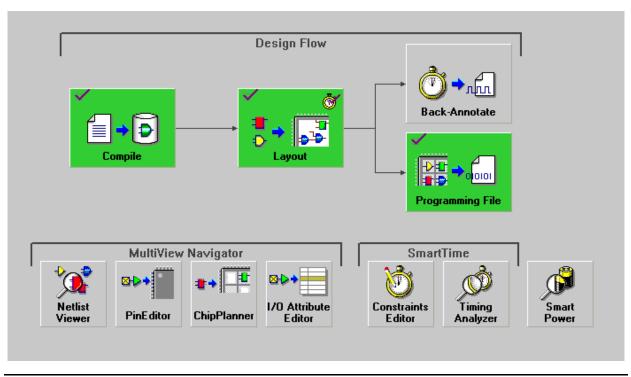


Figure 5-2 • Actel Designer Desktop

Step 8 – Connect to the Target

Before programming the FPGA, you will connect to the target board and setup HyperTerminal to communicate over the UART in your design. Perform the following steps to setup the communication.

- Open the HyperTerminal application (Start > Programs > Accessories > Communications > HyperTerminal). Enter M1AFS_Tutorial on the Name field in the Connection Description dialog box and click OK.
- 2. Select the COM port you identified in the Getting Started Section of this tutorial and click **OK**.
- 3. Enter the following for the properties (Figure 5-3):
 - Bits per second:57600
 - Data bits: 8
 - Parity: None
 - Stop bits: 1
 - Flow control: None

Port Settings		
<u>B</u> its per second:	57600	*
<u>D</u> ata bits:	8	~
<u>P</u> arity:	None	~
<u>S</u> top bits:	1	~
<u>F</u> low control:	None	~
	<u>R</u> estore D	efaults
	K Cancel	

Figure 5-3 • COM3 Properties

4. Click **OK**. HyperTerminal is now connected with the appropriate settings to communicate with the UART on the target design.

Step 9 – Program the M1AFS1500 FPGA

Now that you have created the Cortex-M1 processor system and generated the corresponding FPGA programming file, you are ready to program the FPGA with your design. Follow the steps below to download the programming file to the FPGA.

1. Confirm that the FlashPro3 programmer is connected as described in Table 2-3 on page 2-11.

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- 2. Important: Do not interrupt power during programming since damage to the device might occur.
- 3. Click on the Programming (FlashPro) icon in the Project Flow tab in Libero IDE Project Manager.

FlashPro - [M1AFS_TUT_TOP]	
Ele Edit View Tools Programmers Configuration Customize Help	
New Project Image: Configure Device Open Project Image: Configure Device	PROGRAM
× Programmer Name	Programmer Programmer Programmer Type Port Status Enabled
1 40342	FlashPro3 usb40342 (USB 2.0)
Refresh/Rescan for Programmers	
RefrestvRescan for Programmers	
 Software Version: 8.5.1.13 PDB file 'D'\CotteXHI Fusion FPGA Design Tutorial Files v1 O\H1AFS_EMBEDDED_KIT\Completed_Desi DESIGN: MIAFS TUT TOP; CHECKSUM: E695; PDB_VERSION: 1.5 Driver: 2.0.4 build 5 programmer' 40342': FlashPro3 Opened 'D'\CotteXHI Fusion FPGA_Design_Tutorial_Files_v1_O\H1AFS_EMBEDDED_KIT\Completed_Design Checking for software updates Info: This software version is up to date. There are no available updates. 	gn\Verilog\Mi&FS_EMB_M1_TUT\designer\impli\Mi&FS_TUT_TOP_fp\Mi&
	2
IIIII All ∧ Errors ∧ Warnings ∧ Info /	

Figure 5-4 • FlashPro Project Flow

- Note: If you receive messages about new hardware detected on your machine, complete the USB driver installation as described in the "Getting Started" section of the FlashPro User's Guide (www.actel.com/products/hardware/program_debug/flashpro/default.aspx#docs).
 - 4. Click the PROGRAM button to program the Fusion device (Figure 5-4). Once programming is complete, the Programmer Status will show **RUN PASSED** in green.



5. Press SW1 on the board to reset the system (Figure 5-5 and Figure 5-6 on page 5-50).



Figure 5-5 • Fusion Embedded Development Kit Reset System with SW1



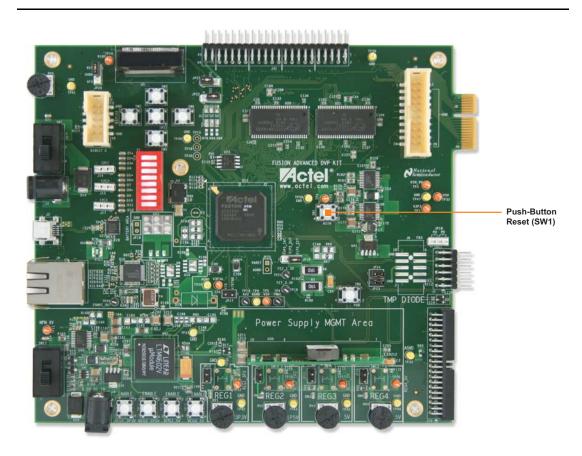


Figure 5-6 • Fusion Advanced Development Kit Board Reset System with SW1

6. After pressing the reset button (SW1), you should see some of the LEDs counting.

7. Go to the HyperTerminal window. You should see the message shown in Figure 5-7 in the HyperTerminal window.

M1AFS_Tutorial - HyperTerminal		
File Edit View Call Iransfer Help 마글국 @ 종 #마놈마 657		
D ≌ ∞ Ѯ ⊫ Ҽ ≌ Press any key to display	v current analog inputs values.	
Connected 0:00:28 Auto detect 57600	8-NJ-1 SCROLL CAPS NUM Capture Print echo	

Figure 5-7 • HyperTerminal Window



Tutorial – Programming

8. Press any key. You should see something like the window shown in Figure 5-8.

M1AFS_Tutorial - HyperTerminal Eile Edit View Call Transfer Help Eile Edit View Call Transfer Help Eile Edit View Call Transfer Help		
Press any key to display c	current analog inputs values.	
AVO : 3310 mV AV1 : 1430 mV AT2 : 32 C	ACO : 286 mA ACI : 537 mA ACL : 2 mA	
-		
Connected 0:01:32 Auto detect 57600 8-N-	1 SCROLL CAPS NUM Capture Print echo	<u>.</u>

Figure 5-8 • HyperTerminal Display

- 9. Change the potentiometer on the development board (upper left corner on M1AFS-EMBEDDED-KIT and near power supply for M1AFS-ADV-DEV-KIT)).
- 10. Press any key. The AC4 value should change.
- 11. The design is measuring the voltage across the potentiometer. You should be able to measure a range of about 0 V to 3.3 V across the potentiometer.

Congratulations!!

You have successfully created a Cortex-M1 system. Now you are ready to develop software for your Cortex-M1 design. If you want to learn how to get started developing software for the Cortex-M1, refer to the ARM Cortex-M1 Embedded Processor Software Development Tutorial for Fusion Mixed-Signal FPGAs (www.actel.com/documents/CortexM1_Proc_SW_Tutorial_UG.pdf).



6 – List of Document Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (50200162-1)	Page
50200162-1 (March 2009)	The "Requirements for this Tutorial" section was revised. FlashPro v8.6 or newer is required. Several of the versions were updated in the "Intellectual Property (IP)" section.	5
	The "Before You Get Started" section was revised to change the names of the files and file hierarchy.	9
	The "Tutorial – Create Design" section was revised to match the new file names and screen shots were updated as appropriate.	13
	The "Instantiate CoreAI" section was significantly changed.	22
	The "Instantiate CoreUARTapb" section was updated, including EQ 3-1.	26
	Table 3-2 • VCC and GND Connections was revised.	32
	Figure 4-3 • Synplify Pro was replaced.	41
	"Step 6 – Perform Place-and-Route" was significantly revised.	42
	The "Save and Generate the SmartDesign System" section was updated with additional information.	35
50200162-0 (March 2009)	The "Download Tutorial Files" section was revised to guard against problems created by a directory name that is too long.	9



A – Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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The technical support email address is tech@actel.com.

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