# **Creating Analog Testbenches**

for Fusion Designs



#### Actel Corporation, Mountain View, CA 94043

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Printed in the United States of America

Part Number: 50200092-0

Release: March 2007

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## Introduction

This tutorial demonstrates how to create analog testbenches for Fusion FPGAs using Libero® IDE and WaveFormer Lite.™

To create an analog testbench, follow the steps below:

- 1. Chapter 1 Setting Up the Example Files
- 2. Chapter 2 Configuring the Voltage/Temperature Monitor
- 3. Chapter 3 Creating the Analog Testbench
- 4. Chapter 4 Simulating the Fusion Design

This tutorial assumes basic knowledge and experience with the Libero IDE design flow and WaveFormer Lite testbench generation tool. For more information about Libero, refer to the *Libero User's Guide*, available at the Actel web site (www.actel.com).

## **Setting Up the Example Files**

In this step, you will set up the project files for the Fusion design used in this tutorial.

- 1. Download the Creating an Analog Testbench tutorial supplemental files from the Actel website.
- 2. Create a new folder on your C drive named VT\_Mon (C:\Actelprj\VT\_Mon).
- 3. Unzip the supplemental files to the C:\Actelprj\VT\_Mon folder.
- 4. From the Start menu, choose Actel Libero IDE or double-click the Actel Libero IDE icon on the desktop.
- 5. From the File menu, choose Open Project.
- 6. Browse to C:\Actelprj\VT\_Mon and click OK. This opens the VT\_Mon project in Libero IDE (see Figure 1-1).

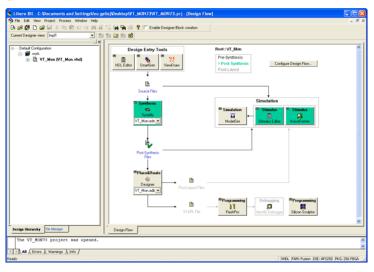


Figure 1-1 · Libero IDE Design Flow Window with VT\_Mon Project

Note: If the Tool Profile Conflict dialog box appears, select Use the profile currently selected in Libero IDE and click OK.

# **Configuring the Voltage/Temperature Monitor**

This step uses SmartGen to configure the voltage and temperature monitor Fusion peripherals and implements them in the design HDL code. The intended function for this design is to monitor a supply voltage and a temperature, and send flags to the Fusion system when the voltage rises above 5.25 V or falls below 4.75 V, and when the monitored temperature exceeds 70° C.

In this step, you will configure a voltage monitor, a temperature monitor, and two gate drivers. The gate driver functions are responsible for sending flags to the Fusion system, which could then either control the input environment or sound alarms, or both.

1. Launch SmartGen by clicking the SmartGen button from the Libero IDE interface. This opens the SmartGen tool (Figure 2-1).

) 📽 🎥 🗊 🔋	Core Varieties for Fusion Family					
<ul> <li>Analog System Builder</li> </ul>	Variety	Function	Vendor	Manine	Datali	
<ul> <li>Analog System builder</li> <li>Arithmetic</li> </ul>	Analog System Builder	Analog System		1.2	Analog System Builder	
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* II Counters	Event Kung	A-55m	Actel	20	Area optimized, Medium Speed	
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Figure 2-1 · SmartGen Window

- 2. Under the Categories tab, click the Analog System Builder category.
- 3. In the Variety window, double-click Analog System Builder. The Analog System Builder (ASB) core configurator (Figure 2-2) allows you to select the required analog functions, the analog inputs that need to be configured, and the specific threshold values required to send event flags to the system logic.

						_
Analog System Builder: Cre	ate core					
ADC Configuration	MHz ADC Clock:	Resolut	ion: 10	r bits	2	idvanced Options
Available peripherals:	Peripherals used in system:					$\mathcal{I} \times$
Vokage Monitor Current Monitor Temperature Monitor	Peripheral	Signal	Туре	Acquisition time (us)	Sampling Bate (ksps)	Package Pin
Colferential Volkoge Menitor Clinet Digital Tiput Gale Driver Real Time Counter Informal Yonge Menitor Informal Volkoge Menitor						
	Modify Sampling Sequence					Generate
Help						Close

Figure 2-2 · Analog System Builder Configurator for Fusion

#### Configuring the Voltage/Temperature Monitor

- 4. In the ADC Configuration panel, enter 40.0 as the System Clock frequency and 10.0 as the Resolution.
- 5. From the Available peripherals list, select Voltage Monitor and click Add to System. This opens the Configure Voltage Monitor Peripheral window.

This input signal configuration will signal the system when the voltage on the AV5V input pin is 5.25 V or higher for one sample, or 4.75 V or lower for the other sample. The ASB will deassert (remove) the system flag after two consecutive samples when the signal falls under 5.25 V or rises above 4.75 V.

- 6. Enter the following information (as shown in Figure 2-3) :
  - Signal name: AV5V
  - Acquisition time: 1.0
  - Maximum voltage: 5.5
  - Enter the following information for Flag 1:
  - Flag Name: over5p25
  - · Flag Type: over
  - Threshold (V): 5.25
  - Assert Samples: 1
  - Deassert Samples: 2
  - Enter the following information for Flag 2:
  - Flag Name: under4p75
  - Flag Type: under
  - Threshold (V): 4.75
  - Assert Samples: 1
  - Deassert Samples: 2

Configure Vo	ltage Mor	nitor Periph	eral					
	AV pad	Signal name:		Pr	escaler	•)-		
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1 2 3 4	OVER5P2 UNDER4F		OVER UNDER		5.25	1		2 2
Help					[	ОК	Car	ncel

#### Figure 2-3 · Configure Voltage Monitor Peripheral Window

- 7. Click OK. This adds the voltage monitor peripheral to the list of peripherals used in the system.
- 8. From the Available peripherals list, select Temperature Monitor and click Add to System. This opens the Configure Temperature Monitor Peripheral window.

This signal will send a flag to the system when one sampling of the input is  $70^{\circ}$  C or higher. Fusion will remove the system flag when the temperature is lower than  $70^{\circ}$  C for two samples.

- 9. Enter the following information (as shown in Figure 2-4) :
  - Signal name: Temp
  - Acquisition time: 10.0

Enter the following information for Flag 1:

- Flag Name: over70C
- Flag Type: over
- Threshold (C): 70
- Assert Samples: 1
- Deassert Samples: 2

õignal nai	nperature Monitor	Peripheral	Acquisition time:	10.0	
-Digital f				1.010	us
	value: 0.000	c			
		Comparison Flag	Specification		<u>*</u> ×
	Flag Name	Flag Type	, Threshold (C)	Assert Samples	De-assert Samples
1	over70C	OVER	70	1	2
2					
4					
4 5					
5					×
5					



- 10. Click OK. This adds the temperature monitor peripheral to the list of peripherals used in the system.
- 11. From the Available peripherals list, select Gate Driver and click Add to System. This opens the Configure Gate Driver Peripheral window.

You will configure the gate driver function for the voltage monitor. The gate driver enable in this case is designed to be the logical NOR of the over and under threshold flags.

- 12. Enter the following information (as shown in Figure 2-5 on page 12):
  - Signal name: Supply\_good
  - Enable signal name: Supply\_good\_en
  - Source current: 1.000

Configuring the Voltage/Temperature Monitor

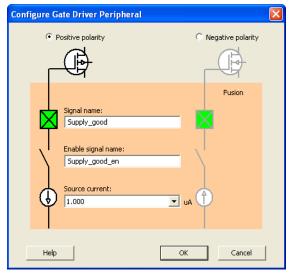


Figure 2-5 · Configure Gate Driver Peripheral Window

- 13. Click OK. This adds the gate driver peripheral to the list of peripherals used in the system.
- 14. From the Available peripherals list, select Gate Driver and click Add to System. This opens the Configure Gate Driver Peripheral window.

You will configure the gate driver function for the temperature system output flag when the temperature exceeds  $70^{\circ}$  C. In this design, the Over\_temp flag is used as the gate driver enable.

- 15. Enter the following information (as shown in Figure 2-6 on page 13):
  - Signal name: Over\_temp
  - Enable signal name: Over\_temp\_en
  - Source current: 1.000

Configure Gate Driver Peripheral	
Positive pularity     Negative pular	rilγ
Fusion Signal name: Over_temp Enable signal name: Over_temp_en	
Source current:	
Help OK Cance	<u>i</u>

Figure 2-6 · Configure Gate Driver Peripheral Window

- 16. Click OK. This adds the gate driver peripheral to the list of peripherals used in the system.
- 17. Click Generate. This brings up the Generate Core dialog box (Figure 2-7).

Generate Core	
Configured cores	a
1	
Core name:	newCore
Output format:	VHDL
Help	OK Canrel

Figure 2-7 · Generate Core Dialog Box

- 18. Enter *VT\_Mon* as the Core name and click OK.
- 19. Click Close to close the Analog System Builder window.
- 20. From the File menu, choose Exit to close SmartGen.

To complete this design you will need to configure and make proper connections to the Flash Memory System Builder. Doing so is beyond the scope of this tutorial.

## **Creating the Analog Testbench**

The next step in a Fusion design flow is to synthesize your design and create a testbench.

SynaptiCAD's WaveFormer Lite v11.11d provides the capability to create and generate a testbench with analog and digital signals. The input signals for the voltage and temperature inputs for the VT\_Mon design can easily be drawn using the WaveFormer Lite user interface.

1. Click the **Stimulus WaveFormer** button in the Libero IDE design flow window to launch WaveFormer Lite. This opens the WaveFormer Lite user interface.

Libero IDE finds the clock and respective input/output signals of the VT\_Mon design. Clock and signal names are already identified in the waveform window. The SYS\_CLK, SYS\_RESET, and INIT\_POWER\_UP input signal names have already been entered in the GUI (Figure 3-1).

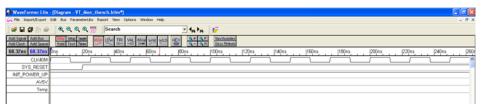


Figure 3-1 · Initial WaveFormer Lite Timing Diagram

The VT\_Mon testbench in WaveFormer Lite has already been configured with a 40 MHz clock, the Initial\_Power\_Up signal goes active high at 10 ns, and the System Reset signal goes active high at 40 ns. The analog inputs AV5V and Temp can now be configured in the WaveFormer window.

- 2. From the Options menu, choose Display Unit > 1µs.
- 3. Double-click the AV5V signal name to open the Signal Properties dialog box.
- 4. In the Signal Properties dialog box, set the following information:
  - Direction: output (default)
  - Size Ratio: Enter 3 to increase the vertical height of the waveform display row.
  - Signal Type: actel\_voltage
  - Radix: real
  - Label Eqn (Equation): Use the arrow 🔟 to open a pop-up list of waveform types. For this testbench, select Ramp (StartV,EndV,Duration). This option enables you to easily insert a ramp of beginning and ending voltages over a specified duration. A ramp waveform equation is perfect for creating a long, slow voltage variation that might be experienced by a voltage monitor input signal in this particular design.

Note: When starting a new waveform, be sure the window is clear of any other equations.

#### Creating the Analog Testbench

Signal Properties 5 W O R D ?	, (Concatenate) Inc(start,increment,count)
orginal reportion	Dec(start, decrement, count)
Name: AV5V Control Active Low	IncString("string",start,increment,count)
	Range(start,finish,count)
Simulate Once Analog Props Grid Lines	RandInt(count, Range_to_zero)
O Drive     C Simulate     O Watch     O Compare	Hex(list) Bin(list)
Equation Entry Verilog VHDL	Rep((list), count)
	Skip(count)
Type: Boolean Eqn 💌 ex. (SIG1 and SIG2) delay 5	File("filename.txt")
	Signal("signalname")
	map {operations} list
Clock: Unclocked 💌 Edge/Level: pos 💌	PRBS7(length,seed)
Set: Not Used 🔻 Clear: Not Used 👻	PRBS15(length,seed)
	Sin(amplitudeV, period, duration)
Clock Enable: Not Used 💌 Advanced Register	SinStart(amplitudeV, period, duration)
	SinEnd(amplitudeV, period, duration)
	CapCharge(amplitudeV, RC, duration) CapDischarge(amplitudeV, RC, duration)
Wfm Eqn 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V 5=X 💌	Ramp(StartV,EndV,Duration)
Label Eqn Ramp(0,0,500)	Kanp(Starty)Endy(Baration)
Export Signal Direction: output	
Analog Display Size Ratio: 3	
Signal Type: actel_voltage	
Radix: real V Bus MSB: LSB:	
Radix: real 💽 Bus MSB: LSB:	
🔲 Falling Edge Sensitive 📃 Rising Edge Sensitive	
OK Cancel Apply Prev Next	

For the initial AV5V signal, edit the ramp equation to Ramp(0,0,500) and click Label Eqn (Figure 3-2). The AV5V data shows a steady state zero voltage for 500  $\mu$ s.

Figure 3-2 · WaveFormer Lite Signal Properties Dialog Box

You can add a subsequent value to the ramp equation that specifies the number of increments to be used in the duration. In the AV5V testbench example, to complete the waveform, each ramp and duration is required to be implemented in five or eight increments (see Step 5 below). More increments would have the effect of providing a smoother waveform.

- 5. With the **Signal Properties** dialog box still open, insert the following series of ramp equations, and click the **Label Eqn** button:
  - Ramp(0,0,500) Zero voltage for 500 μs
  - Ramp(1,5,200,8) Ramps from 1.0 V to 5.0 V in 200 µs, in 25 µs increments
  - Ramp(5,5,100,5) Voltage stays steady at 5.0 V for 100 μs
  - Ramp(5,5.5,200,8) Ramps from 5.0 V to 5.5 V in 200 µs, in 25 µs increments
  - Ramp(5.5,5.5,100,5) Voltage stays steady at 5.5 V for 100 μs
  - Ramp(5.5,5,200,8) Ramps from 5.5 V to 5.0 V in 200 µs, in 25 µs increments
  - Ramp(5,5,100,5) Voltage stays steady at 5.0 V for 100 μs
  - Ramp(5,4.6,200,8) Ramps from 5.0 V to 4.6 V in 200 µs, in 25 µs increments
  - Ramp(4.6,4.6,100,5) Voltage stays steady at 4.6 V for 100  $\mu s$
  - Ramp(4.6,5,200,8) Ramps from 4.6 V to 5.0 V in 200 µs, in 25 µs increments
  - + Ramp(5,5,200,5) Voltage stays steady at 5 V for 200  $\mu s$
  - Note: Clear the Label Eqn field prior to entering each equation to avoid duplicating the same equation for the next segment of the waveform.



The total signal duration is  $2100 \ \mu s$ .

WaveFormer easily concatenates the new data waveform to the preceding waveform so that a continuous waveform is created.

- 6. Click OK.
- 7. Right-click the Temp signal name to open the Signal Properties dialog box for the Temp signal.
- 8. In the Signal Properties dialog box, set the following information:
  - Direction: output (default)
  - Size Ratio: Enter 3 to increase the vertical height of the waveform display row.
  - Signal Type: actel\_temperature
  - Radix: real
  - Label Eqn (Equation): Use the arrow 🔟 to open a pop-up list of waveform types, and select Ramp (StartV,EndV,Duration). In the case of temperature, use values in degrees Celsius, starting with 70° C.
- 9. Enter the following series of ramp equations, incorporating each by clicking the Label Eqn button:
  - Ramp(50,50,500) Temperature stays steady at 50° C for 500 µs
  - Ramp(50,70,400,16) Temperature increases from 50°C to 70°C in 400 µs in 25 µs increments
  - Ramp(70,72,200,8) Temperature increases from 70° C to 72° C in 200 µs in 25 µs increments
  - Ramp(72,72,200,10) Temperature stays steady at 72°C for 200 μs
  - Ramp(72,70,200,8) Temperature drops from 72°C to 70°C in 200 µs in 25 µs increments
  - Ramp(70,68,200,8) Temperature drops from 70°C to 68°C in 200 µs in 25 µs increments
  - Ramp(68,72,200,8) Temperature ramps from 68°C to 72°C in 200 µs in 25 µs increments
  - Ramp(72,71,200,8) Temperature drops from 72° C to 71° C in 200 µs in 25 µs increments The total signal duration is 2100 µs

The total signal duration is 2100  $\mu$ s.

10. Click **OK**. The resulting data for the AV5V and Temp signals is shown in the WaveFormer window as individual pulses or increments with the analog values for each increment (Figure 3-3).

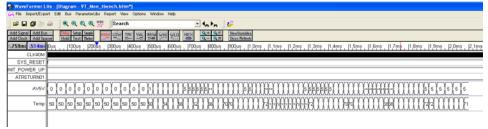


Figure 3-3 · Resulting Waveform for AV5V Voltage Monitor Signal

#### Creating the Analog Testbench

File Import/Export	Edit Bus Paran	neterLibs Proje	t Report View	v Options Wind	fow Help							- 8
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CLK40M												
SYS_RESET								_				
IT_POWER_UP												
ATRETURN01								_				
AV5V												
Temp												
VAREF												
Supply_good												
Over_temp												

If you use SynaptiCAD WaveFormer Pro software, check Analog Display in the Signal Properties dialog box to provide a visual representation of the analog signal (Figure 3-4).

Figure 3-4 · Resulting WaveForm Pro Waveform for AV5V Voltage Monitor Signal

- 11. From the File menu, choose Save.
- 12. From the Import/Export menu, choose Export Timing Diagram As. In the Export dialog box, select VHDL w/Top Level Test Bench (.vhd) and click OK.

## **Simulating the Fusion Design**

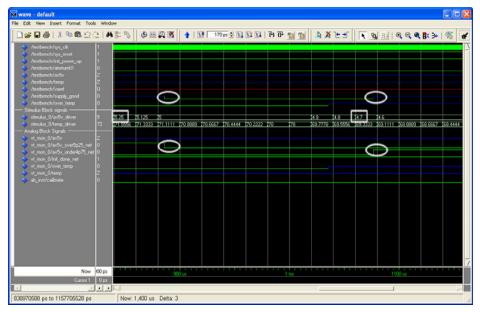
In this step, you will simulate the design.

- 1. Right-click the **Stimulus Editor** button in the Libero IDE interface and choose **Organize Stimulus**. This opens the Organize Stimulus dialog box.
- 2. Select your testbench file and click Add. This adds your testbench to the Associated Files list (Figure 4-1).

Organize Stimulus	
Click to select a stimulus file in the project, and Use the Remove button to remove associated f Use the Up/Down arrow buttons to specify the The top level module should appear last in the I	files. compilation order for the simulator.
Stimulus files in the project: VT_Mon_tbench_equ.vhd	Associated files:
	<u>A</u> dd → ← <u>R</u> emove
Help	OK Cancel

Figure 4-1 · Organize Stimulus Dialog Box

- 3. Click OK.
- 4. Click the **Simulation ModelSim** button. This opens the ModelSim user interface. The results of the simulation for the VT\_Mon design are shown in Figure 4-2 and Figure 4-3 on page 20.

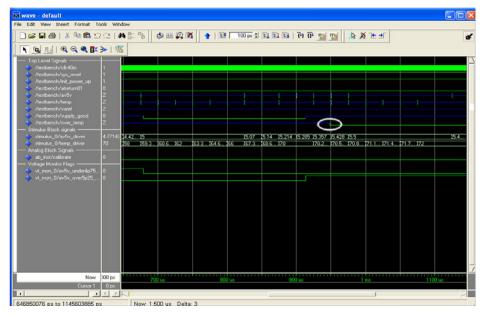


#### Figure 4-2 · Effect of the AV5V Input Testbench after Simulation

Figure 4-2 demonstrates the effect of the varying voltage on the AV5V input. The stimulus\_0/av5v\_driver line shows that part of the waveform where the voltage is initially 5.25 V and ramps down below 4.75 V between 800 and 1100  $\mu$ s. As specified by the AV5V maximum voltage threshold flag, and visualized by the /testbench/supply\_good

#### Simulating the Fusion Design

output signal, the Fusion logic asserts the overvoltage flag where the voltage is exceeding 5.25 V and deasserts it as the voltage drops below 5.25 V. The threshold flag remains deasserted until the voltage drops below 4.75 V, where it reasserts, as indicated by the vt\_mon\_0/av5v\_under4.75v logic and /testbench/supply\_good output signal, at approximately 1080  $\mu$ s. Any delay between the input voltage signal and the respective flag threshold value is a function of the specified sampling rate, resolution of the analog to digital converter, and number of samples taken before assert/deassert flag is set. The AV5V testbench works as desired, clearly showing the assert/deassert of the flags based on the requested thresholds.





The temperature monitoring threshold flag in the Fusion ASB has been set to assert when the temperature exceeds  $70^{\circ}$  C and will deassert when the temperature is less than or equal to  $70^{\circ}$  C. Figure 4-3 demonstrates the effect of a varying temperature on the Temp input of the design, where the temperature is rising from  $50^{\circ}$  C and passes through  $70^{\circ}$  C. Note that the testbench/over\_temp signal, which has been deasserted, asserts as the temperature passes above  $70^{\circ}$  C, and the /testbench/over\_temp output simultaneously asserts as directed by the threshold detection logic. Any delay in the actual assertion or deassertion as compared to the input temperature is a function of the specified sampling rate and resolution of the analog to digital converter. The Temp testbench shows the over\_temp assertion/assertion as the temperature rises above the specified threshold of  $70^{\circ}$  C.

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Product Support

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The technical support email address is tech@actel.com.

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