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TOTAL IONIZATION DOSE TEST REPORT

No. 99T-RT1280A-2
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1.0 SUMMARY TABLE

A1280A Parametrics/Characteristics	Results
1. Functionality	Not tested to the limit, Passed 12 krad(Si) (Table 4)
2. $I_{DDSTDBY}$	Passed 12 krad(Si) (~ 9mA) (Figure 3)
3. V_{IL}/V_{IH}	Passed 12 krad(Si) (Table 5)
4. V_{OL}/V_{OH}	Passed 12 krad(Si) (Figures 4, 5)
5. Propagation Delays	Passed 12 krad(Si) (Table 6)
6. Rising/Falling Edge Transient	Passed 12 krad(Si) (Figures 6-13)

2.0 TID TEST

This section describes the device under test (DUT), the irradiation parameters, and the testing method.

2.1 TEST DEVICE

Table 1 lists the DUT information.

Table 1

Part Number	A1280A
Package	CQFP176
Foundry	MEC
Technology	0.8 µm CMOS
Die Lot Number	U1H486
Date Code	9843
Quantity Tested	4
Serial Numbers	LAN1001 (Control), LAN1002, LAN803, LAN1005

2.2 IRRADIATION

Table 2 lists the irradiation parameters.

Table 2

Facility	NASA
Radiation Source	Co-60
Dose Rate	1.8 krad(Si)/day (+-10%)
Final Total Dose for DC/AC Parameter Measurement	12 krad(Si)
Temperature	Room
Bias	5 V

2.3 TESTING METHOD

The testing method is following the spirit of TM1019 with modifications to simulate, as closely as possible, the extremely slow-dose-rate space environment. Figure 1 shows its flow. Rebound annealing at 100°C is omitted in the flow, since there are enough data showing that Actel's FPGA had no rebound effects (see, for example, the most recent TID Report No. 98-T14100-2).

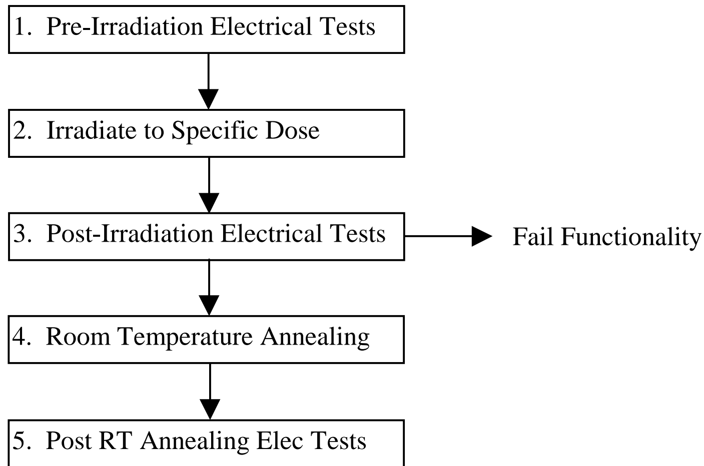

Figure 1. Test method flow-chart

2.4 ELECTRICAL PARAMETERS/CHARACTERISTICS TESTS

The electrical parameters/characteristics were measured on bench with relative low noise. The corresponding logic design circuits are listed in Table 3.

Table 3

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power line
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	CMOS output
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output

3.0 TEST RESULTS

This section presents all the parameteric testing results for pre-irradiation (step 1 in Figure 1), post-irradiation (step 3), and post room temperature annealing tests (step 5).

3.1 FUNCTIONAL TEST

Table 4 lists the functional testing results of four testing DUTs.

Table 4. Functionality Test

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN1001	passed	passed	passed
LAN1002	passed	passed	passed
LAN1003	passed	passed	passed
LAN1005	passed	passed	passed

3.2 IDDSTANDBY

$I_{DDstandby}$ was monitored during the irradiation and annealing period. Because the board had a measurable leakage, only the delta $I_{DDstandby}$ due to radiation and/or annealing was recorded. Using delta instead of $I_{DDdstandby}$ do not create significant extraneous errors since the pre-irradiation value of $I_{DDstandby}$ is only approximately 0.5 mA. The increment of $I_{DDstandby}$ due to radiation is defining the tolerance.

The original three testing-DUTs, series number LAN1002, LAN1003, and LAN1005 were irradiated until $I_{DDdstandby}$ reached closing to 25 mA. Previous experience indicates this being the right point to stop the irradiation and perform the testing and subsequent annealing. However, the dosimetry of these three DUTs was found not well calibrated after the post-irradiation measurement and annealing. To find the right dose, the control DUT and a new DUT were irradiated at the same spot after all the measurements were done. Figure 2 shows the delta $I_{DDstandby}$ versus total dose of the two calibration-DUTs. It indicates that the original three DUTs were irradiated well over 12 krad(Si). To be conservative, we will report the testing DUTs been irradiation up to 12 krad(Si).

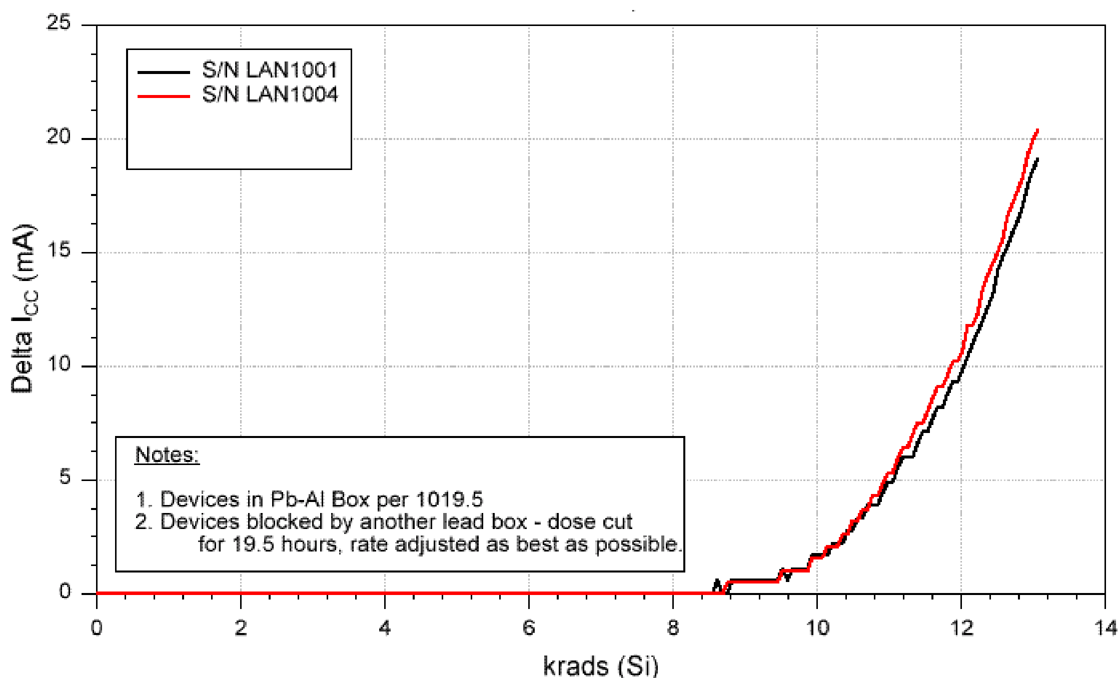

Figure 2. Delta $I_{DDstandby}$ versus total cumulative dose

Room temperature annealing was performed after 12 krad(Si) irradiation. Figure 3 shows the room temperature annealing characteristics in which delta $I_{DDstandby}$ dropped to approximately 9 mA after approximately 480 hours of annealing.

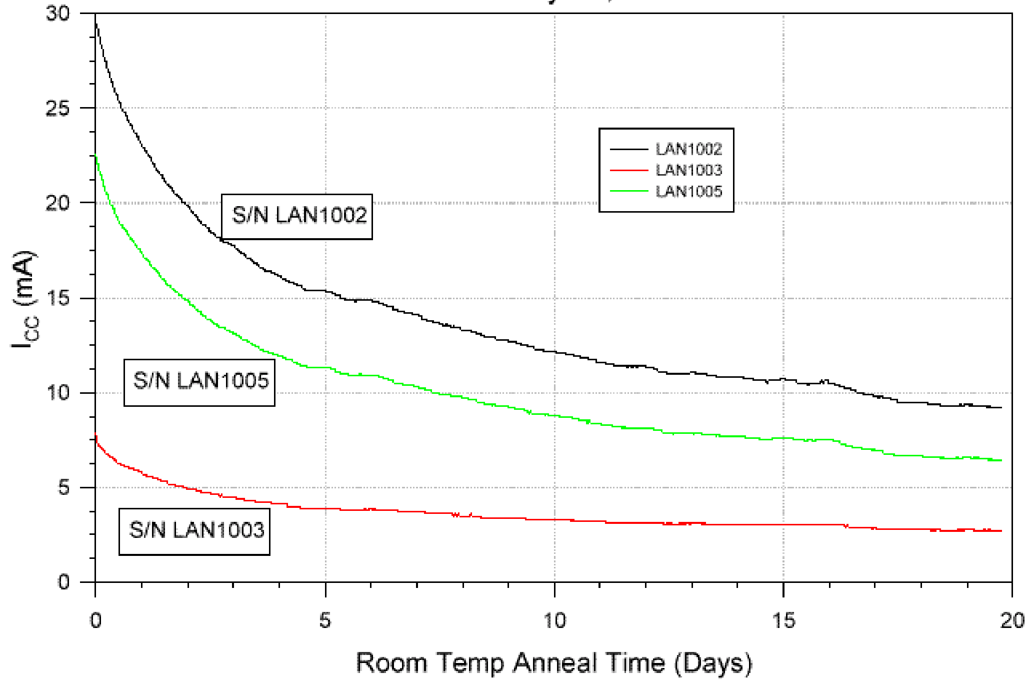

Figure 3. $I_{DDstandby}$ room temperature annealing curve of DUTs post 12 krad(Si) irradiation

3.3 INPUT LOGIC THRESHOLD

The testing results of input logic threshold (V_{IH}/V_{IL}) are tabulated in Table 5. The measurement setup is operated at a resolution of approximately 0.1 V.

Table 5. Input Logic Threshold Voltage (V)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN1001	1.6	1.6	1.6
LAN1002	1.6	1.8	1.8
LAN1003	1.6	1.8	1.8
LAN1005	1.6	1.6	1.6

3.4 OUTPUT CHARACTERISTICS

The output drive characteristics were measured only at step 5, after room temperature annealing. Figure 4 shows the V_{OL} characteristics, and Figure 5 shows the V_{OH} characteristics.

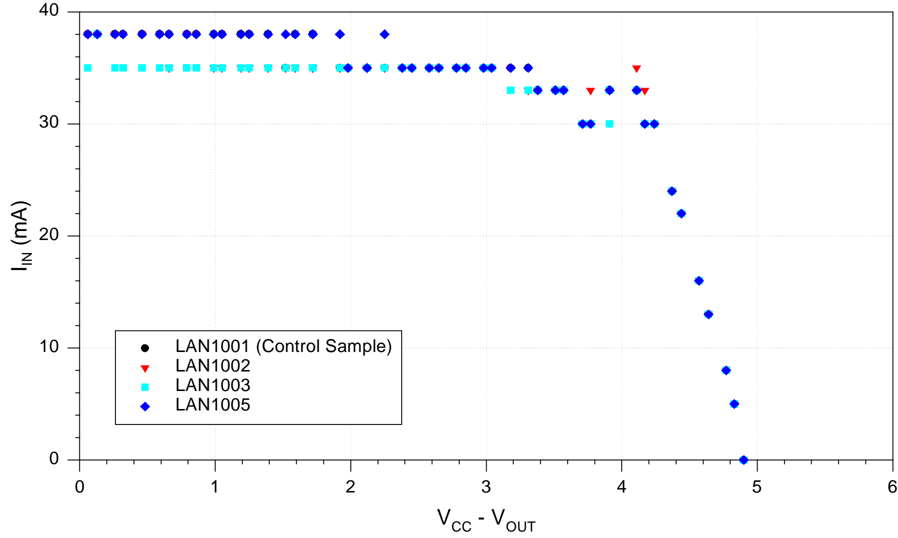

Figure 4. V_{OL} characteristics of testing DUTs after room temperature annealing.

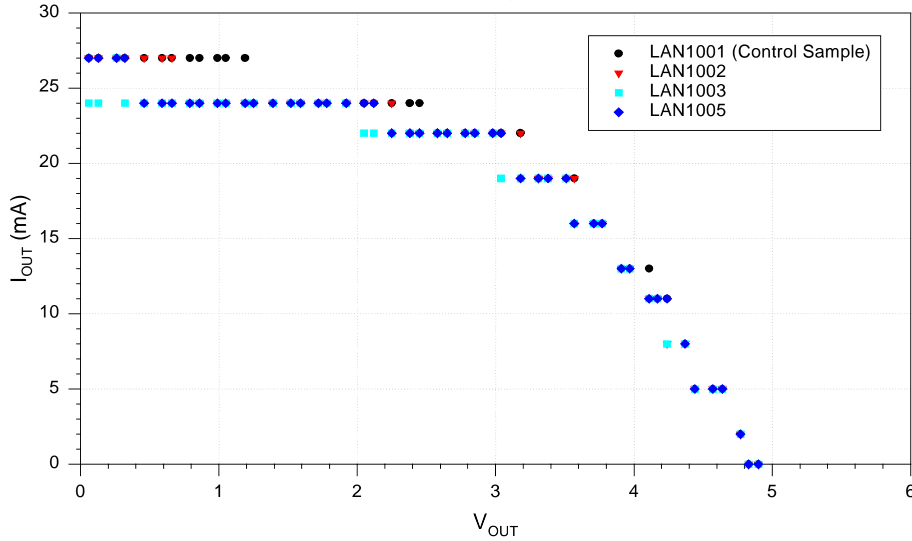

Figure 5. V_{OH} characteristics of testing DUTs after room temperature annealing

3.5 PROPAGATION DELAYS

The testing results of propagation delay are shown in Table 6.

Table 6. Propagation Delays (ns)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN1001	745	747	745
LAN1002	733	735	720
LAN1003	757	764	752
LAN1005	744	741	749

3.6 RISING/FALLING EDGE TRANSIENT

The 12 krad(Si) total dose effects on the rising and falling edge transient characteristics were measured on a D flip-flop. Figures 6-9 show the rising edge of the testing DUTs. Figures 10-13 show the falling edge. No significant radiation effects can be detected in any case.

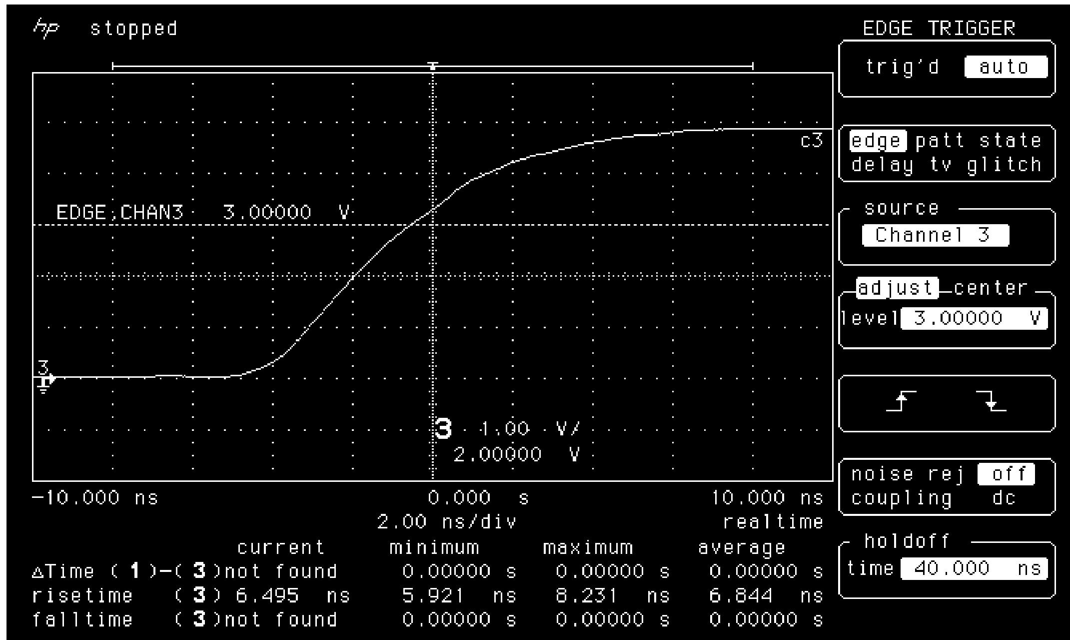

Figure 6a. Rising edge of LAN1001 pre-irradiation

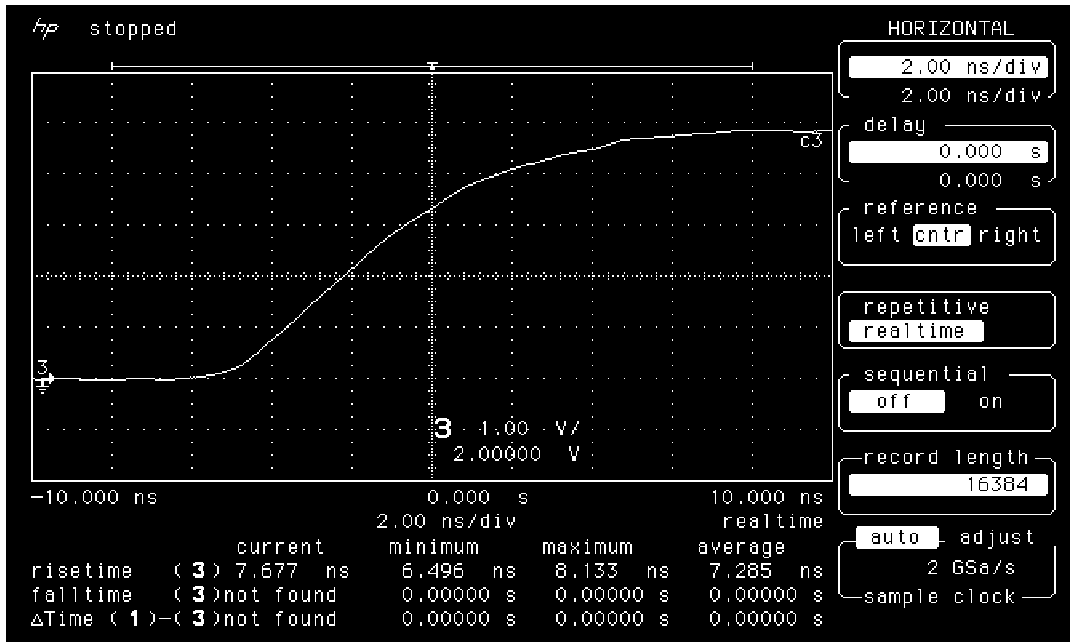

Figure 6b. Rising edge of LAN1001 post-12 krad(Si). Irradiation

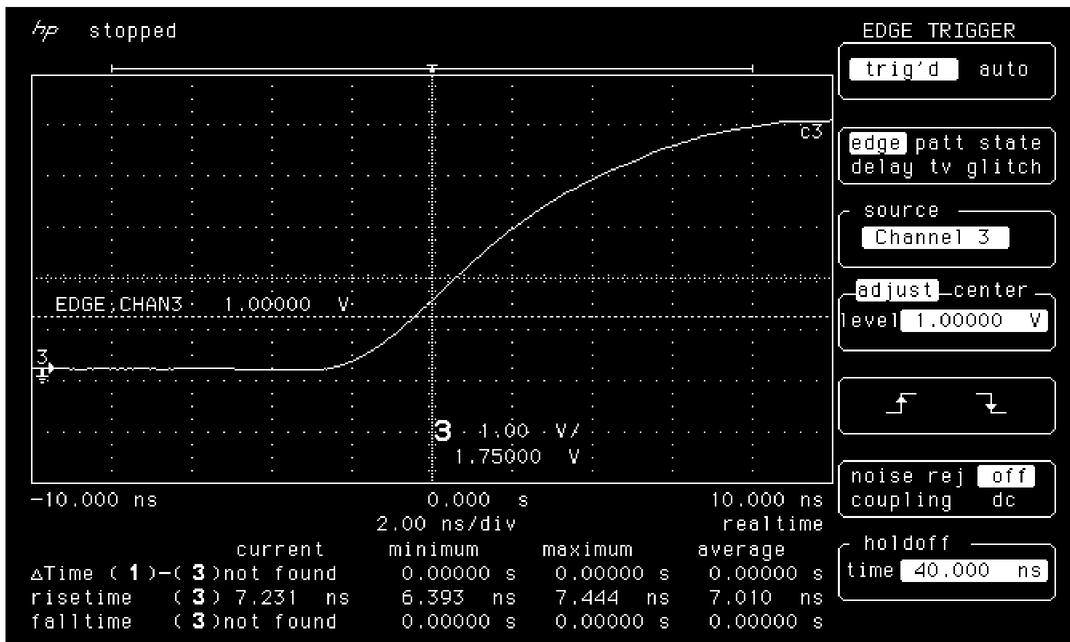

Figure 6c. Rising edge of LAN1001 post-room-temperature-annealing

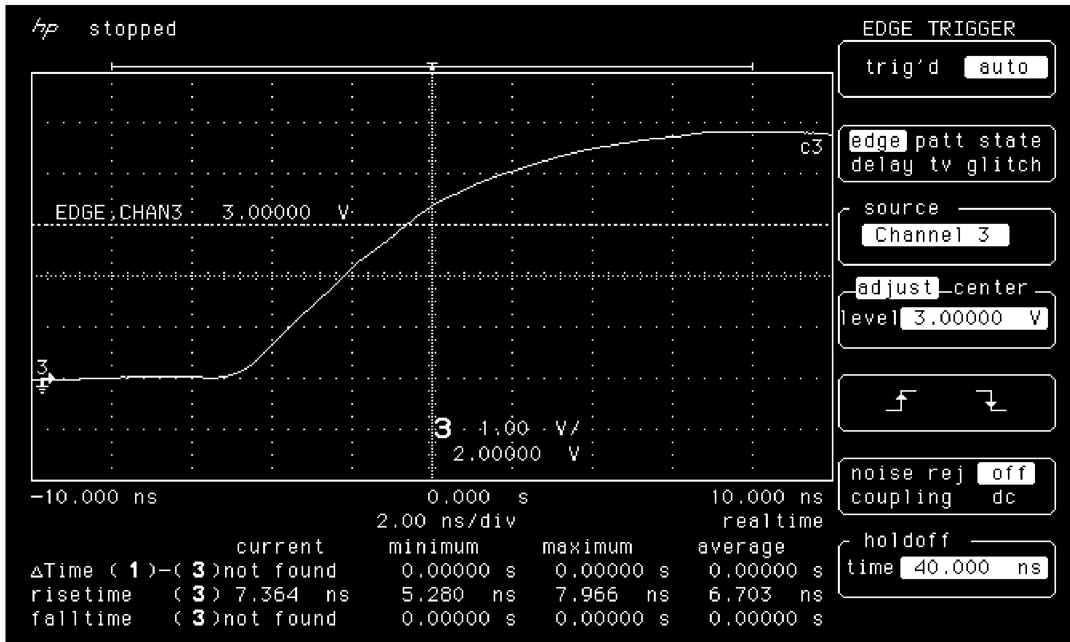

Figure 7a. Rising edge of LAN1002 pre-irradiation

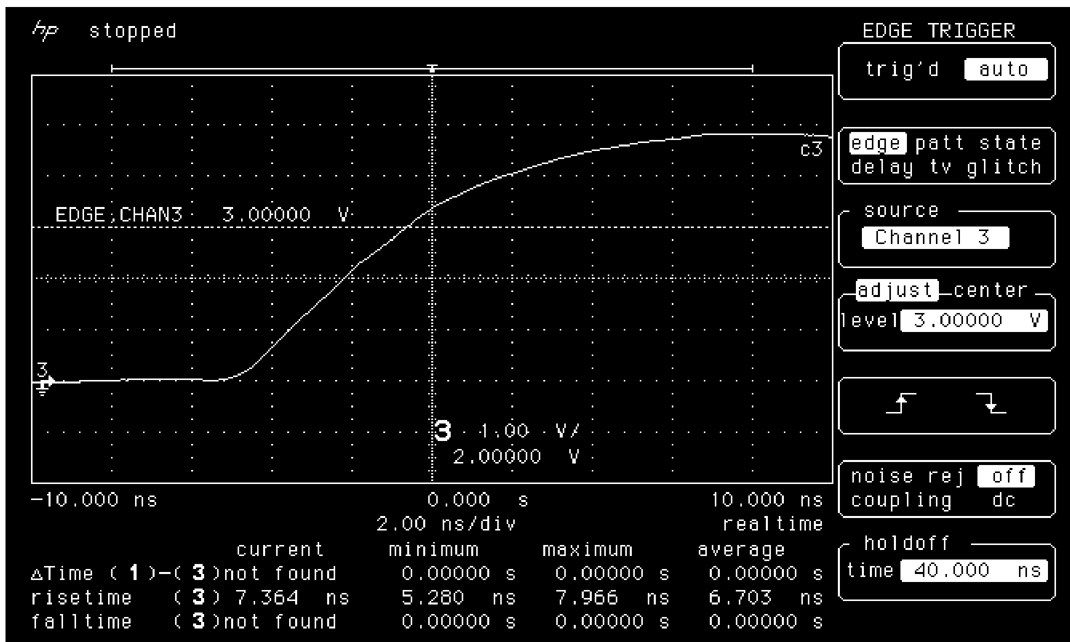

Figure 7b. Rising edge of LAN1002 post-12 krad(Si) irradiation

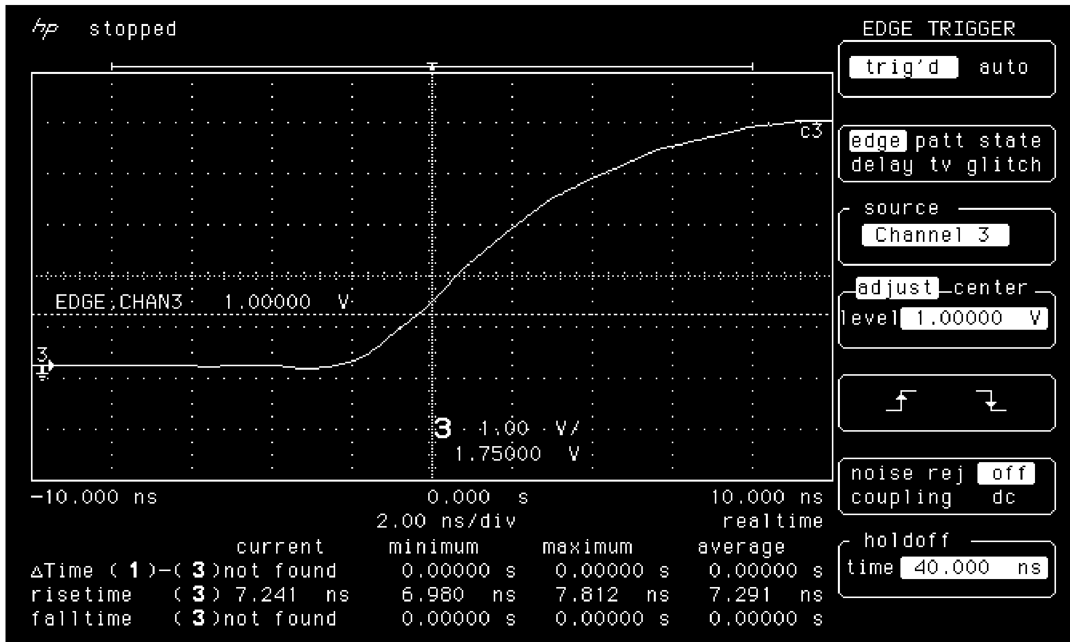

Figure 7c. Rising edge of LAN1002 post-room-temperature annealing

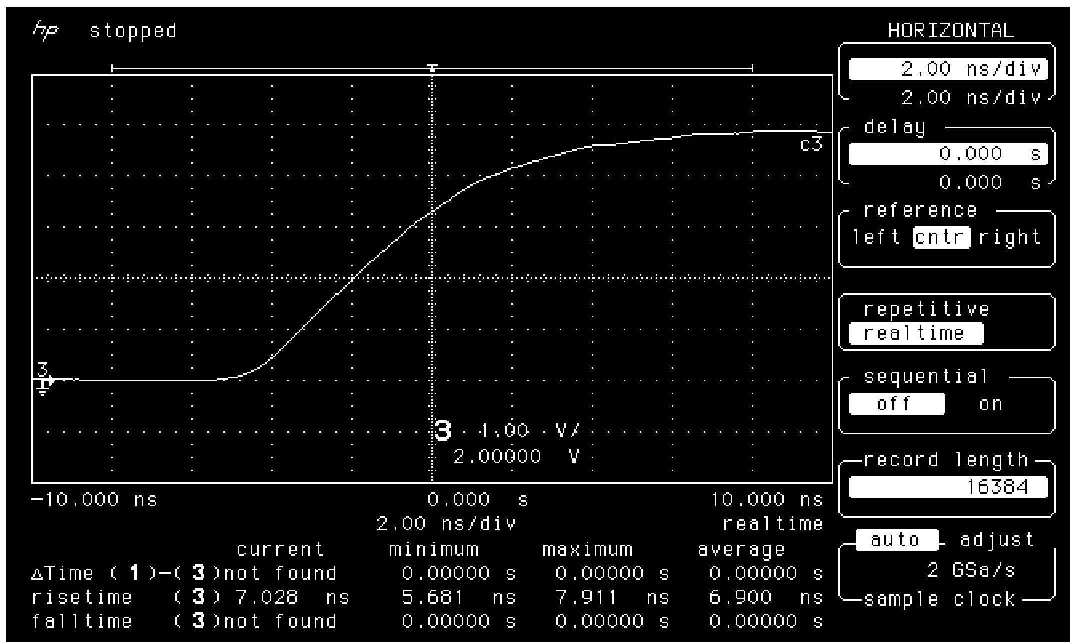

Figure 8a. Rising edge of LAN1003 pre-irradiation

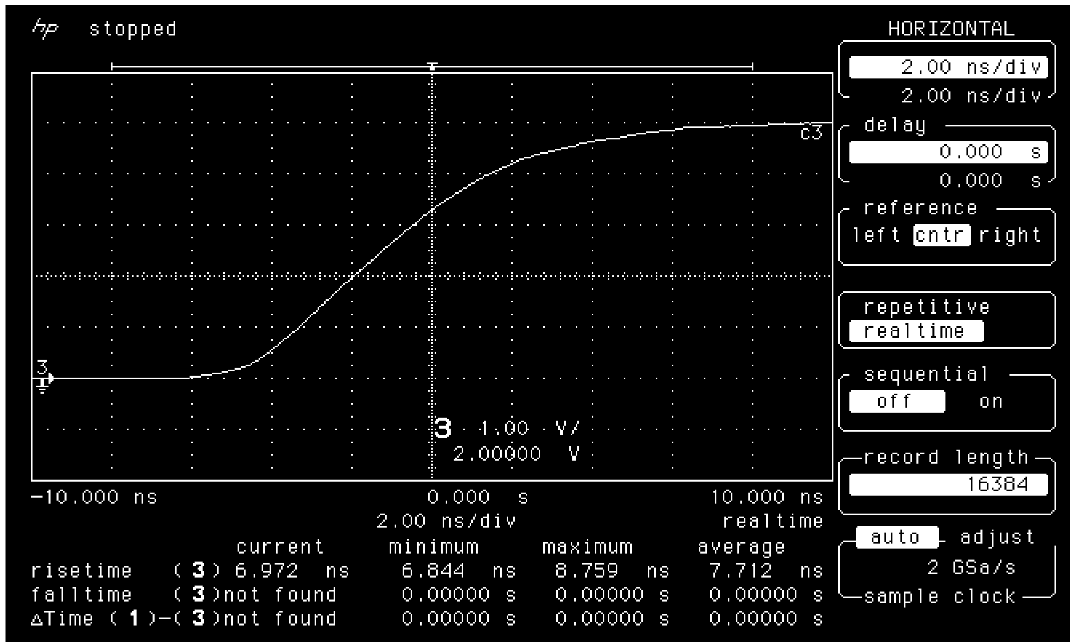

Figure 8b. Rising edge of LAN1003 post-12 krad(Si) irradiation

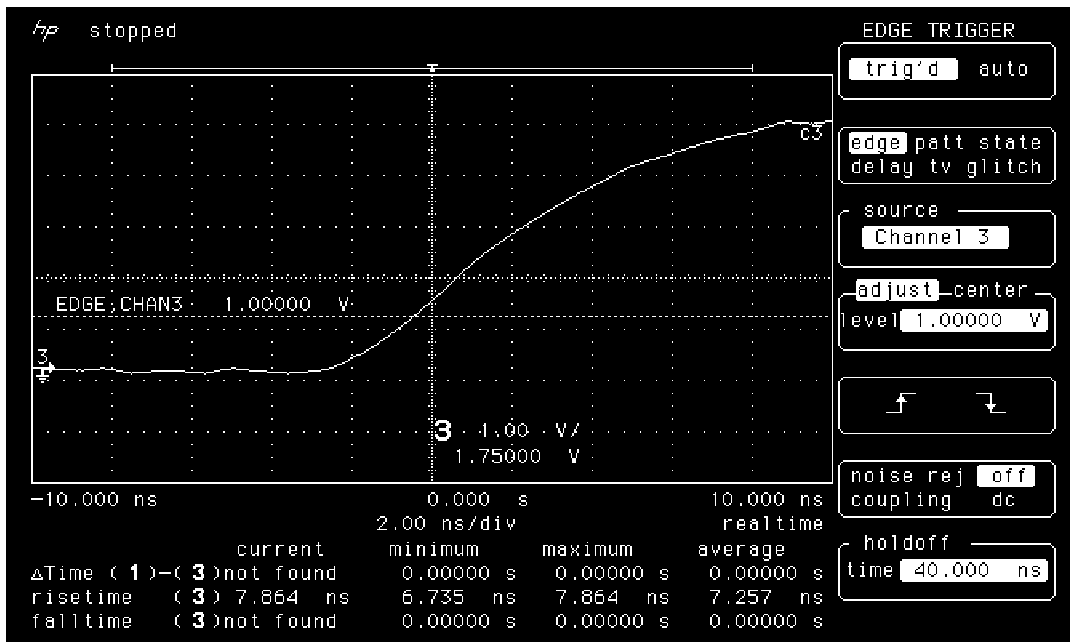

Figure 8c. Rising edge of LAN1003 post-room-temperature annealing

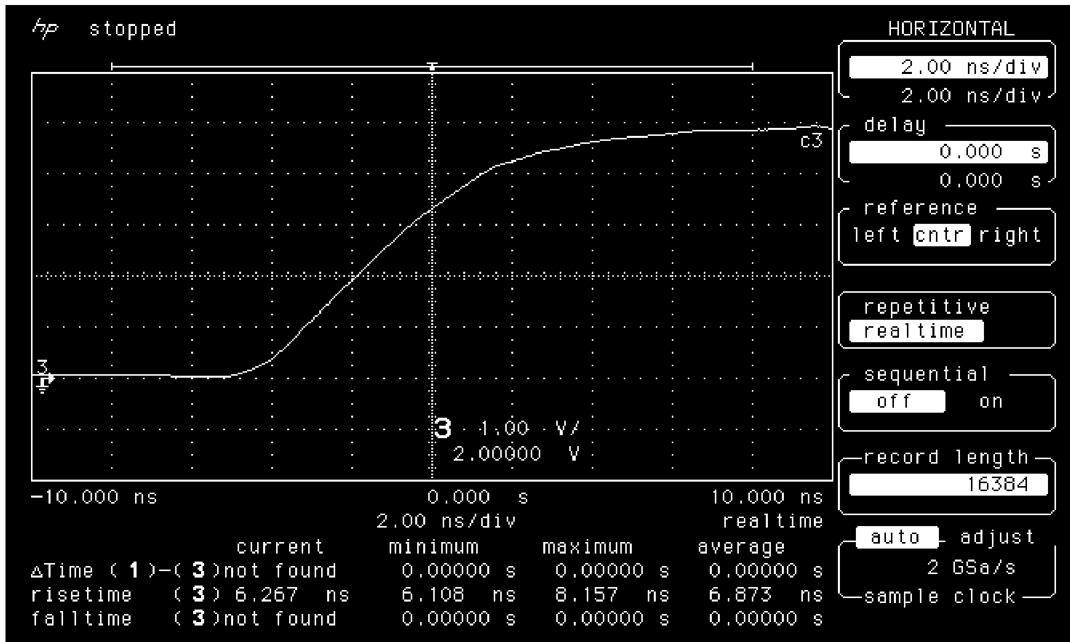

Figure 9a. Rising edge of LAN1005 pre-irradiation

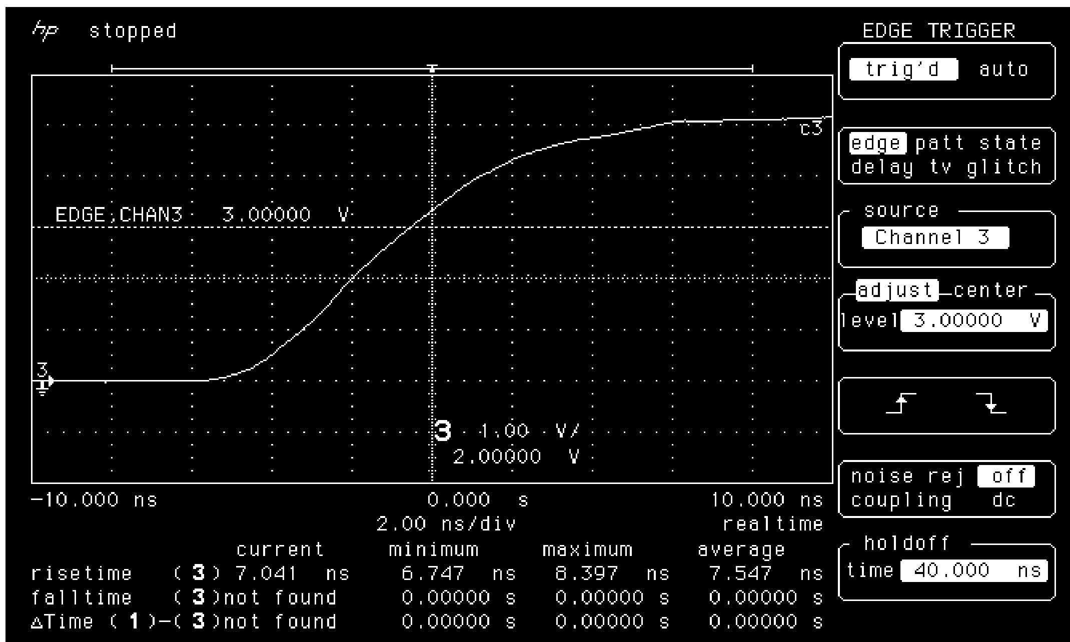

Figure 9b. Rising edge of LAN1005 post-12 krad(Si) irradiation

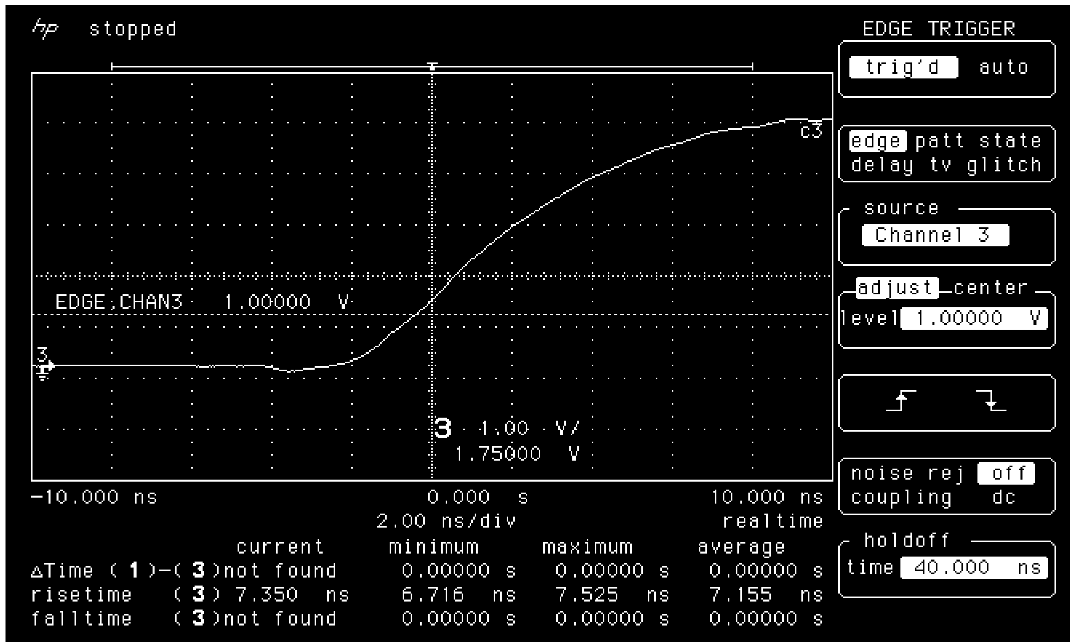

Figure 9c. Rising edge of LAN1005 post-room-temperature annealing

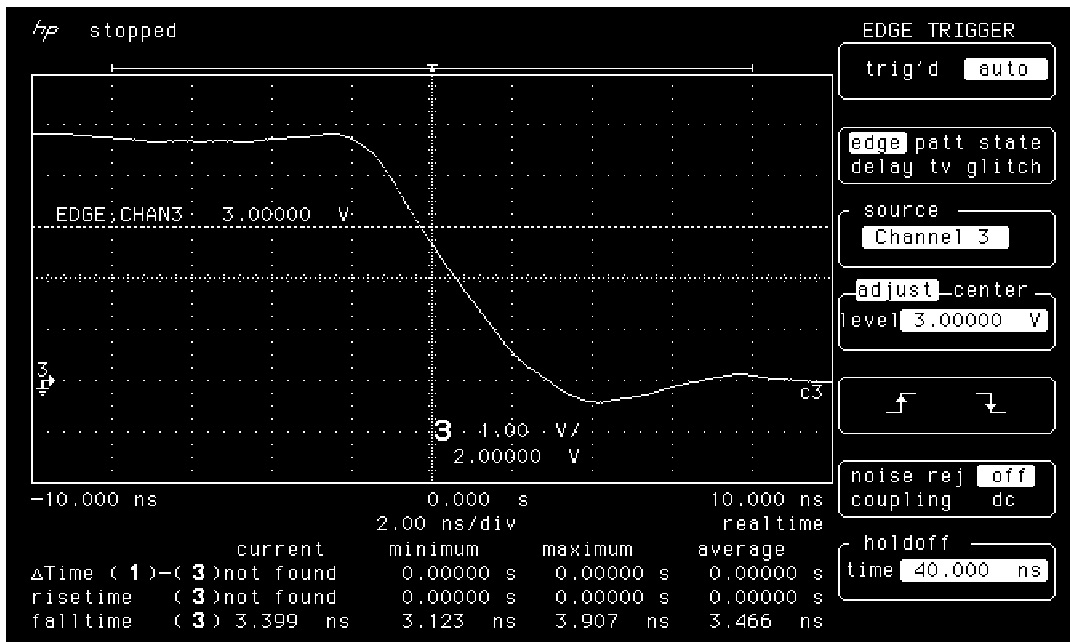

Figure 10a. Falling edge of LAN1001 pre-irradiation.

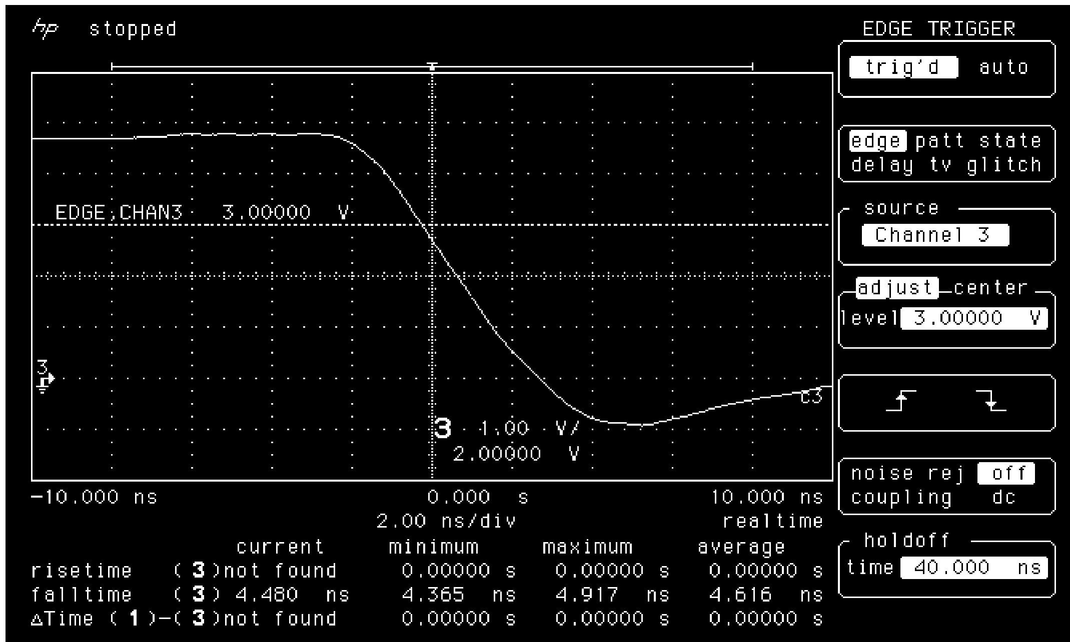

Figure 10b. Falling edge of LAN1001 post-12 krad(Si) irradiation

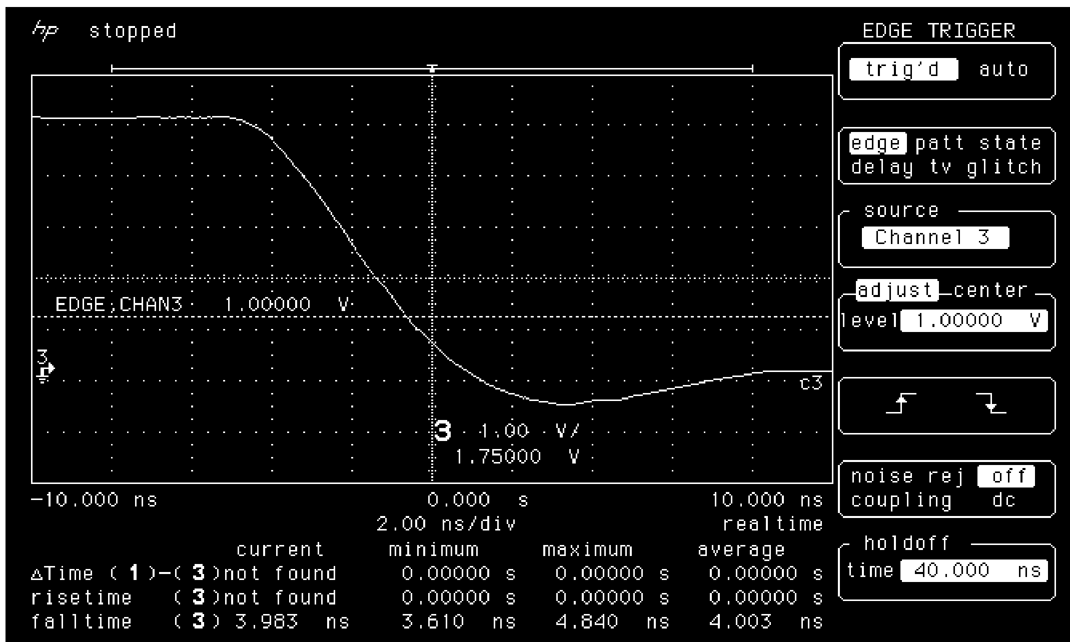

Figure 10c. Falling edge of LAN1001 post room temperature annealing

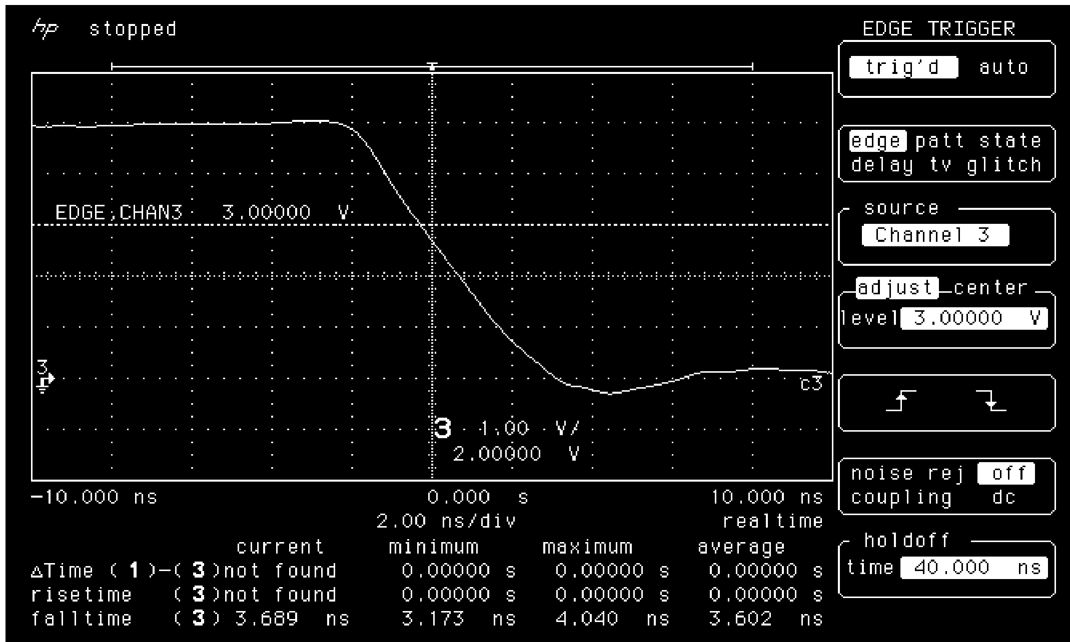

Figure 11a. Falling edge of LAN1002 pre-irradiation.

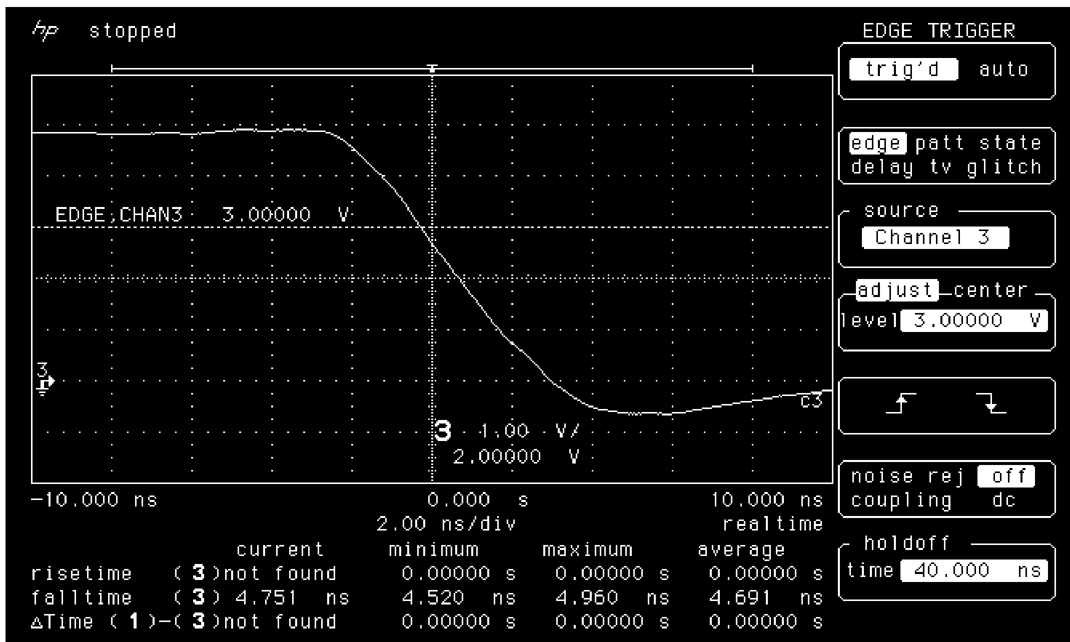

Figure 11b. Falling edge of LAN1002 post-12 krad(Si) irradiation

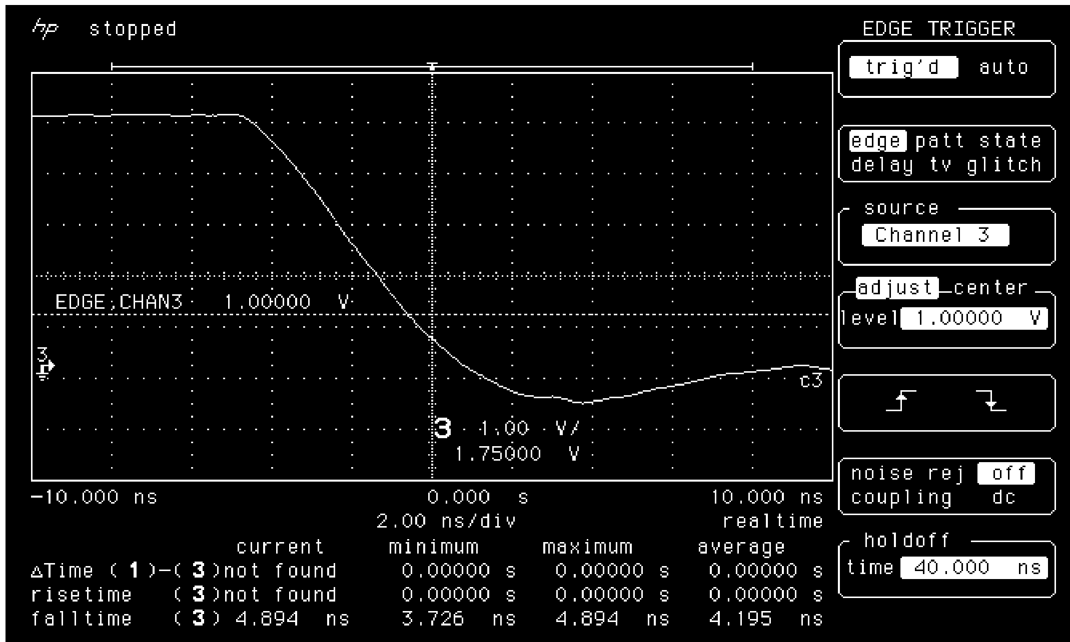

Figure 11c. Falling edge of LAN1002 post room temperature annealing

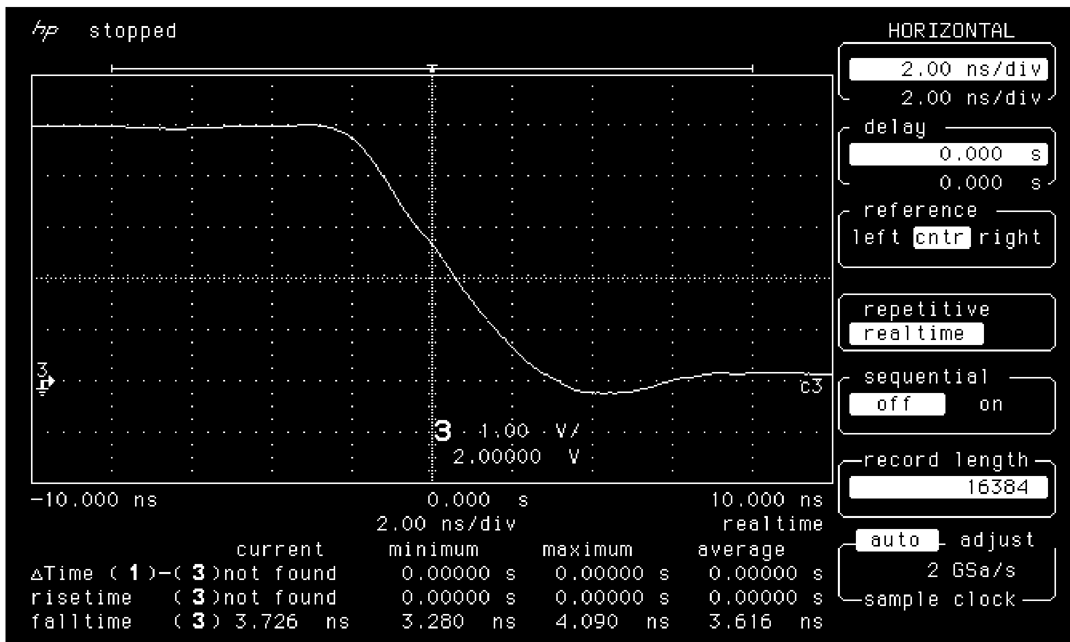

Figure 12a. Falling edge of LAN1003 pre-irradiation

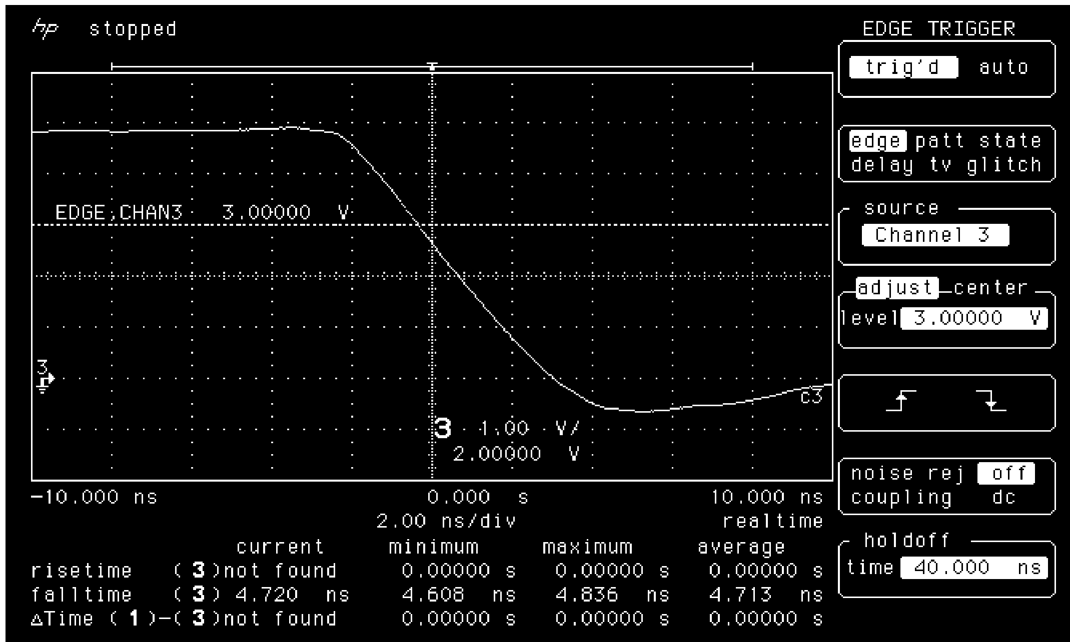

Figure 12b. Falling edge of LAN1003 post-12 krad(Si) irradiation

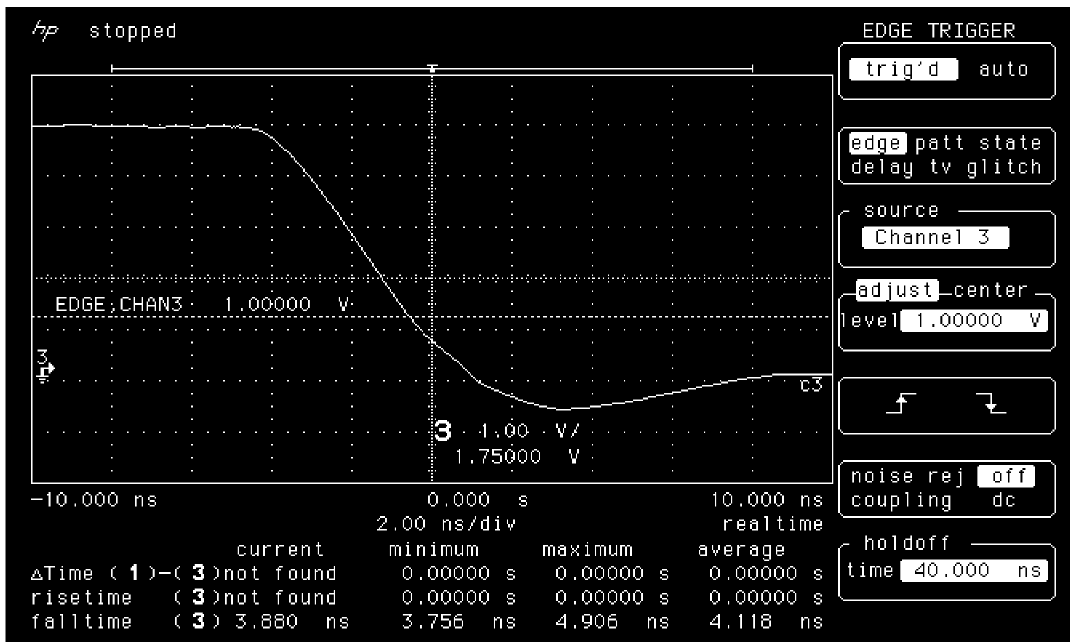

Figure 12c. Falling edge of LAN1003 post room temperature annealing

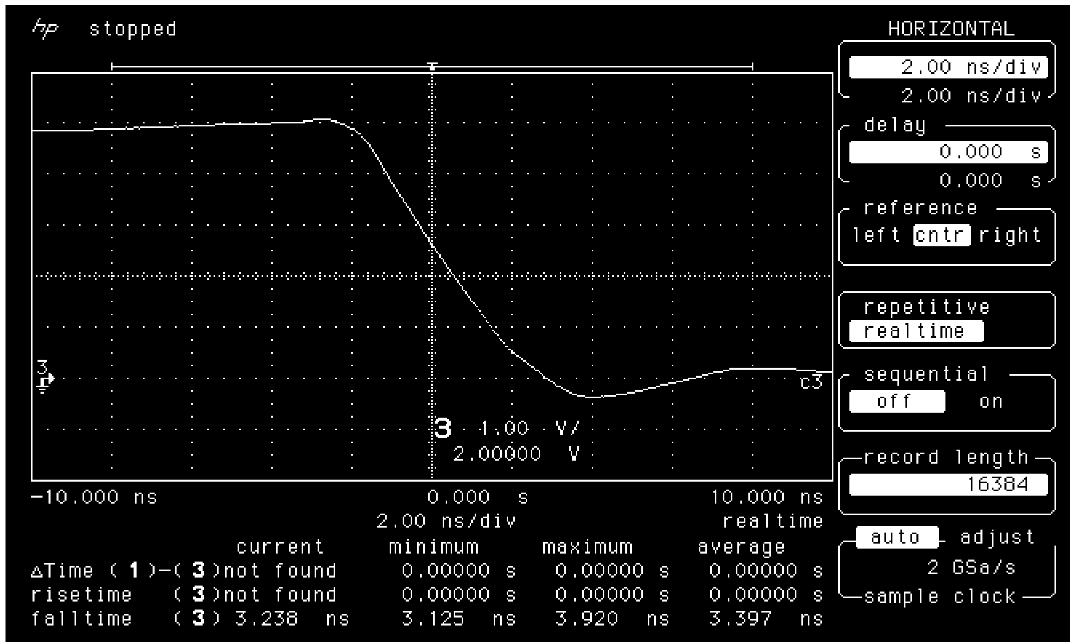

Figure 13a. Falling edge of LAN1005 pre-irradiation

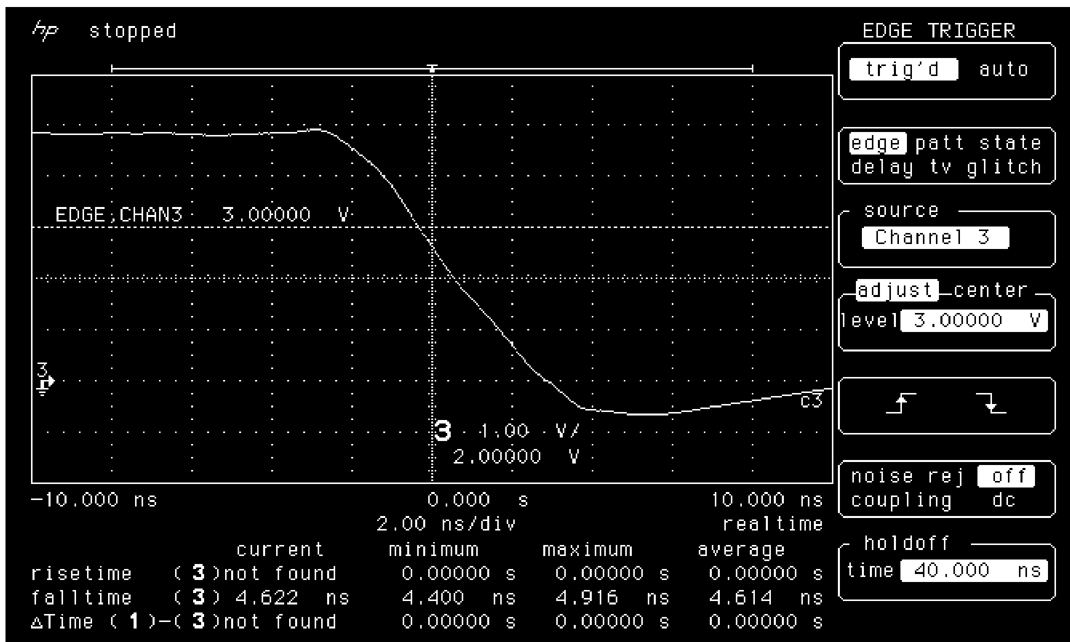

Figure 13b. Falling edge of LAN1005 post-12 krad(Si) irradiation

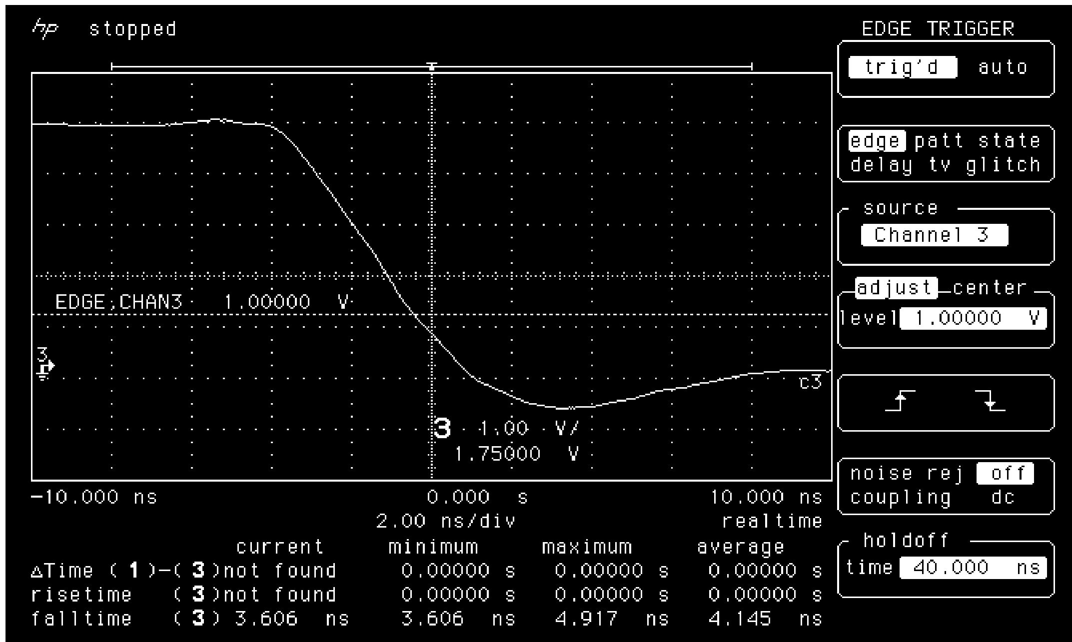

Figure 13c. Falling edge of LAN1005 post room temperature annealing