Sept. 28, 1998

TOTAL IONIZATION DOSE TEST REPORT

No. 98-RT1425-3
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1.0 SUMMARY TABLE

Parametrics/Characteristics	Results
1. Functionality	Functional up to 40 krad(Si) (Figure 2)
2. $I_{DDSTDBY}$	~ 20 mA after ~30 krad(Si) (Figure 2), <4 mA after 23 krad(Si) + 168 hrs room temp anneal (Figure 3, 4)
3. V_{IL}/V_{IH}	Negligible change for 23 krad(Si) (Table 5)
4. V_{OL}/V_{OH}	Negligible change for 23 krad(Si) (Figures 5-14)
5. Propagation Delays	Negligible change for 23 krad(Si) (Table 6, 7)
6. Start-up Transient	Negligible change for 23 krad(Si) (Figures 15-24)
7. Rising/Falling Edge Transient	Negligible change for 23 krad(Si) (Figures 25-34)

2.0 TID TEST

This section describes the device under test (DUT), the testing method, and the irradiation parameters.

2.1 TEST DEVICE

Table 1 lists the DUT information.

Table 1

Part Number	A1425A
Package	PGA
Foundry	MEC
Technology	0.8 um CMOS
Die Lot Number	UCJ014X
Date Code	9819
Quantity Tested	5
Serial Numbers	LAN201 (Control), LAN202, LAN203, LAN204, LAN205

2.2 IRRADIATION

Table 2 lists the irradiation parameters.

Table 2

Facility	NASA
Radiation Source	Co-60
Dose Rate	6 krad(Si)/day (+-10%)
Final Total Dose for DC/AC Parameter Measurement	23 krad(Si)
Temperature	Room
Bias	5 V

2.3 TEST METHOD

The test method is basically a modified TM1019 suitable for space applications. Figure 1 shows its flow. Rebound annealing is omitted in this test flow. So that after post-irradiation testing (step 3) or post-room-temperature-anneal testing (step 5) , the DUTs can be irradiated more until functional failure occurs (step 6). The omission of rebound annealing doesn't affect the integrity of the test because all the previous data showed that Actel's FPGA had no rebound effect (see, for example, the most recent TID Report No. 98-T14100-2). During annealing, the bias is the same as during irradiation.

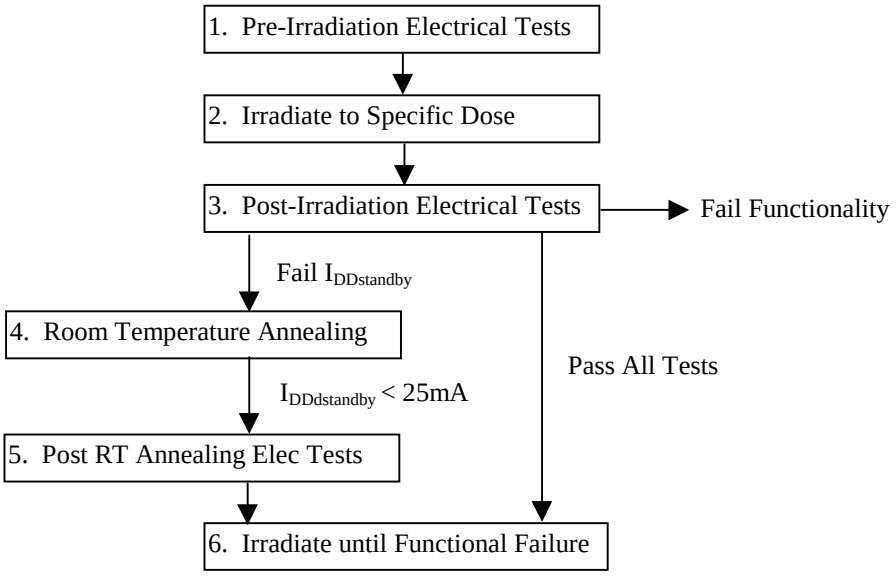

Figure 1. Test Method Flow Chart

2.4 ELECTRICAL PARAMETERS/CHARACTERISTICS TESTS

The electrical parameters/characteristics were measured on bench with relative low noise. The corresponding logic design circuits (referring to Appendix) are listed in Table 3.

Table 3

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power line
3. V_{IL}/V_{IH}	IOPRECLR, monitored on IODIO19
4. V_{OL}/V_{OH} (Output I-V)	OUTX1
5. Propagation Delays	Input = INX1, Output = OUTX1
6. Start-up Transient	DUT power line
7. Rising/Falling Edge	QA0 (D flip-flop output)

3.0 TEST RESULTS

This section presents all the testing results.

3.1 FUNCTIONAL TEST

Table 4 shows the test results matrix.

Table 4. Functionality Test

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN201	passed	passed	passed
LAN202	passed	passed	passed
LAN203	passed	passed	passed
LAN204	passed	passed	passed
LAN205	passed	passed	passed

3.2 IDDSTANDBY AND FINAL FUNCTIONAL FAILURE

$I_{DDstandby}$ was monitored during the irradiation and annealing period. Because the board had a measurable leakage, only the delta I_{DD} due to radiation and/or annealing was recorded. Using delta I_{DD} is quite appropriate since the pre-irradiation value of $I_{DDstandby}$ is only approximately 0.5 mA.

Figure 3 shows the delta $I_{DDstandby}$ curves versus total cumulative dose up to 23 krad(Si). At total dose of 23 krad(Si), the delta $I_{DDstandby}$ of every DUT is close to 10 mA. Based on previous experiences, this is a save point to perform all the electrical tests with low risk of failure.

Although room-temperature annealing to reduce delta $I_{DDstandby}$ is not necessary from the qualification point of view, it was done for the sake of low-power design. Figure 4 shows the room temperature annealing characteristics in which delta $I_{DDstandby}$ dropped to approximately 2 mA after approximately a week's annealing.

After post room temperature annealing tests, all the DUTs were irradiated again until final functional failure occurred. The criterion for that is shown in Figure 2. When delta $I_{DDstandby}$ starts to increase drastically to over 100 mA, it indicates the initiation of the charge pump failure ["Antifuse FPGA for Space Applications" by J. Wang et al, 1997 RADECS Conference Workshop, p.11-p.16] and also the subsequent device functional failure. Before that happens, the device is always functional. Based on this criterion, Figure 2 shows the functional failure won't happen before 40 krad(Si).

3.3 INPUT LOGIC THRESHOLD

The input logic threshold (V_{IH}/V_{IL}) is tabulated in Table 5. The equipment limited the resolution to be only 0.1 V, which rendered the difference between V_{IH} and V_{IL} within the noise.

Table 5. Input Logic Threshold Voltage (V)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN201	1.48	1.48	1.48
LAN202	1.46	1.43	1.45
LAN203	1.47	1.45	1.45
LAN204	1.49	1.43	1.45
LAN205	1.50	1.42	1.45

3.4 OUTPUT I-V CHARACTERISTICS

Figures 5 to 14 display the radiation effects on output characteristics (I-V curves).

3.5 PROPAGATION DELAYS

Rising and falling edge delays are shown in Table 6 and 7 respectively.

Table 6. Rising Edge Propagation Delays (ns)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN201	247.9	246.9	246.9
LAN202	249.0	255.9	256.0
LAN203	250.2	258.6	257.3
LAN204	246.5	254.3	253.6
LAN205	251.4	259.4	258.8

Table 7. Falling Edge Propagation Delays (ns)

	Pre-Irradiation	Post-Irradiation	RT Anneal
LAN201	255.9	254.2	254.3
LAN202	255.8	268.5	266.1
LAN203	257.2	270.2	267.5
LAN204	254.2	266.9	264.6
LAN205	258.4	271.3	268.8

3.6 STARTUP CURRENT TRANSIENT

The TID effect on startup current transient in Actel's FPGA was sometimes considered as a potential problem for spacecraft designers ["Total Dose Responses of Actel 1020B and 1280A Field Programmable Gate Arrays" by R. Katz et al, RADECS 95, p.412-p.419]. The recent study by NASA/GSFC and Actel showed strong dose rate dependence on this effect. Using dose rate much higher than space may draw an over-conservative conclusion about this particular characteristic. The recommendation is that if this is the limiting characteristic for the total dose tolerance, the post radiation room temperature annealing characteristic should be measured carefully. Since it's impractical to use the same dose rate as the real space environment, room temperature annealing after irradiation is always necessary.

The oscilloscope plots of startup current transient are shown in Figure 15 to 24. All the pictures in each Figure are the same measurement for the same part and arranged in the order of, from top, pre-irradiation, post-irradiation, and post room temperature annealing. C1 is the voltage with the scale of 1 volt/division and C2 the current with 100 mA/division. The overviews using time scale of 500 us/division show voltage and current glitches at about C1 = 3 V. The close-ups using time scale of 1 us/division show the details of the glitches. No significant radiation effect can be detected in any case for total dose of 23 krad(Si).

3.7 RISING/FALLING EDGE TRANSIENT

The TID effects on the rising and falling edge transient characteristics were also measured on a D flip-flop (QA0 in page 2 of Appendix). Figure 25 to 29 show oscilloscope pictures of the rising edge, and Figure 30 to 34 show the falling edge. The arrangement of pictures is the same as those in the last section. No significant radiation effects can be detected in any case for total dose of 23 krad(Si).

APPENDIX A: TEST PATTERN SCHEMATICS