Total Ionizing Dose Test Report

No. 13T-RTSX72SU-CQ256-D1SLL1

March 27, 2013

Microsemi

Table of Contents

I. **Summary Table** 3

II. **Total Ionizing Dose (TID) Testing** 3

- A. Device-Under-Test (DUT) and Irradiation Parameters 3
- B. Test Method 4
- C. Design and Parametric Measurements 5

III. **Test Results** 6

- A. Functionality 6
- B. Power Supply Current (ICCA and ICCI) 6
- C. Input Logic Threshold (VIL/VIH) 7
- D. Output-Drive Voltage (VOL/VOH) 9
- E. Propagation Delay 10
- F. Transition Characteristics 11

Appendix A: DUT Bias 23

Appendix B: DUT Design Schematics 25

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 60 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 100 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO_2)
5. Propagation Delay	Passed 100 krad (SiO_2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D1SLL1
Quantity Tested	6
Serial Number	100 krad(SiO_2): 17896, 17899, 17912 60 krad(SiO_2): 17976, 17989, 18005
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

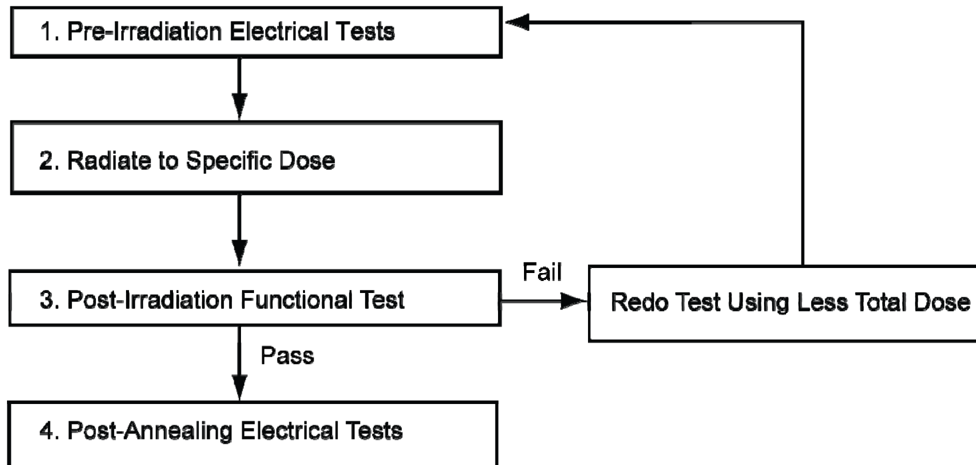

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 4 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin CLOCK to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation and post-annealing ICCA and ICCI data.

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in this test is defined as the highest ICCA/ICCI in the RTSXSU spec sheet of 25 mA.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)		ICCI (mA)	
		Pre-irrad	Post-ann	Pre-irrad	Post-ann
17896	100 krad	1.31	103	0.72	94
17899	100 krad	1.36	80	0.72	89
17912	100 krad	1.27	93	0.73	147
17976	60 krad	1.33	14	0.70	15
17989	60 krad	1.29	16	0.70	23
18005	60 krad	1.28	15	0.70	21

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds. All data are within the specification limits. The post-annealing shift in every case is very small.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	17896 (100 krad)				17899 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1140	1165	1495	1465	1125	1225	1550	1475
DAH/QA0H	1415	1425	1415	1425	1415	1455	1440	1440
ENCNTRH/YO0H	1380	1385	1425	1440	1370	1385	1450	1435
IDII0/IDIO0	1490	1440	1425	1460	1500	1390	1445	1455
IDII1/IDIO1	1270	1365	1405	1425	1470	1230	1405	1405
IDII2/IDIO2	1490	1385	1420	1410	1395	1460	1425	1390
IDII3/IDIO3	1430	1390	1380	1350	1445	1415	1380	1410
IDII4/IDIO4	1240	1335	1400	1390	1355	1285	1435	1430
IDII5/IDIO5	1430	1370	1400	1380	1425	1415	1395	1390
IDII6/IDIO6	1405	1385	1490	1490	1435	1455	1410	1500
IDII7/IDIO7	1425	1390	1405	1395	1425	1430	1415	1415

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	17912 (100 krad)				17976 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1150	1225	1505	1465	1130	1240	1540	1455
DAH/QA0H	1480	1460	1450	1445	1440	1460	1425	1425
ENCNTRH/YO0H	1370	1385	1435	1435	1450	1450	1410	1415
IDII0/IDIO0	1500	1480	1430	1450	1495	1385	1460	1410
IDII1/IDIO1	1375	1275	1450	1445	1240	1240	1410	1455
IDII2/IDIO2	1400	1455	1425	1390	1405	1470	1420	1405
IDII3/IDIO3	1445	1395	1385	1390	1455	1290	1390	1375
IDII4/IDIO4	1320	1285	1430	1425	1355	1285	1430	1570
IDII5/IDIO5	1405	1415	1405	1375	1405	1415	1390	1385
IDII6/IDIO6	1405	1425	1450	1400	1405	1425	1505	1395
IDII7/IDIO7	1450	1395	1440	1410	1440	1405	1420	1390

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	17989 (60 krad)				18005 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1125	1225	1545	1445	1125	1240	1565	1455
DAH/QA0H	1410	1450	1420	1420	1425	1455	1455	1430
ENCNTRH/YO0H	1380	1440	1440	1435	1455	1385	1410	1400
IDII0/IDIO0	1410	1440	1420	1410	1410	1390	1455	1450
IDII1/IDIO1	1370	1220	1395	1430	1290	1305	1400	1445
IDII2/IDIO2	1390	1470	1415	1400	1390	1465	1415	1395
IDII3/IDIO3	1445	1425	1385	1375	1440	1420	1415	1365
IDII4/IDIO4	1320	1260	1435	1570	1335	1295	1430	1575
IDII5/IDIO5	1385	1350	1415	1380	1420	1360	1430	1385
IDII6/IDIO6	1455	1430	1495	1395	1445	1430	1485	1390
IDII7/IDIO7	1425	1385	1405	1385	1435	1400	1425	1400

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	17896 (100 krad)		17899 (100 krad)		17912 (100 krad)		17976 (60 krad)		17989 (60 krad)		18005 (60 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	10	10	10	10	10	10	10	10	10	10	10	10
12 mA	115	115	115	114	114	114	115	115	113	112	115	114
20 mA	192	191	190	190	190	189	192	191	188	187	190	190
50 mA	483	479	479	477	478	476	482	480	473	470	479	476
100 mA	989	982	982	977	980	976	989	984	970	964	981	975

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	17896 (100 krad)		17899 (100 krad)		17912 (100 krad)		17976 (60 krad)		17989 (60 krad)		18005 (60 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4979	4975	4979	4975	4979	4976	4978	4978	4978	4977	4979	4978
8 mA	4850	4846	4850	4845	4851	4846	4850	4848	4849	4847	4849	4847
20 mA	4624	4617	4622	4615	4625	4619	4623	4620	4620	4617	4619	4617
50 mA	4011	3997	4006	3991	4017	4003	4010	4004	3999	3994	3998	3993
100 mA	2628	2567	2595	2529	2644	2581	2627	2599	2559	2535	2567	2543

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Annealing (µs)	Degradation (%)
17896	100 krad	1.43	1.44	0.70%
17899	100 krad	1.48	1.50	1.35%
17912	100 krad	1.49	1.50	0.67%
17976	60 krad	1.45	1.41	-3.10%
17989	60 krad	1.48	1.45	-2.03%
18005	60 krad	1.48	1.43	-3.05%

F. Transition Characteristics

Figure 2a to Figure 13b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

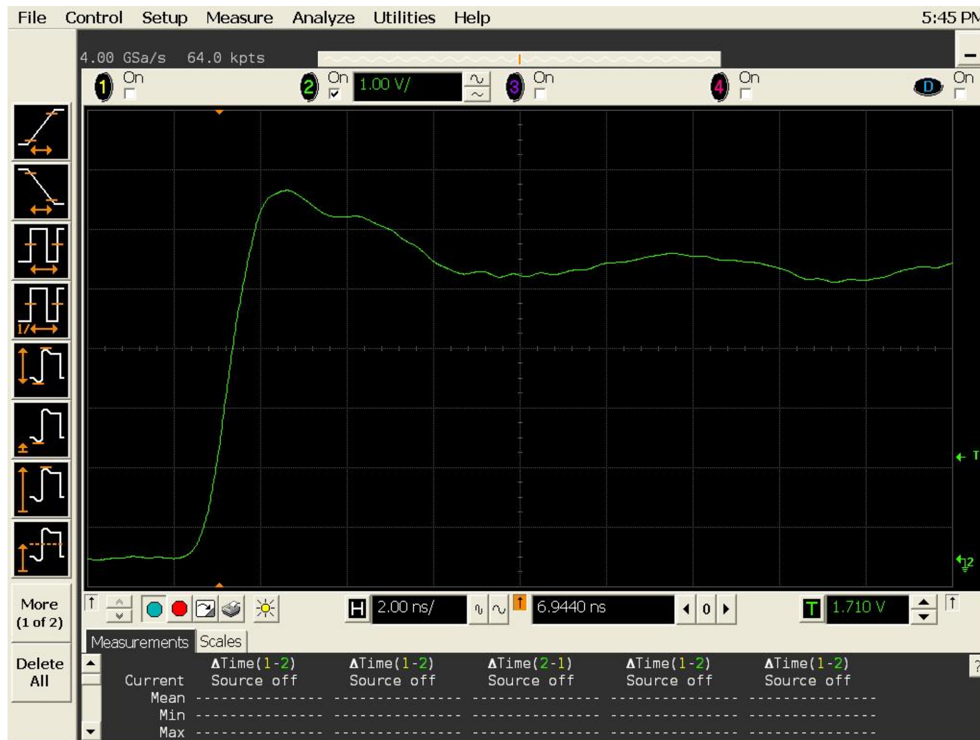

Figure 2a DUT 17896 Pre-Irradiation Rising Edge

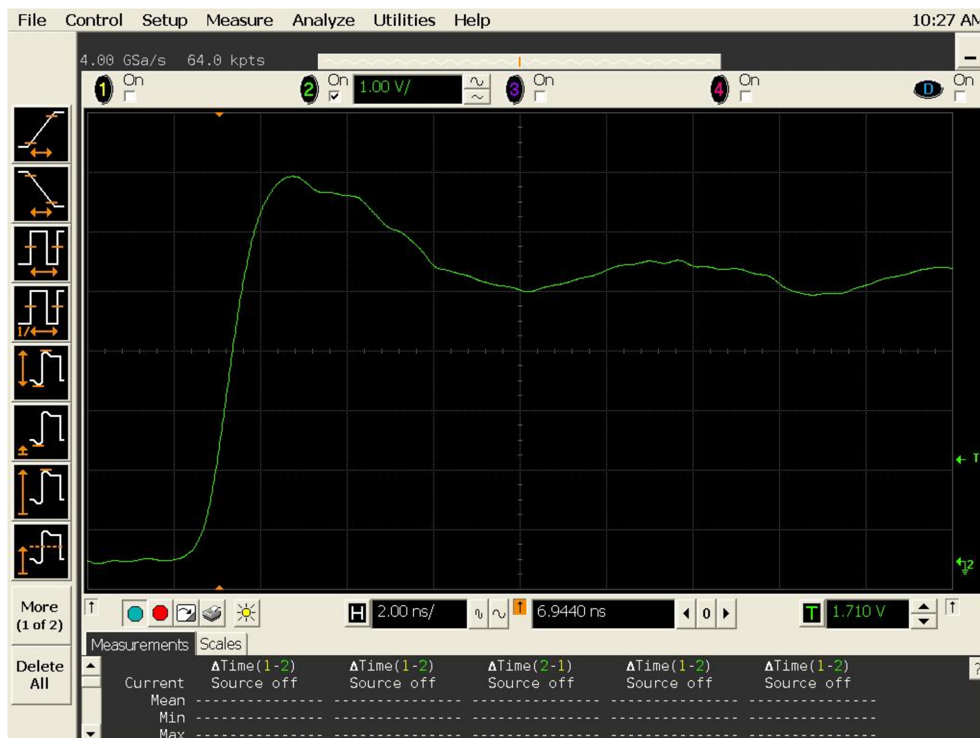

Figure 2b DUT 17896 Post-Annealing Rising Edge

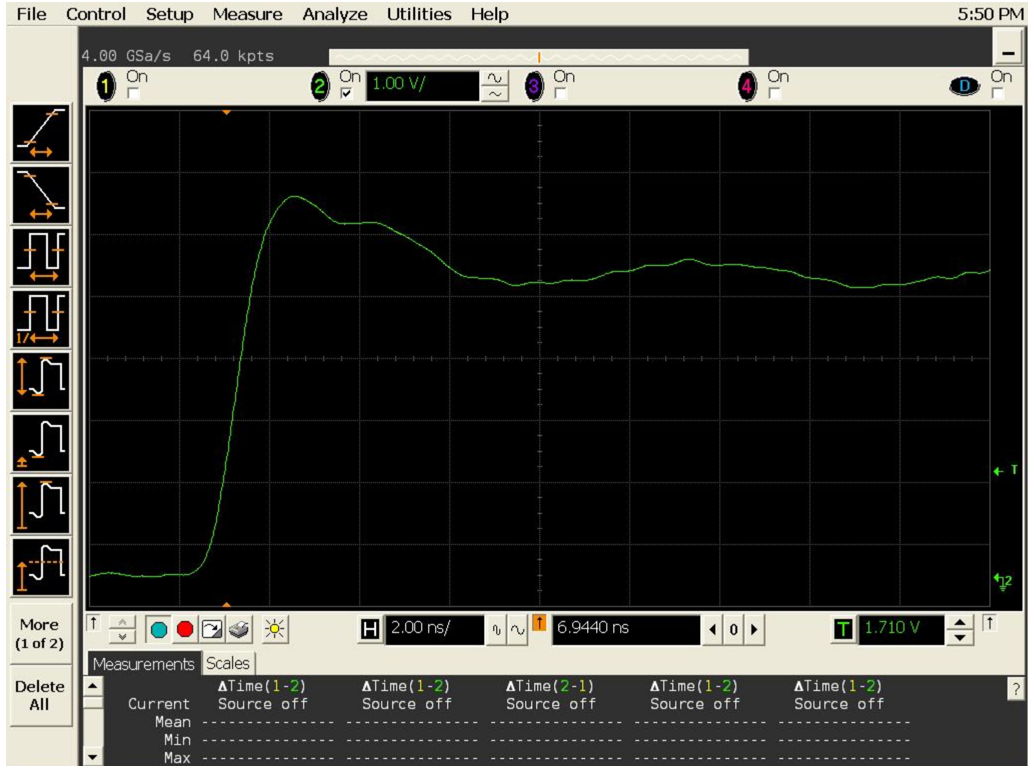

Figure 3a DUT 17899 Pre-Irradiation Rising Edge

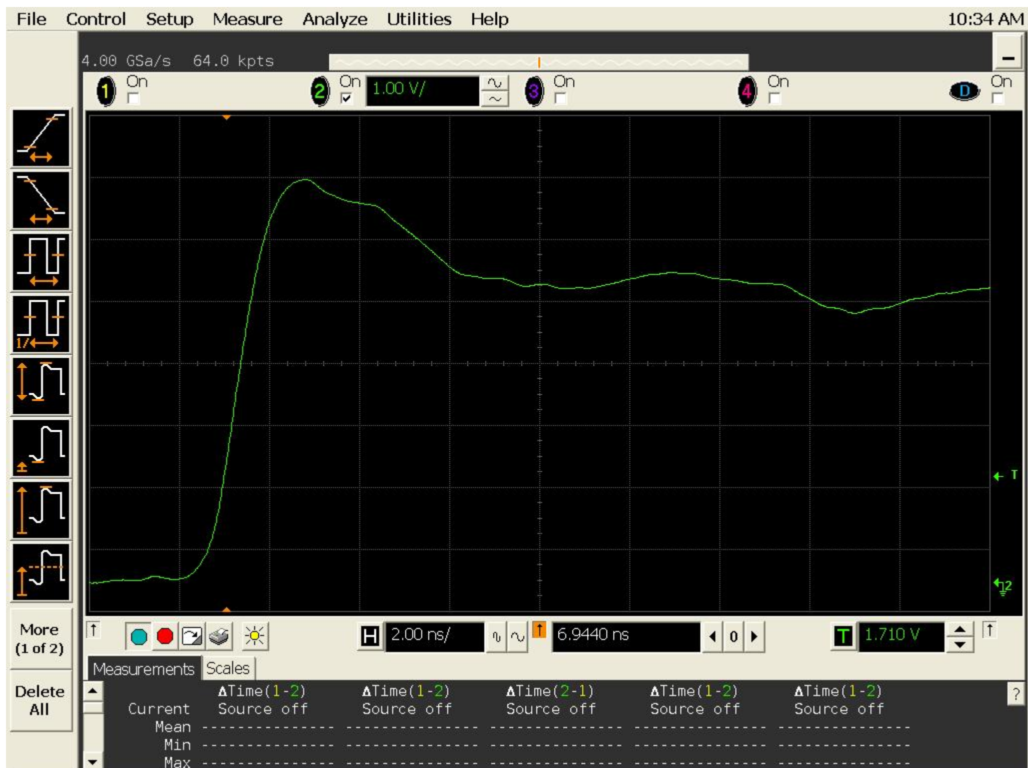

Figure 3b DUT 17899 Post-Annealing Rising Edge

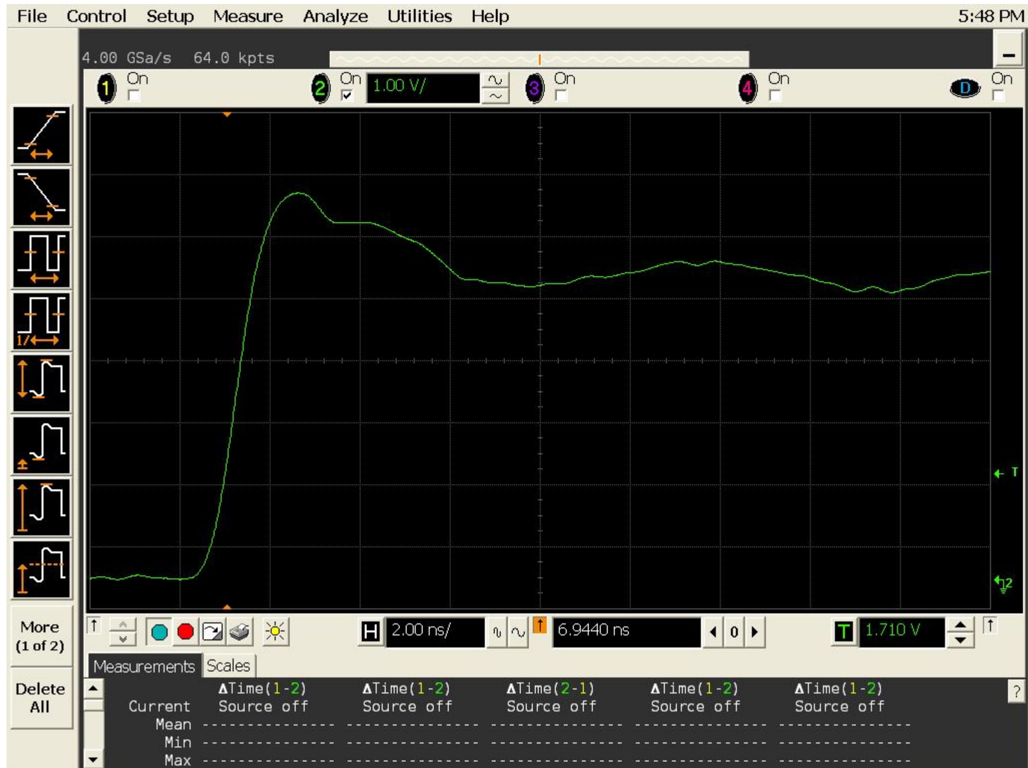

Figure 4a DUT 17912 Pre-Radiation Rising Edge

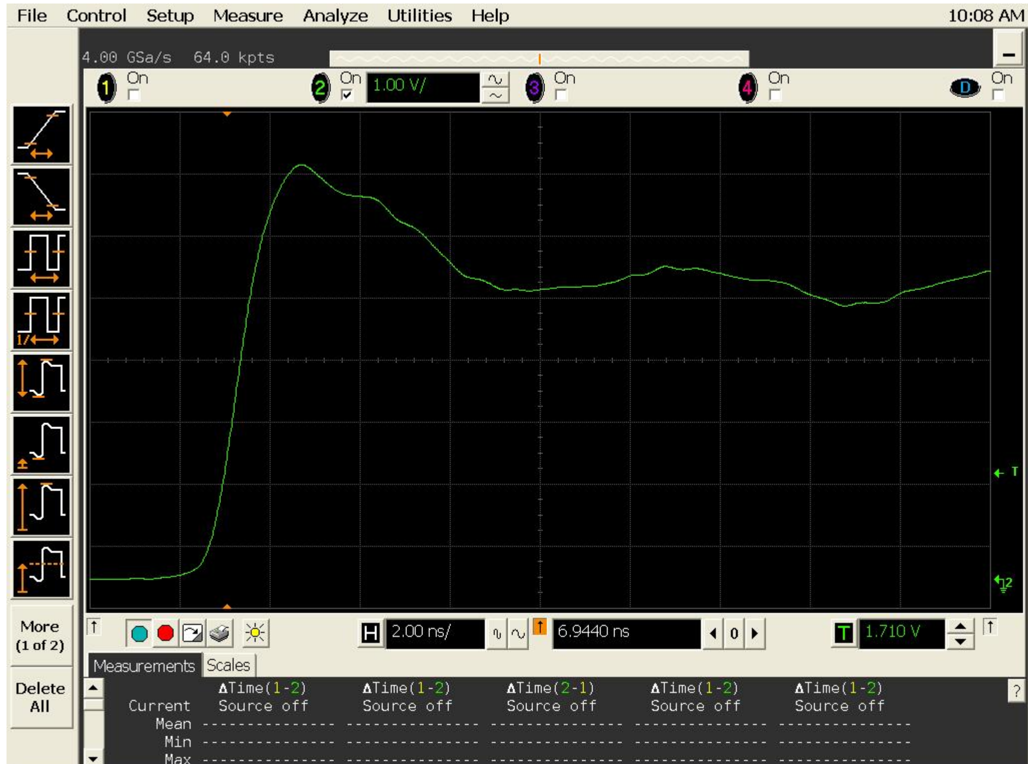

Figure 4b DUT 17912 Post-Annealing Rising edge

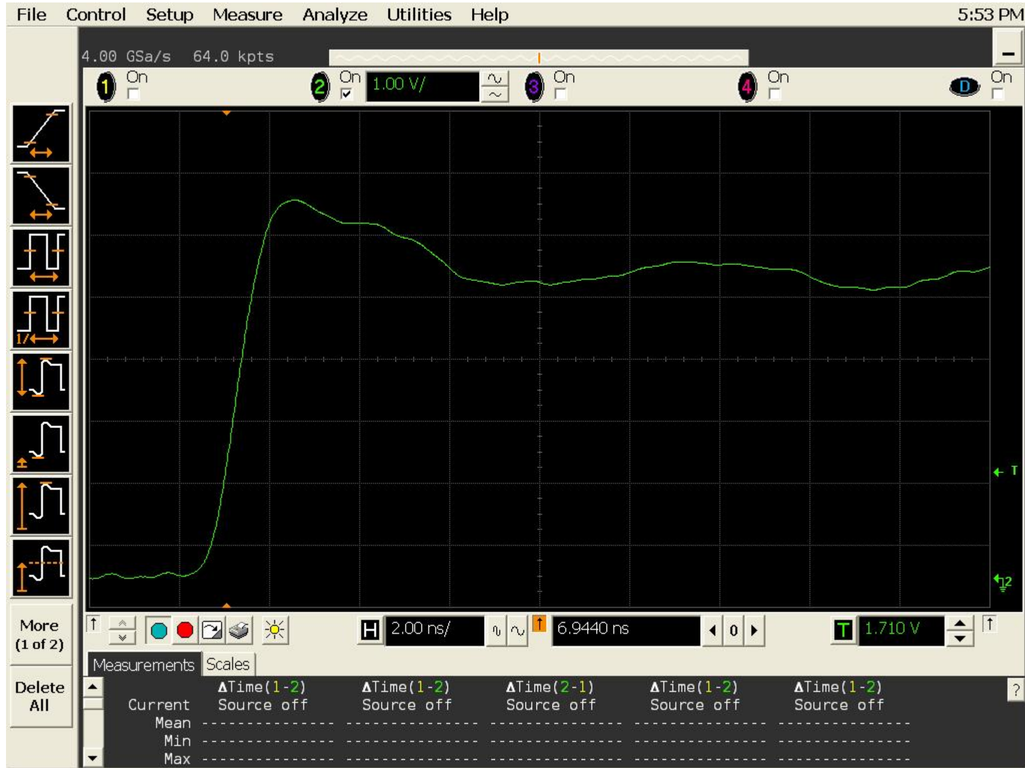

Figure 5a DUT 17976 Pre-Irradiation Rising Edge

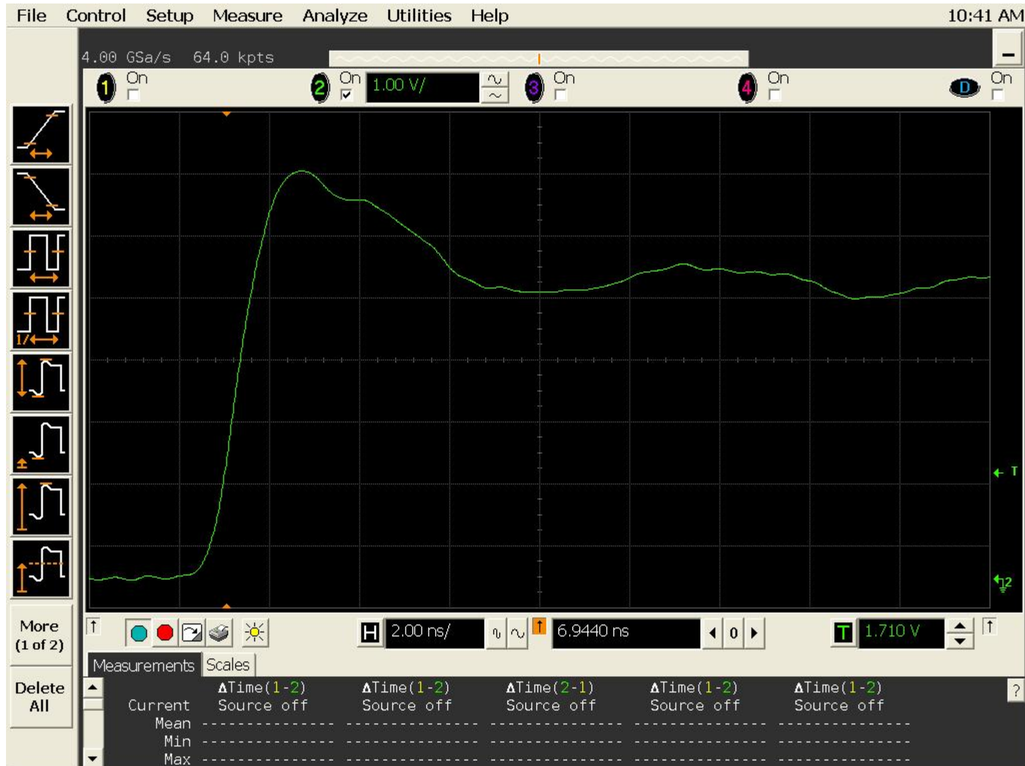

Figure 5b DUT 17976 Post-Annealing Rising Edge

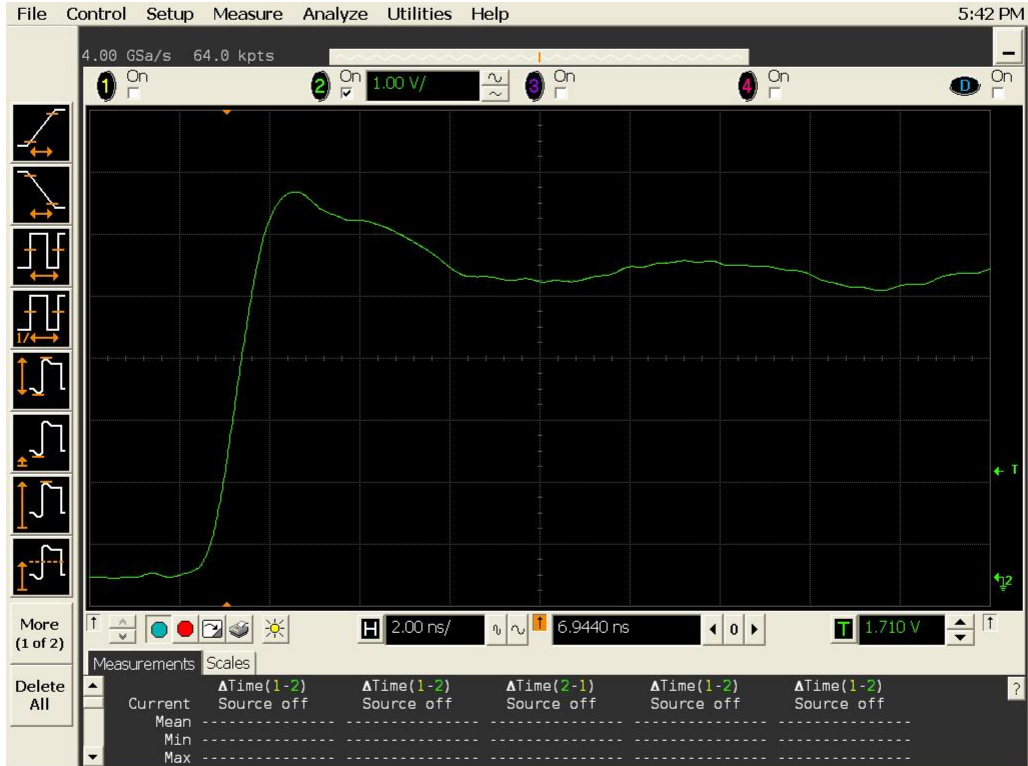

Figure 6a DUT 17989 Pre-Irradiation Rising Edge

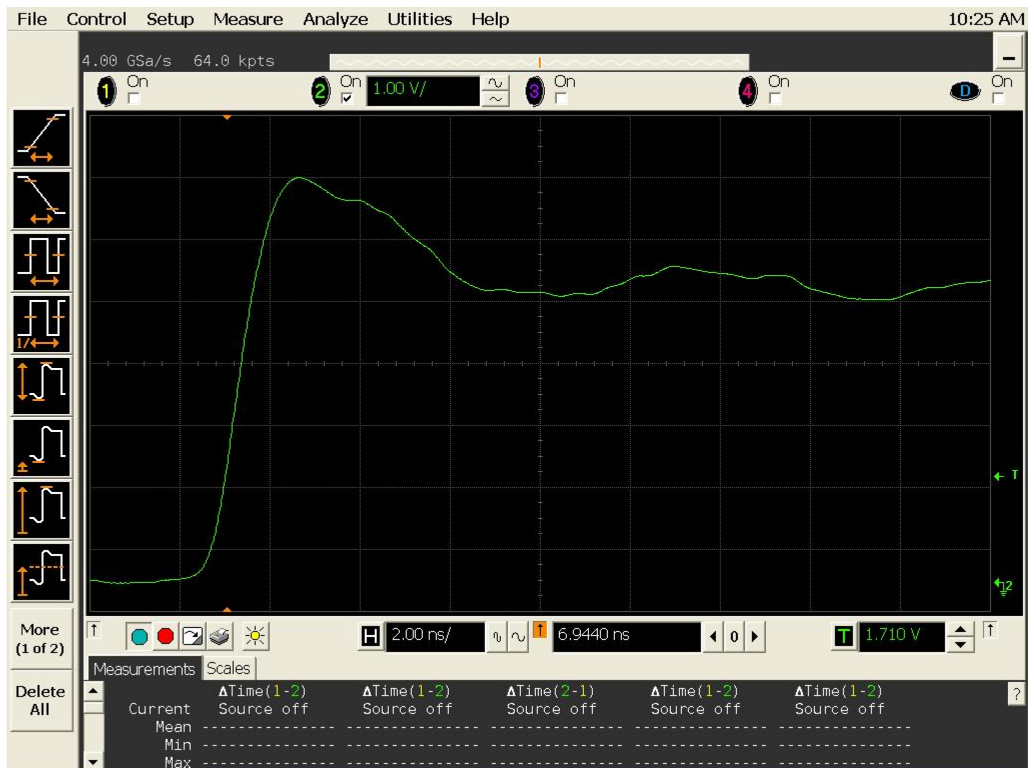

Figure 6b DUT 17989 Post-Annealing Rising Edge

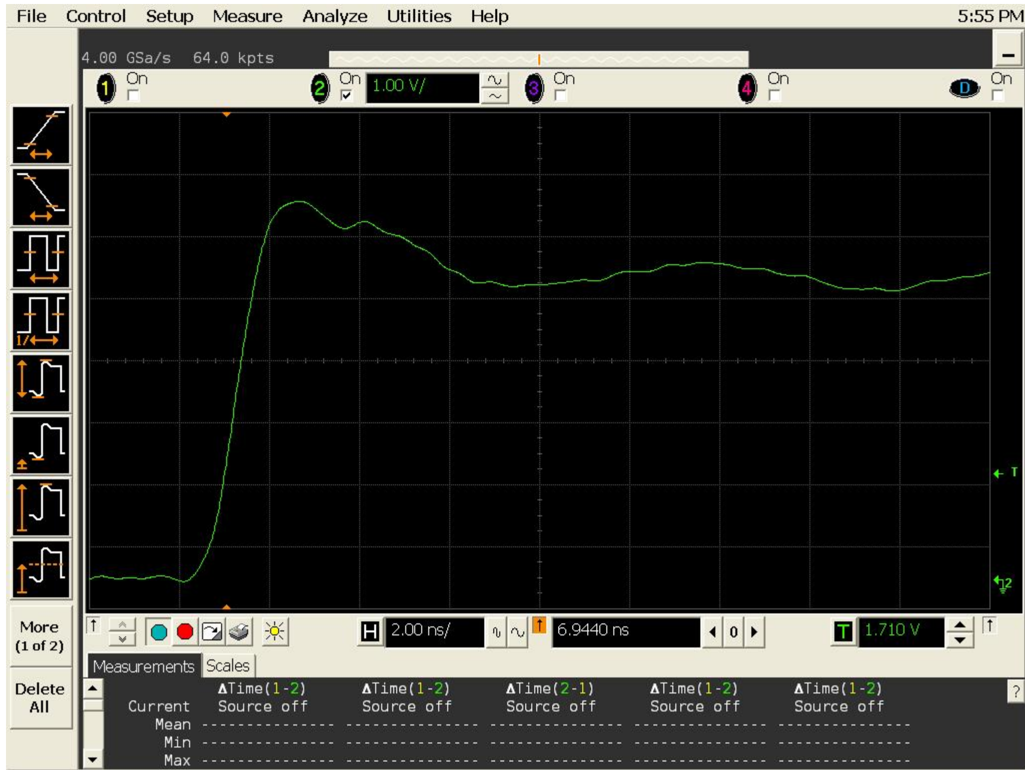

Figure 7a DUT 18005 Pre-Irradiation Rising Edge

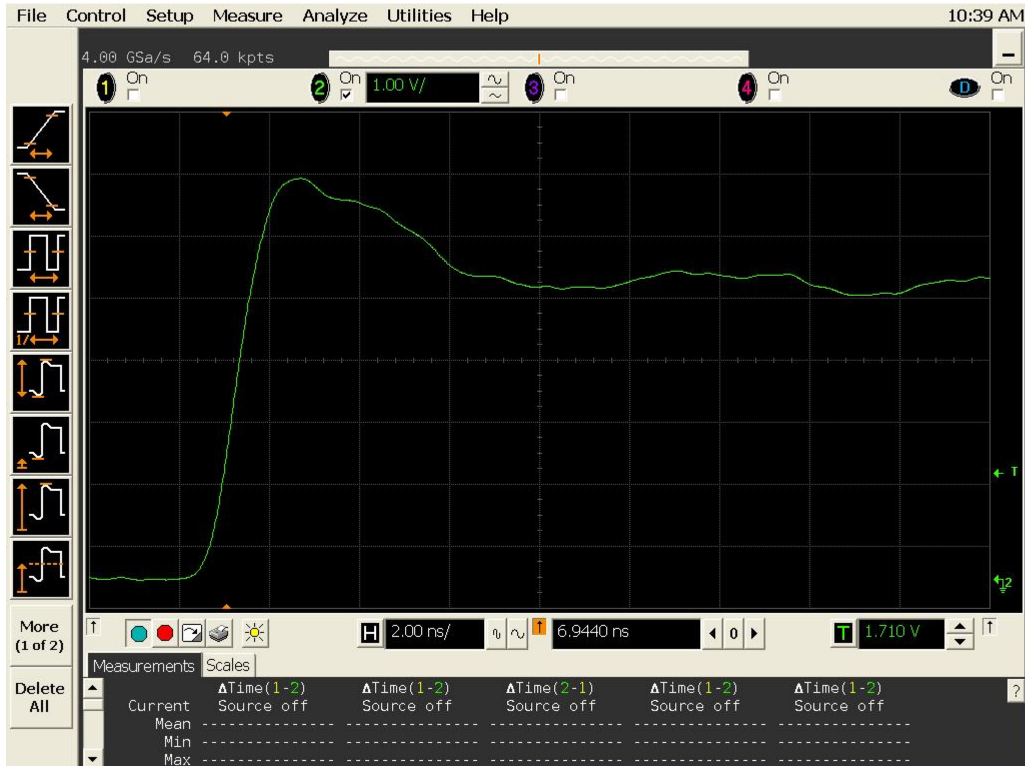

Figure 7b DUT 18005 Post-Annealing Rising Edge

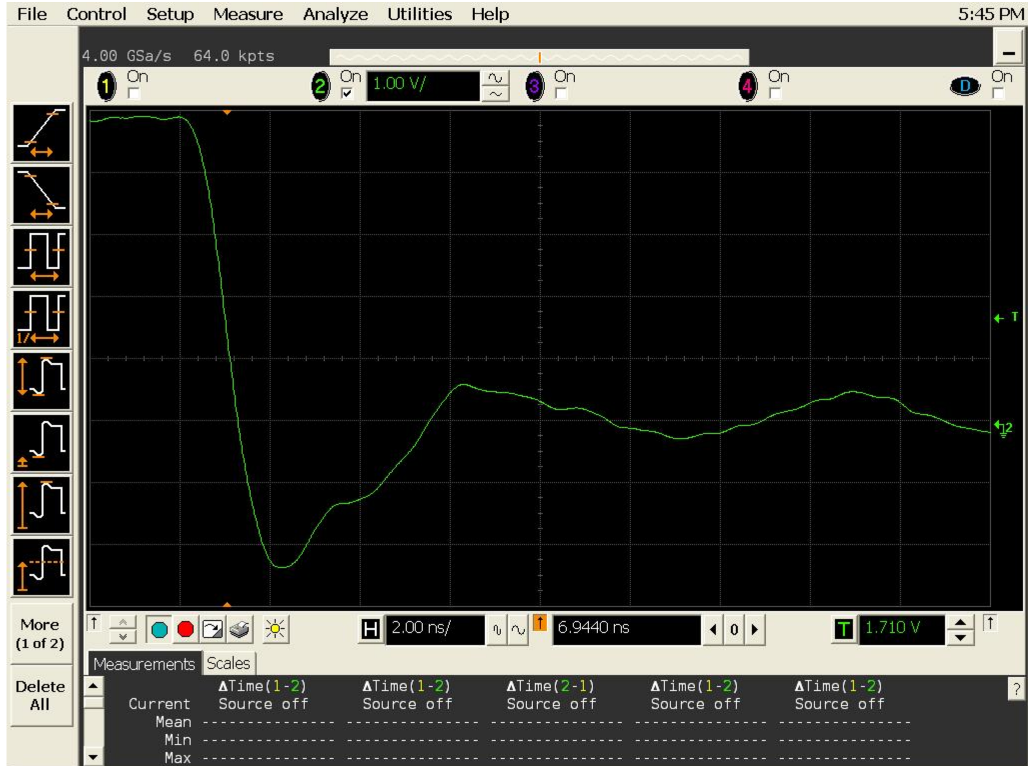

Figure 8a DUT 17896 Pre-Radiation Falling Edge

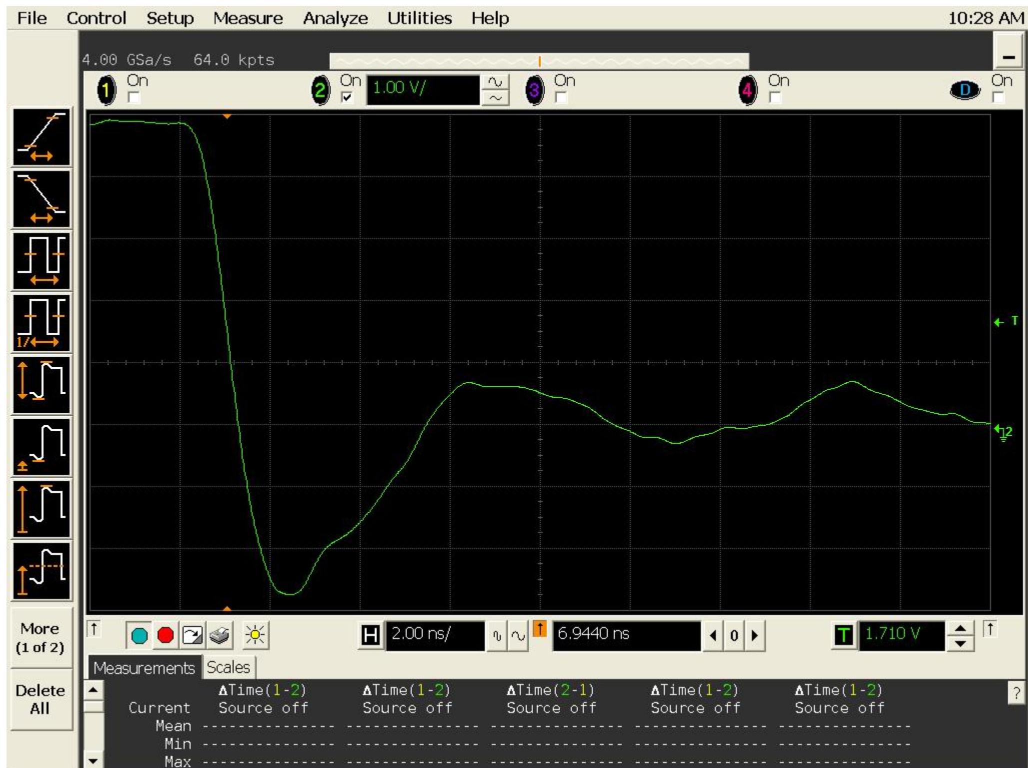

Figure 8b DUT 17896 Post-Annealing Falling Edge

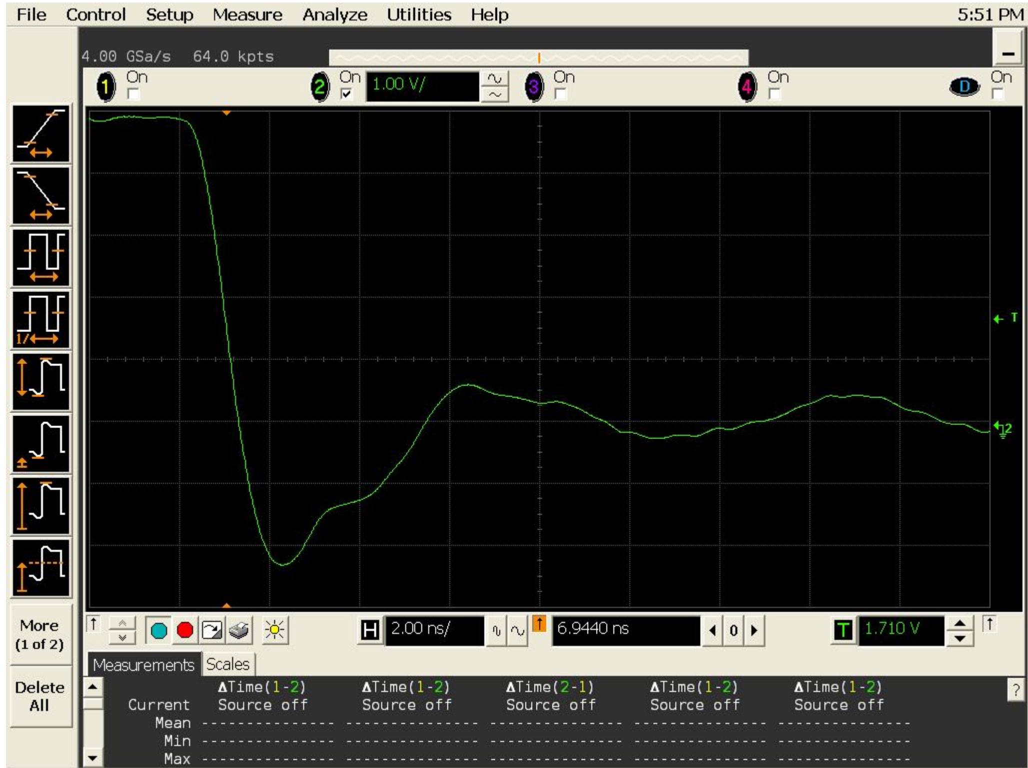

Figure 9a DUT 17899 Pre-Irradiation Falling Edge

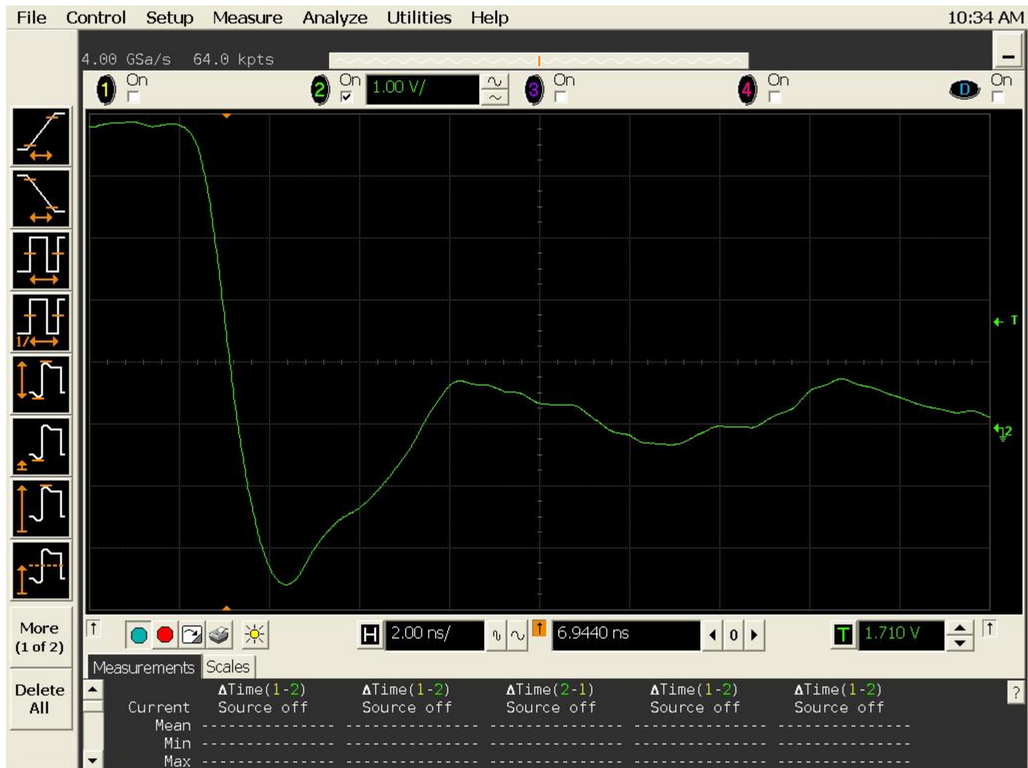

Figure 9b DUT 17899 Post-Annealing Falling Edge

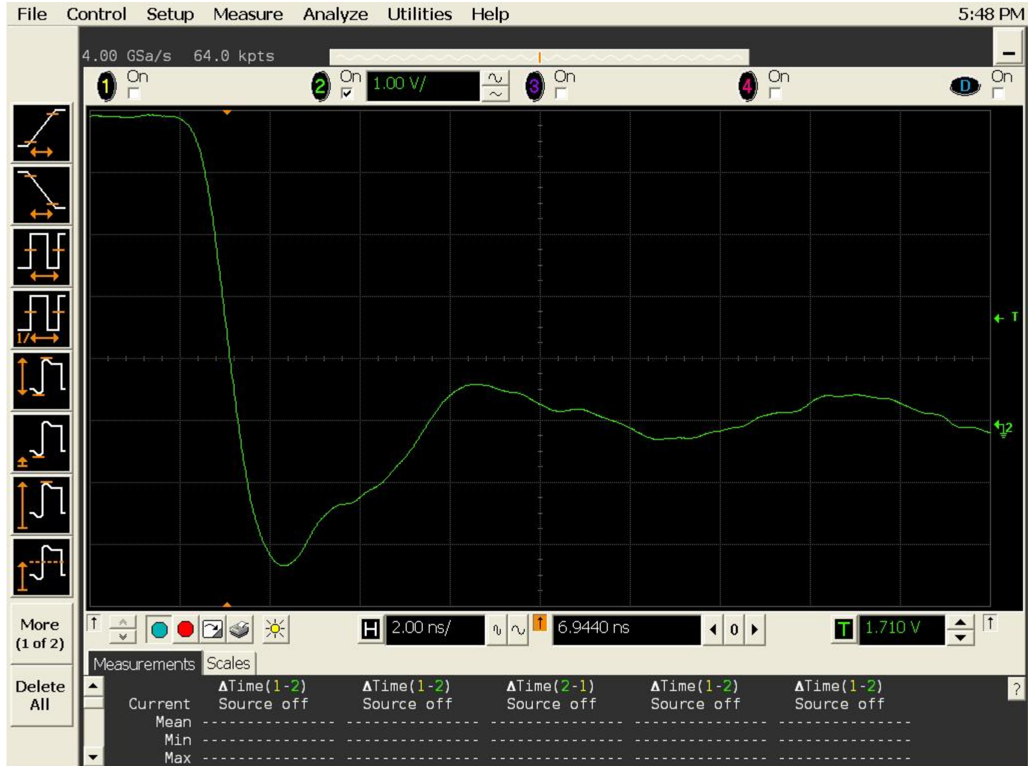

Figure 10a DUT 17912 Pre-Irradiation Falling Edge

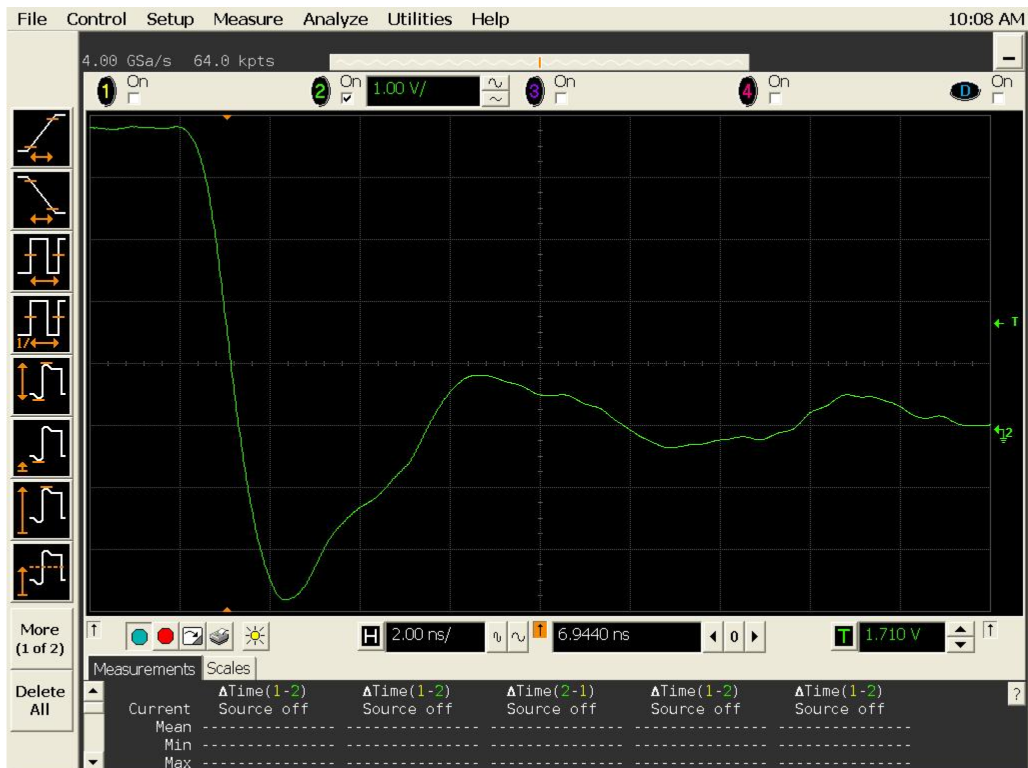

Figure 10b DUT 17912 Post-Annealing Falling Edge

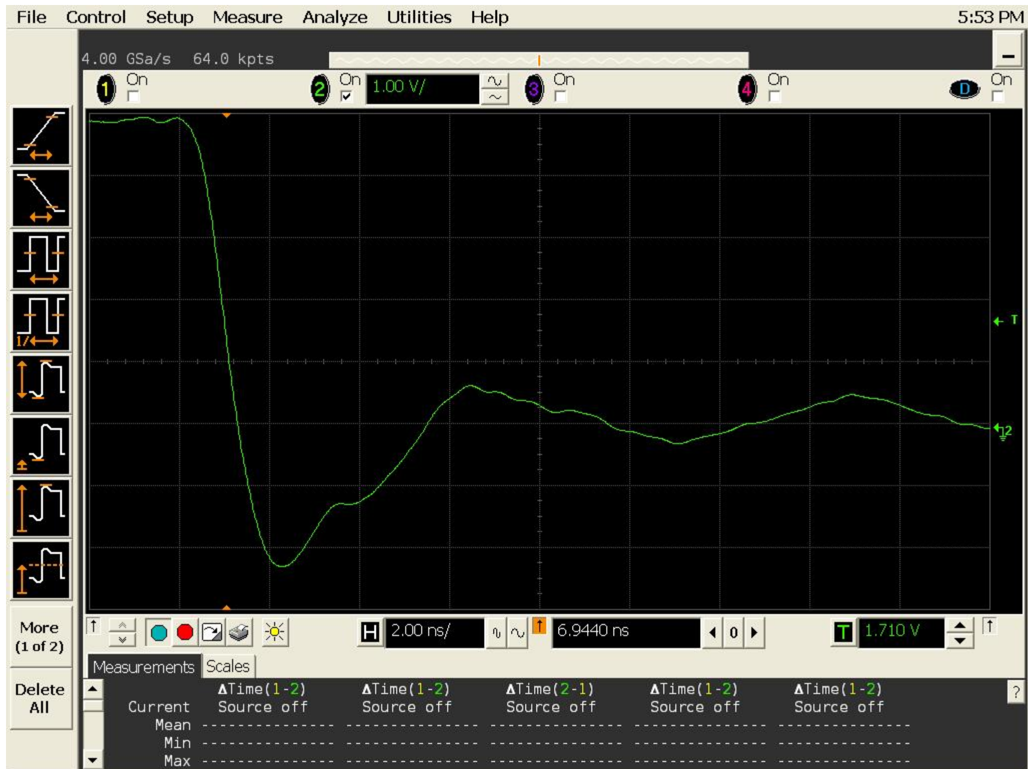

Figure 11a DUT 17976 Pre-Irradiation Falling Edge

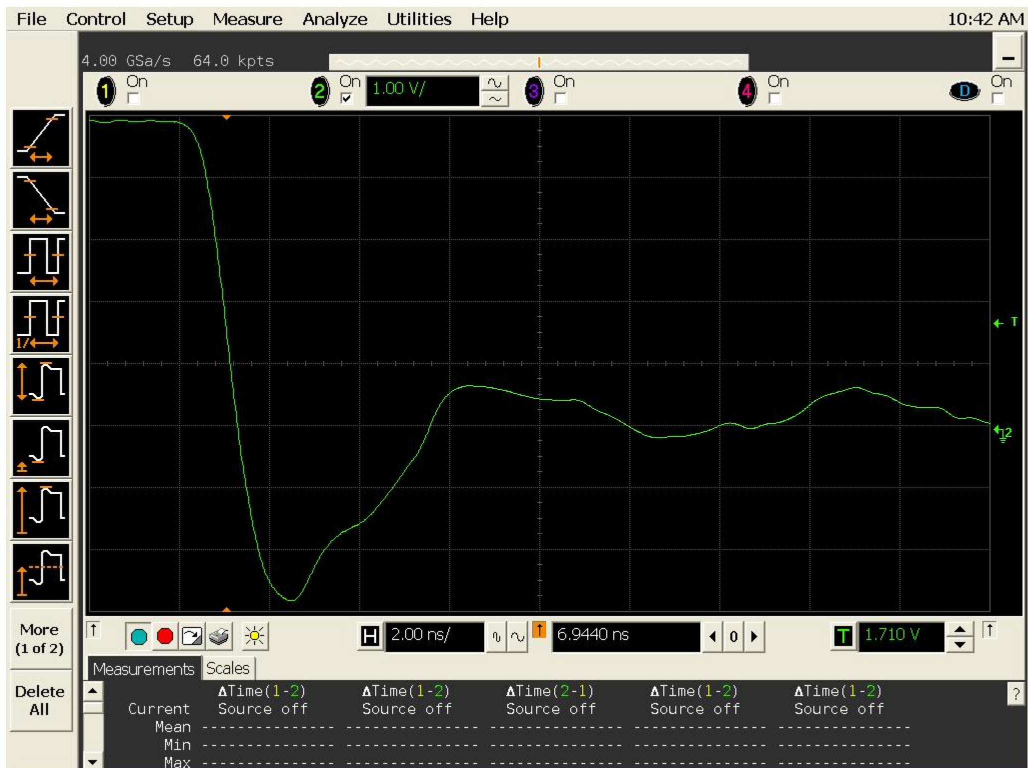

Figure 11b DUT 17976 Post-Annealing Falling Edge

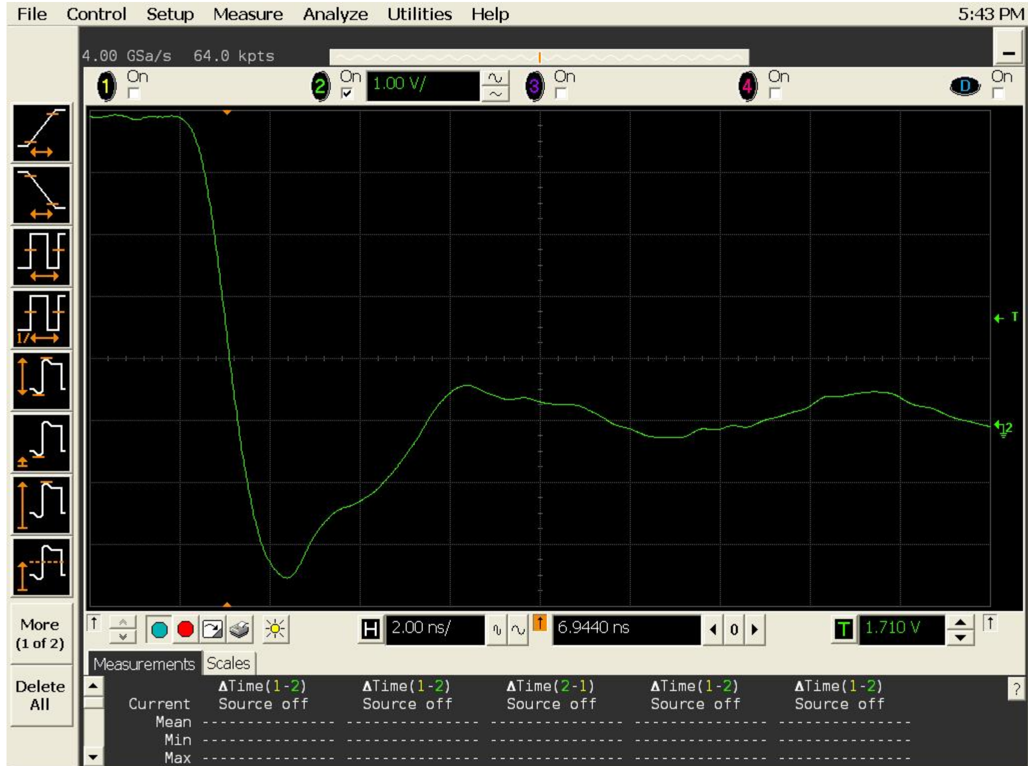

Figure 12a DUT 17989 Pre-Irradiation Falling Edge

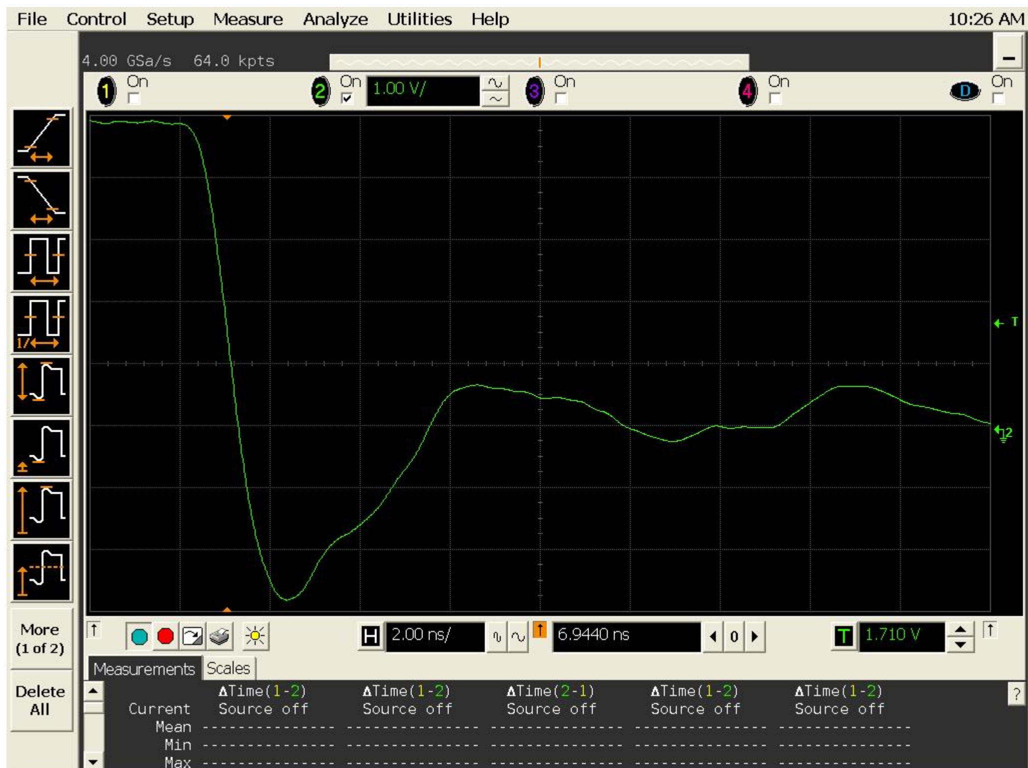

Figure 12b DUT 17989 Post-Annealing Falling Edge

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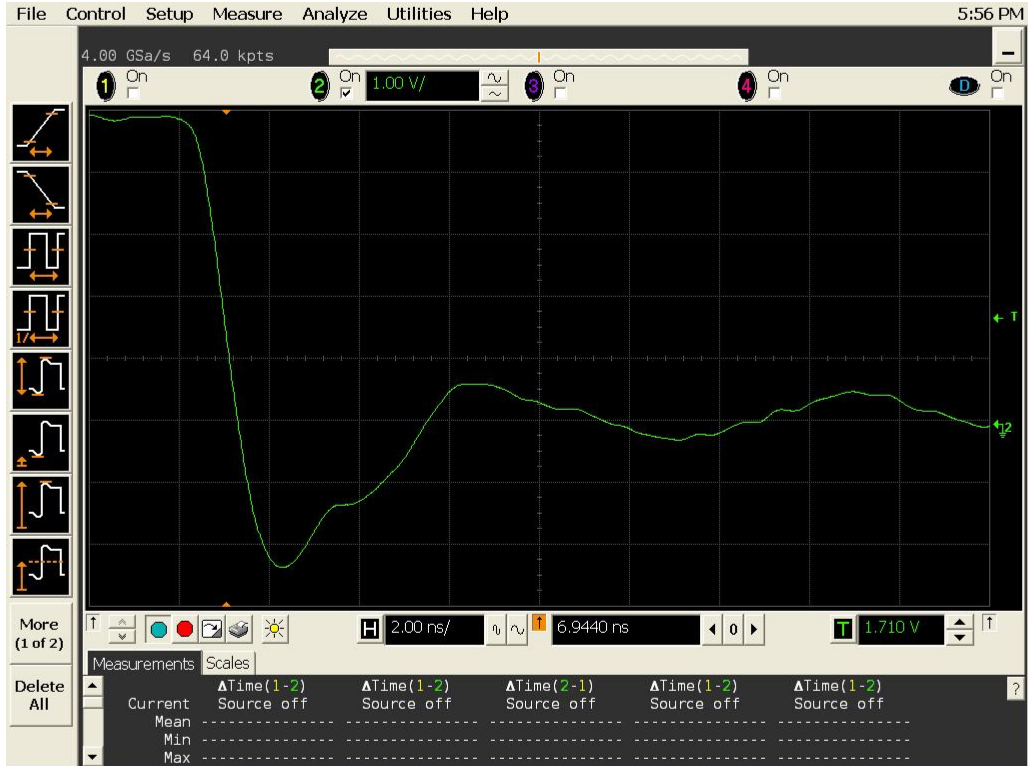


Figure 13a DUT 18005 Pre-Irradiation Falling Edge

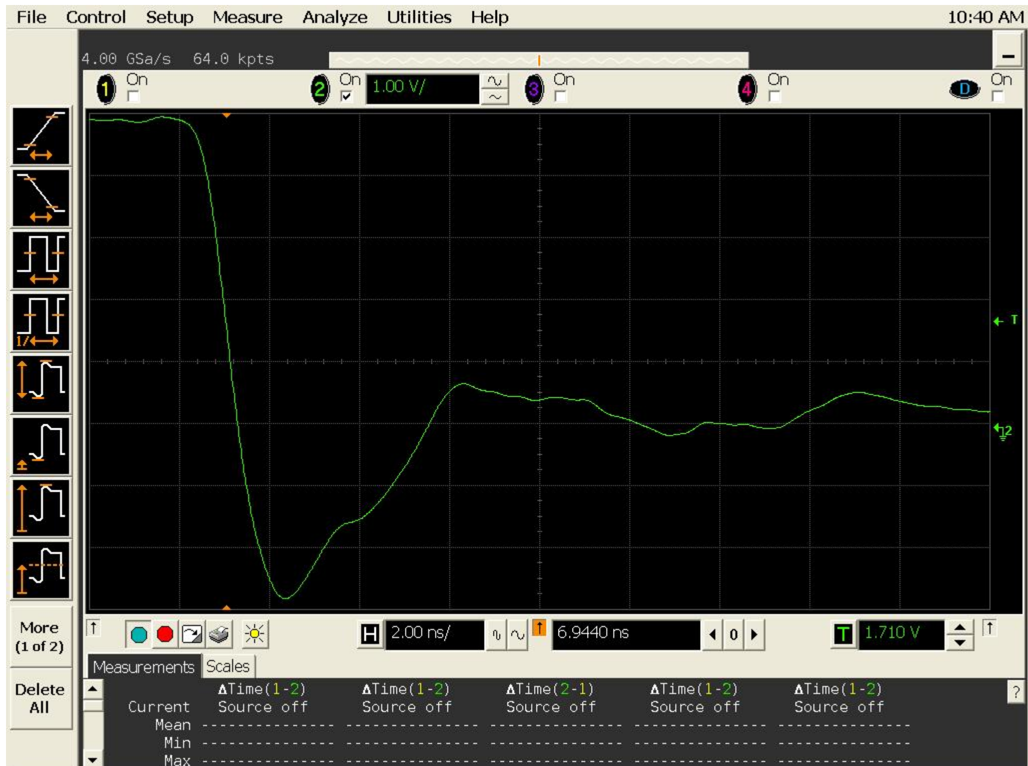


Figure 13b DUT 18005 Post-Annealing Falling Edge

Appendix A: DUT Bias

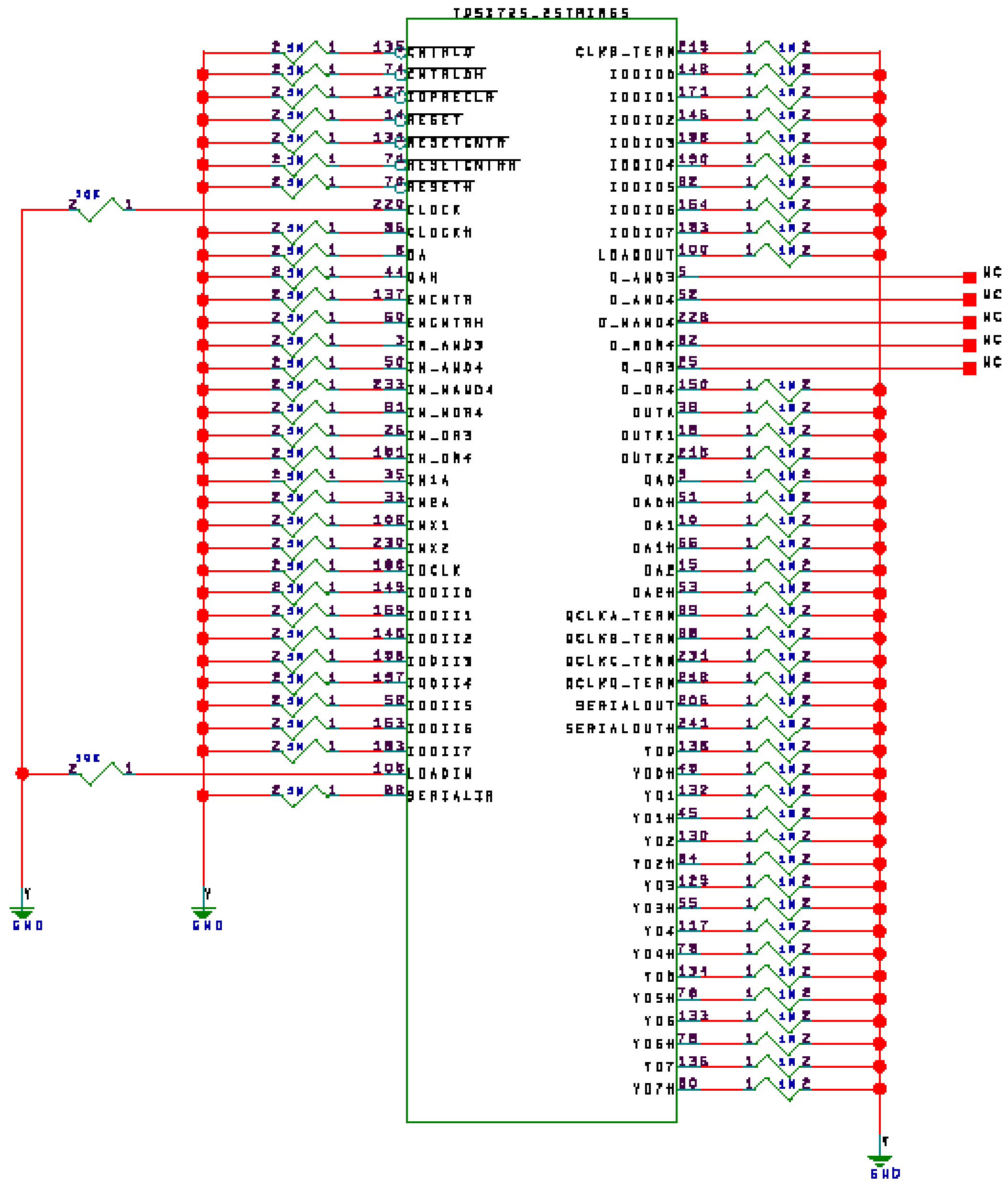


Figure A1 I/O Bias During Irradiation

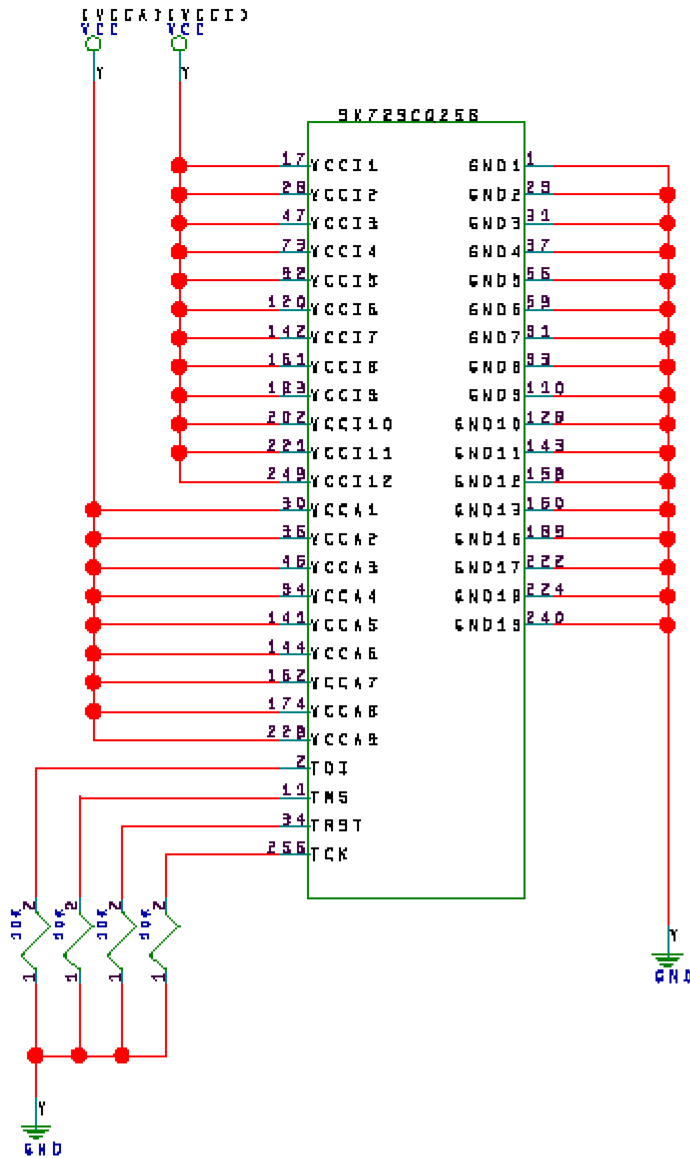
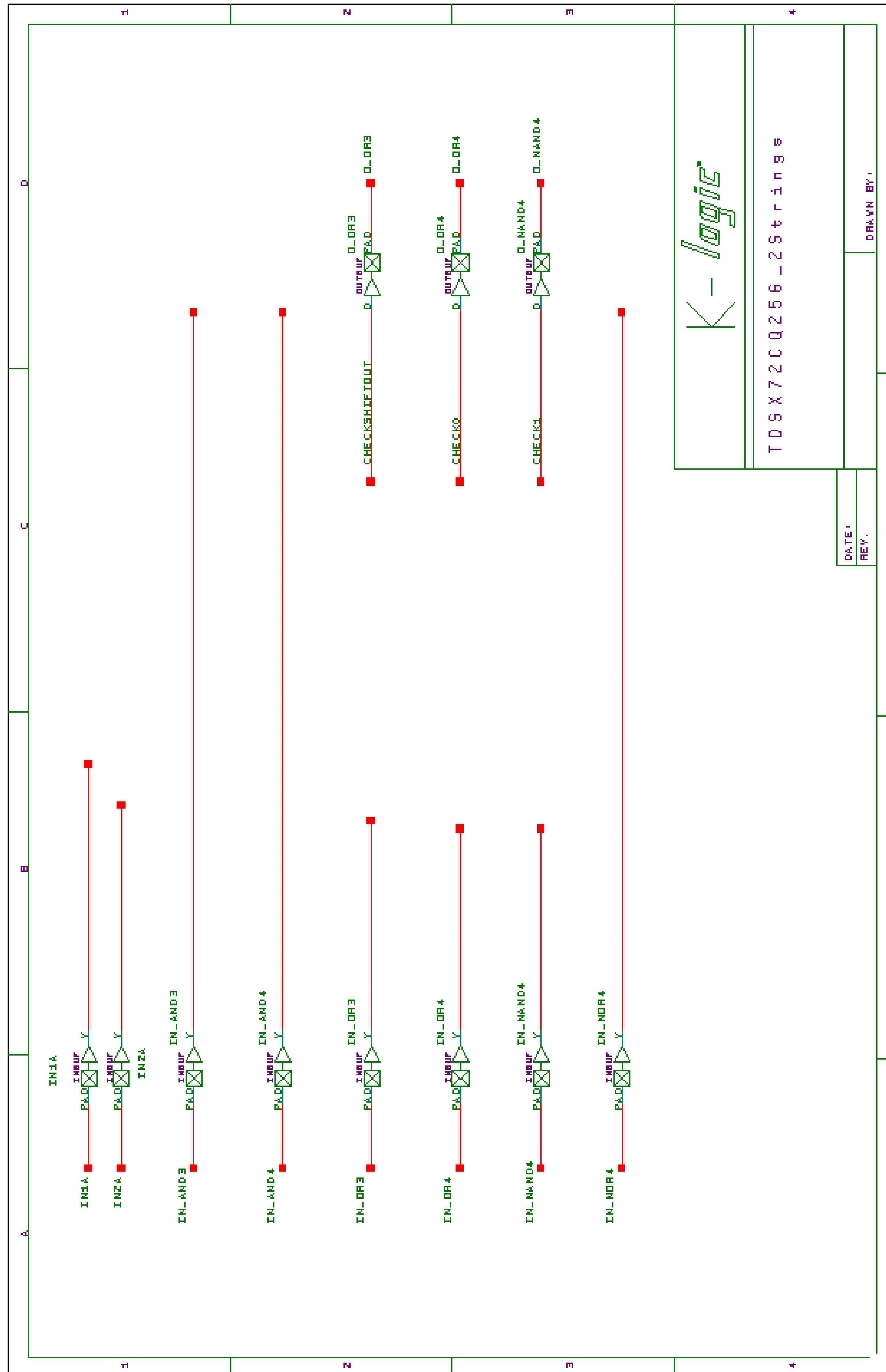
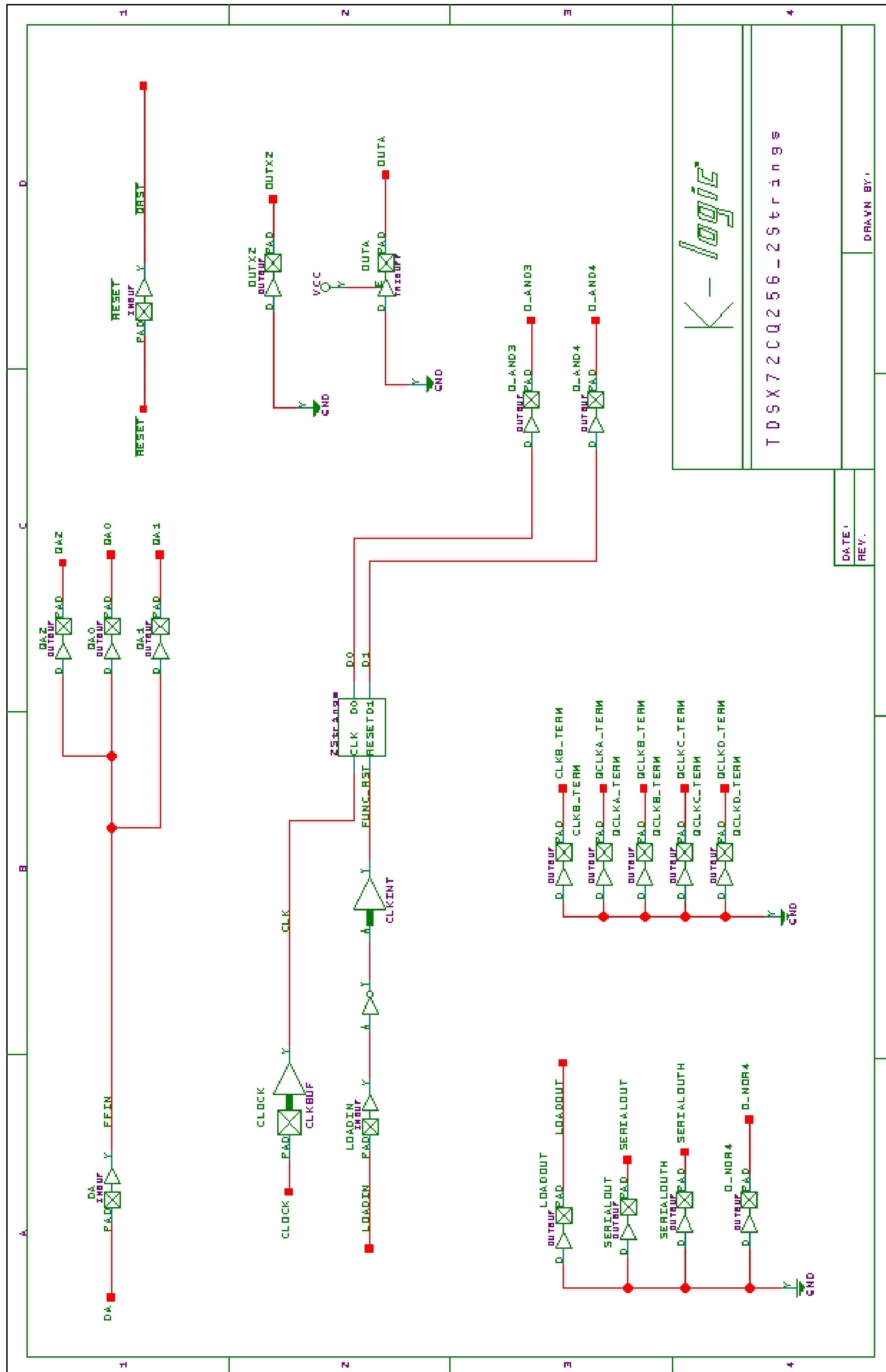


Figure A2 Power Supply, Ground and Special Pins Bias During Irradiation

Appendix B: DUT Design Schematics

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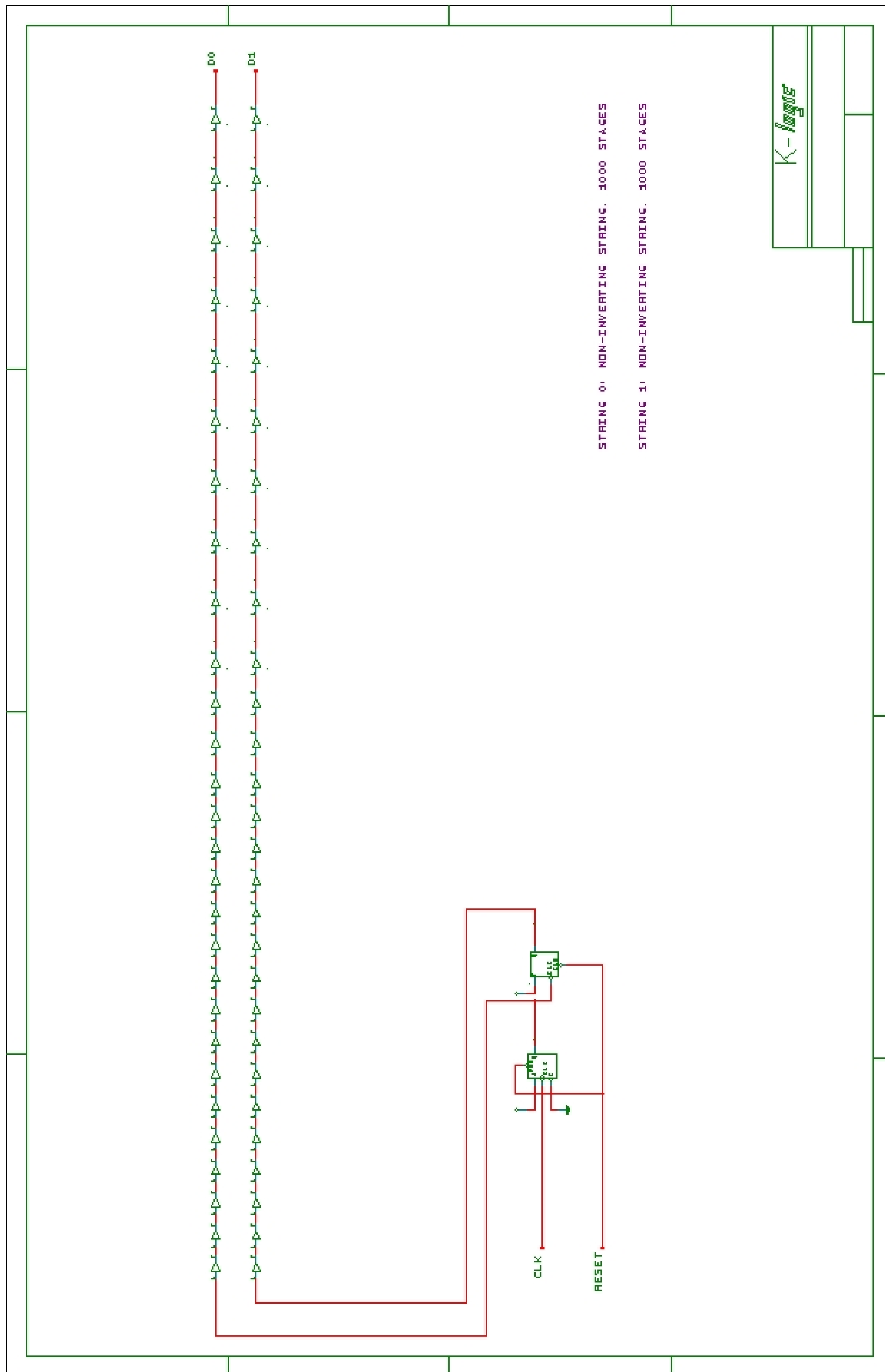
TDSX72CQ256_25strings
DRAWN BY:
DATE:
REV.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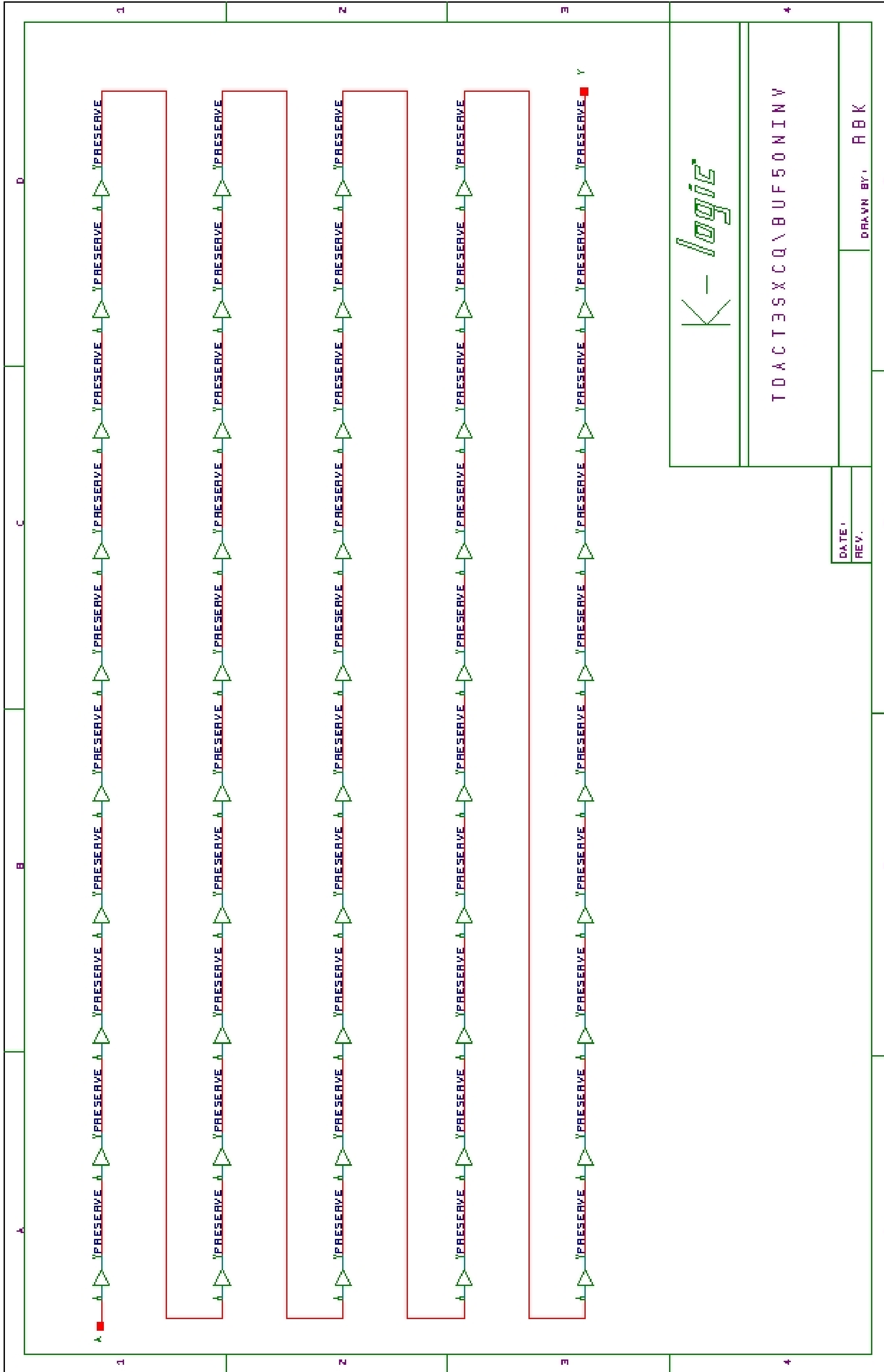
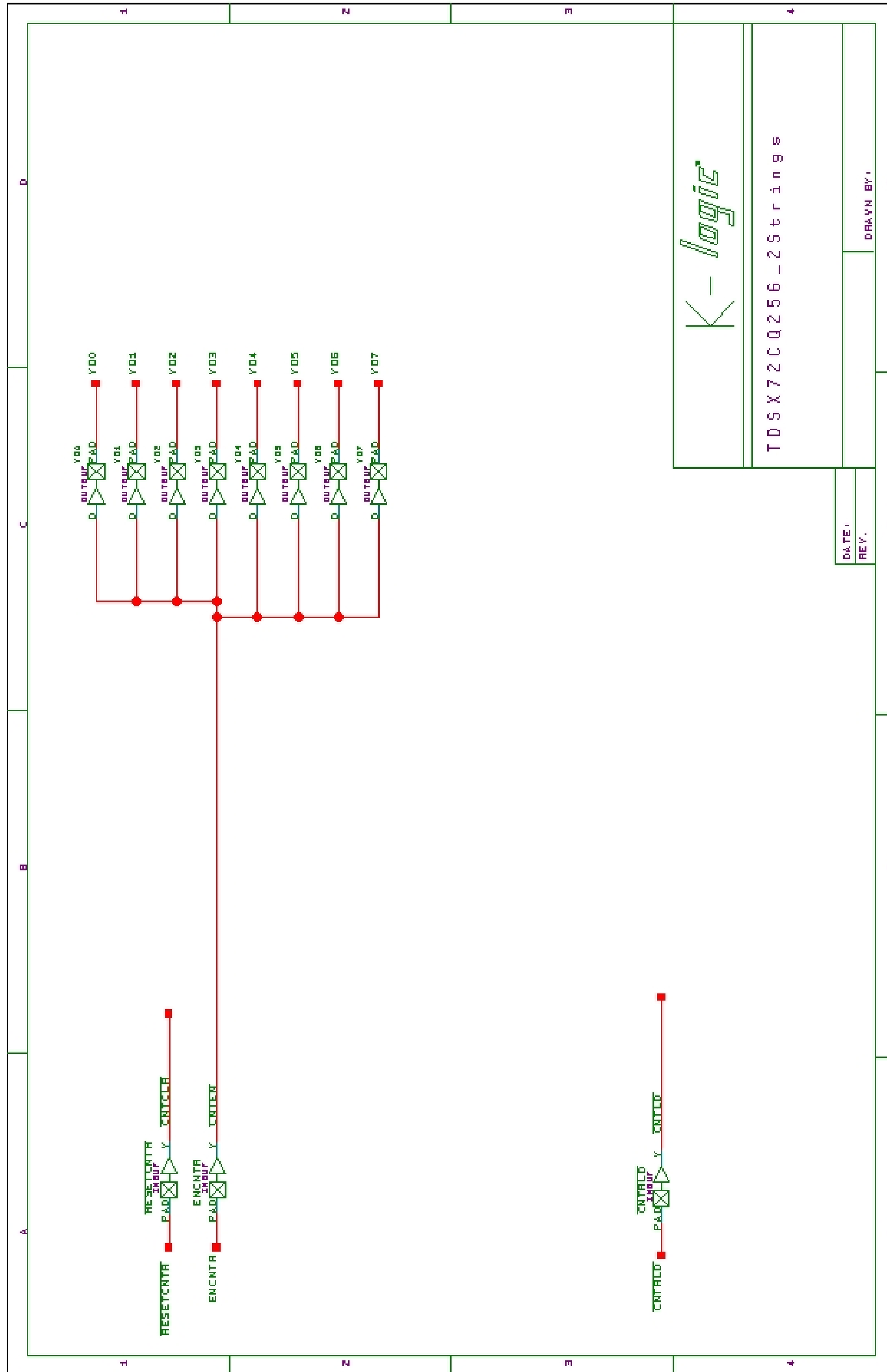
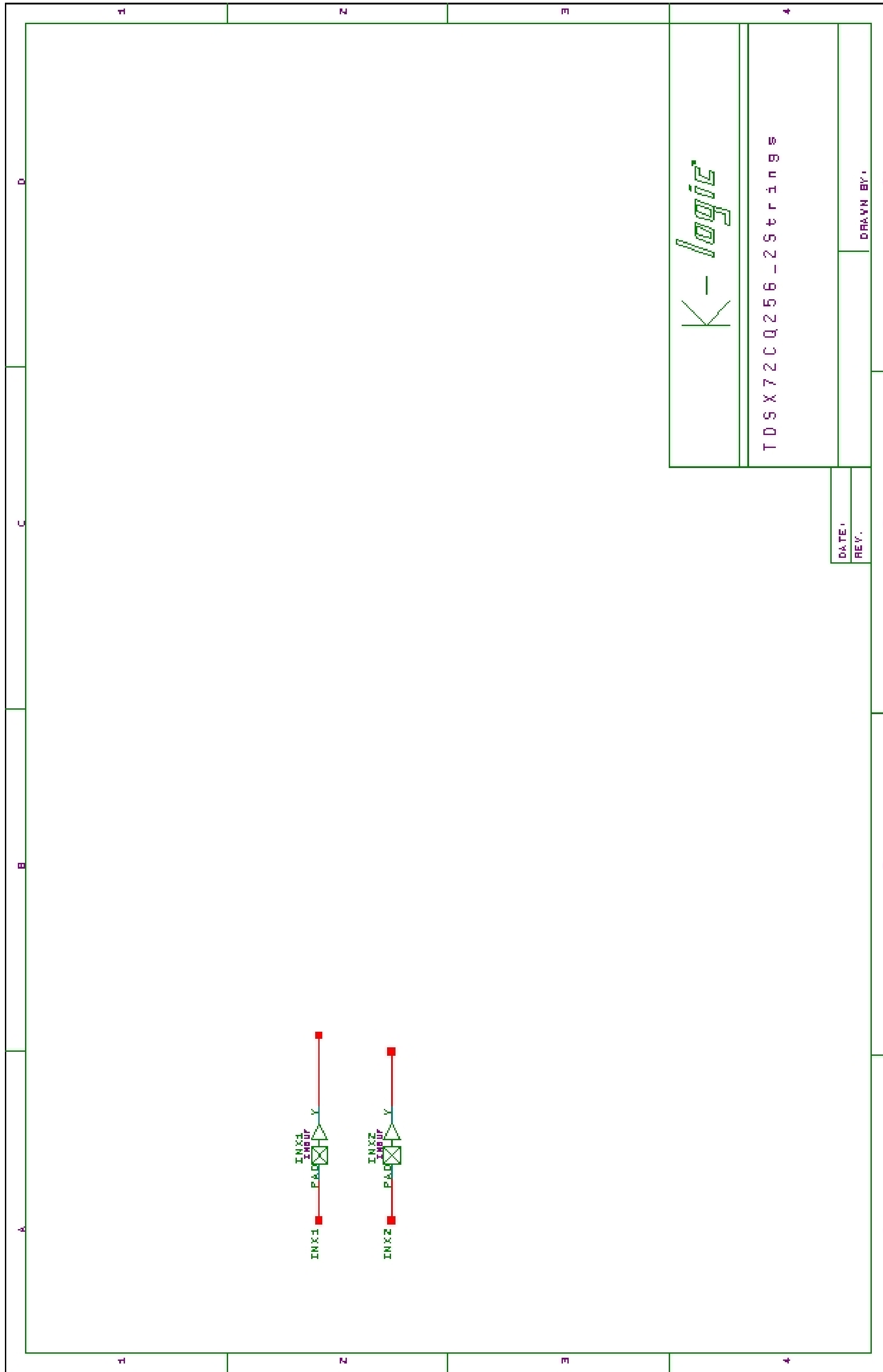
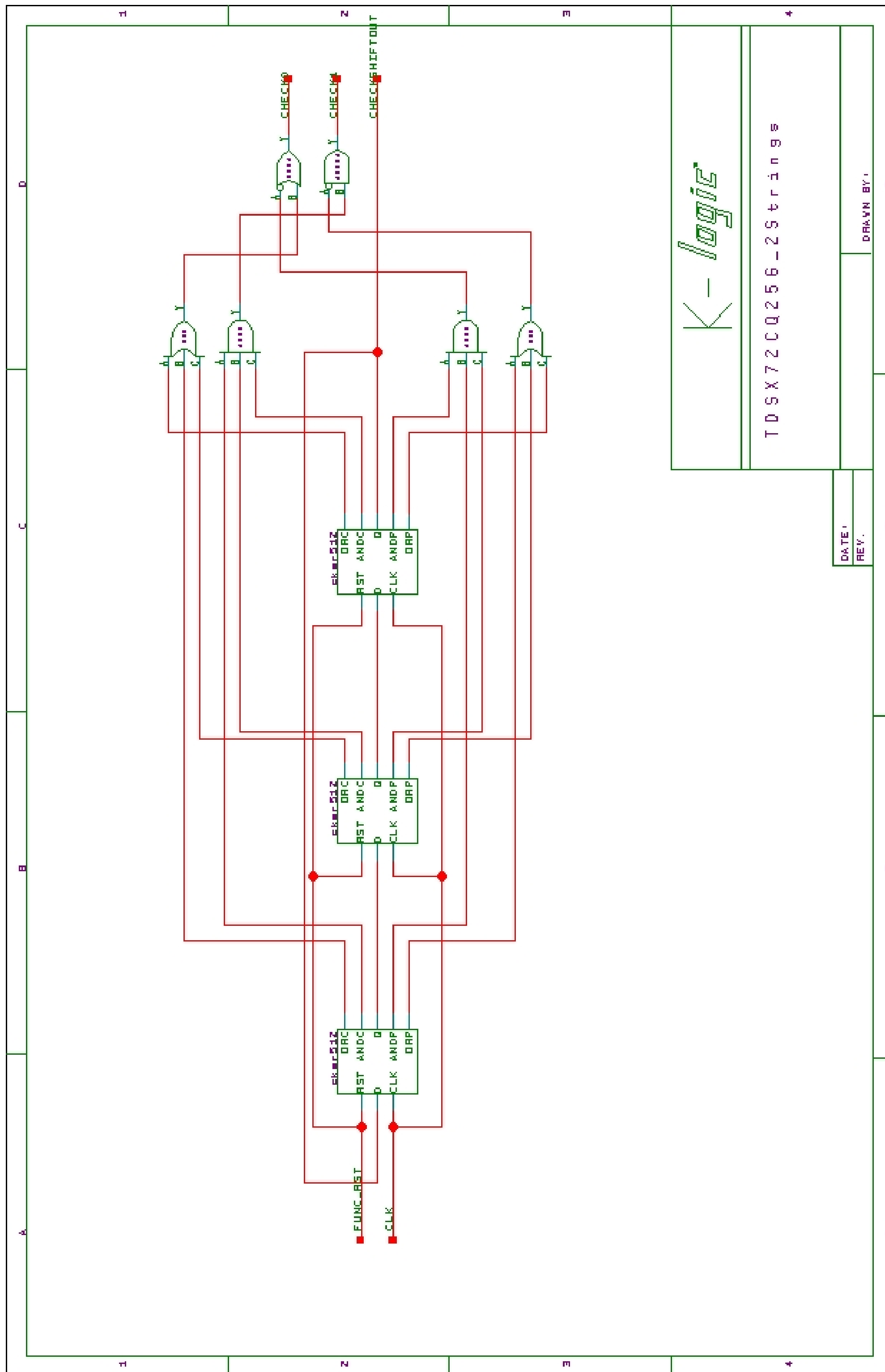
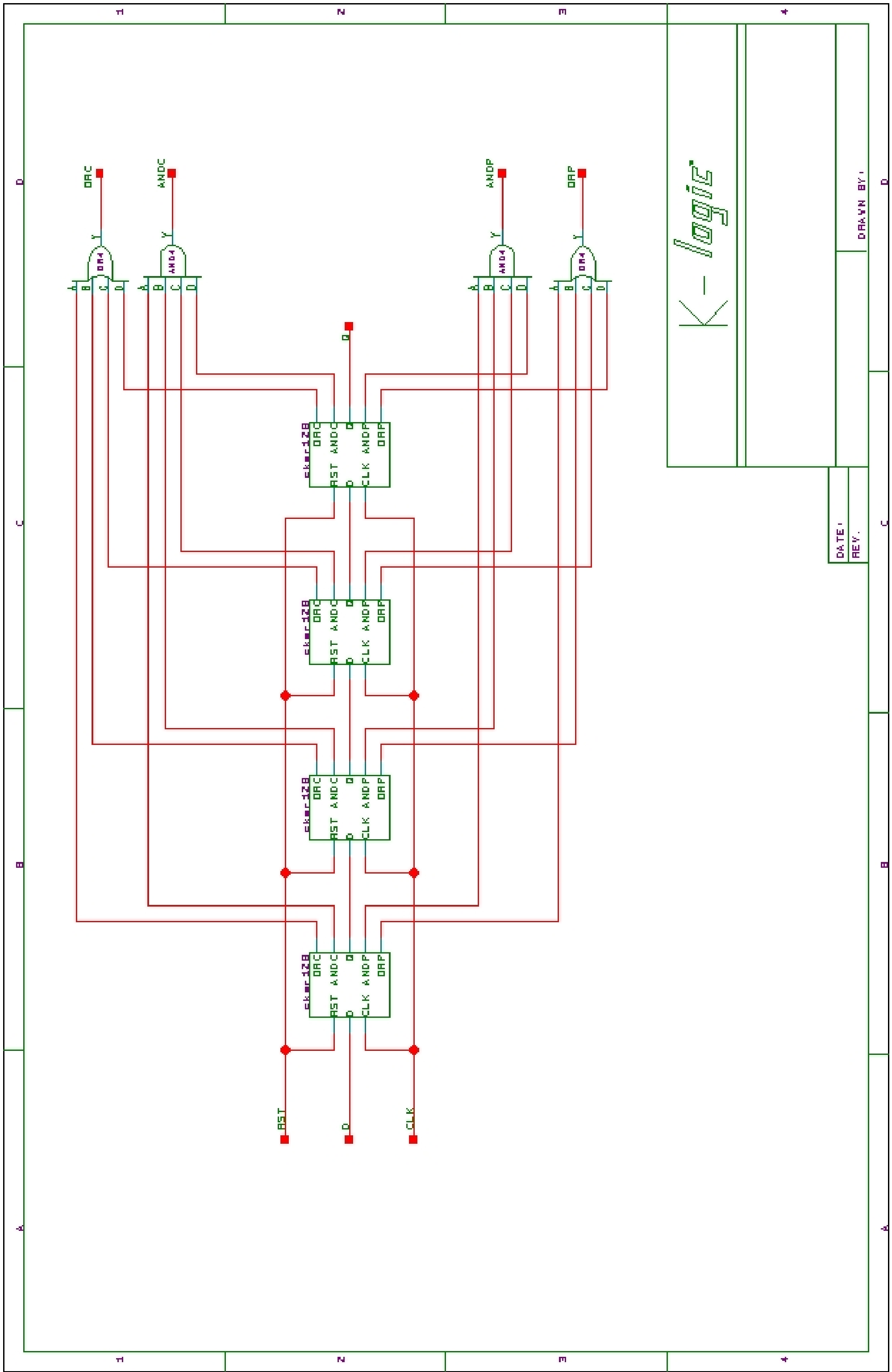
D1
STRING 0: NON-INVERTING STRING. 1000 STAGES
STRING 1: NON-INVERTING STRING. 1000 STAGES
K-logic
CLK
RESET

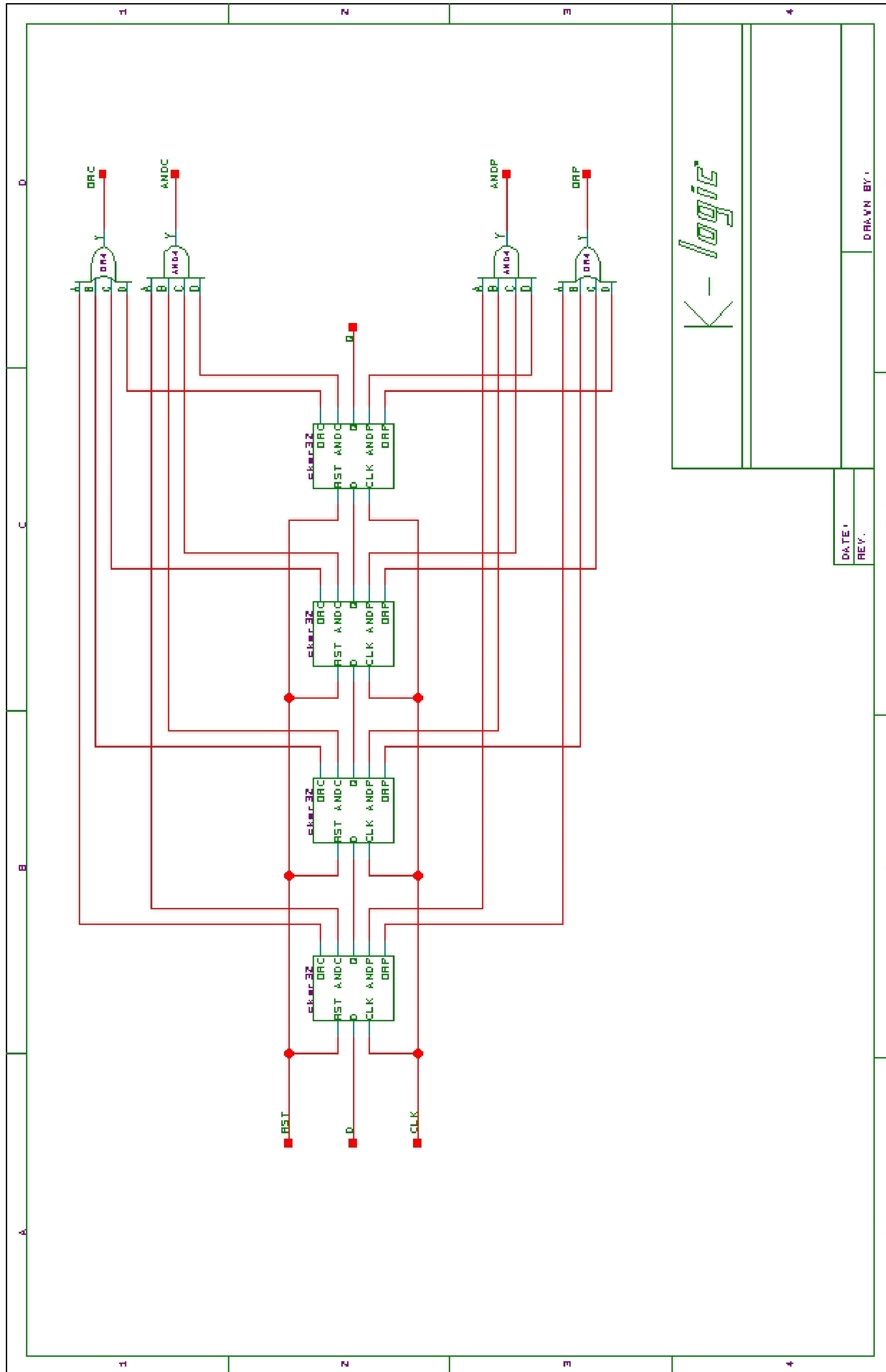

K-logic
TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
PRESERVE
A
Y

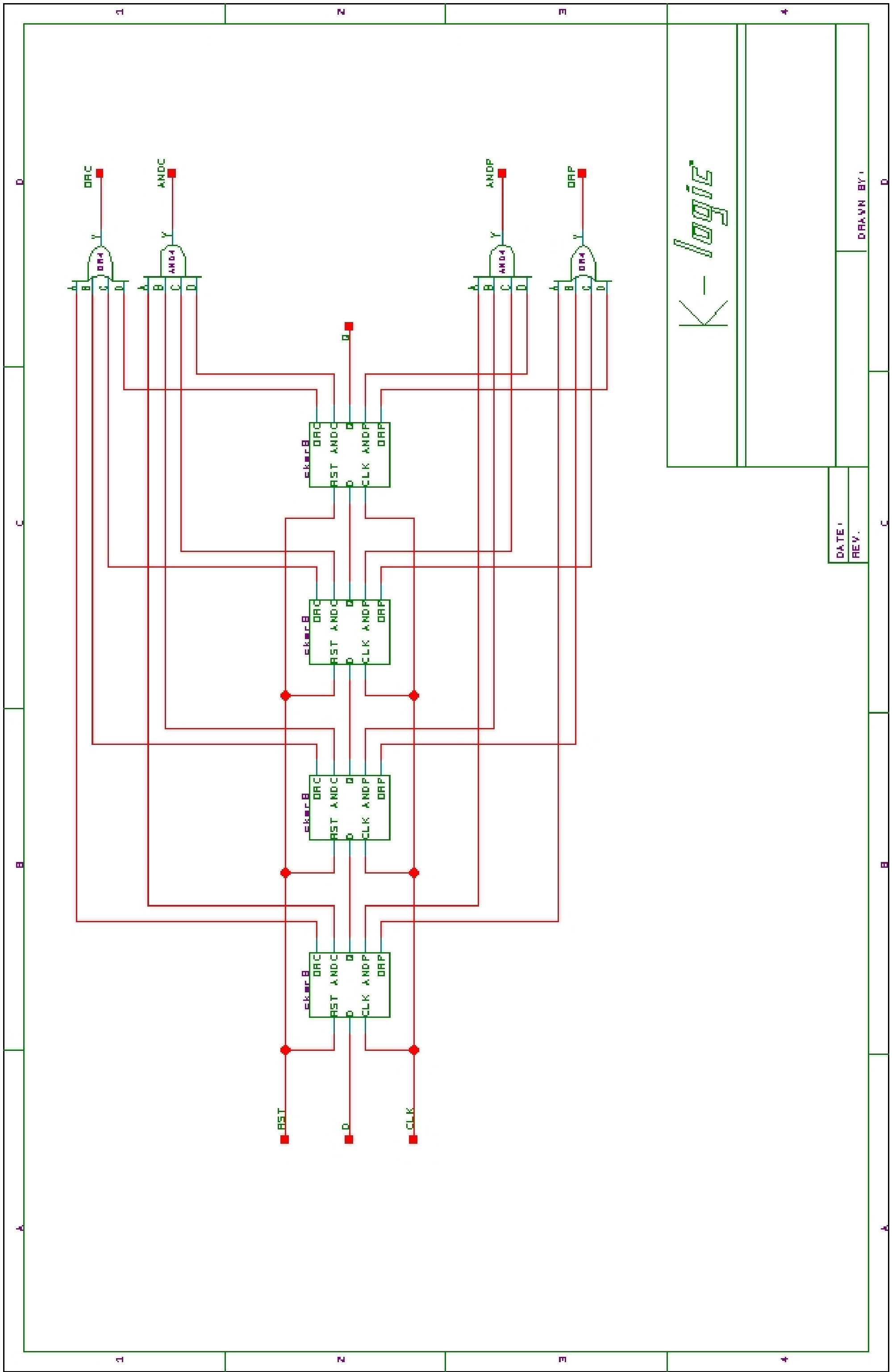

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YO0
YO1
YO2
YO3
YO4
YO5
YO6
YO7
RESETCNTA
ENCNTA
CNTALD
CNTCLR
CNTEN
CNTLD

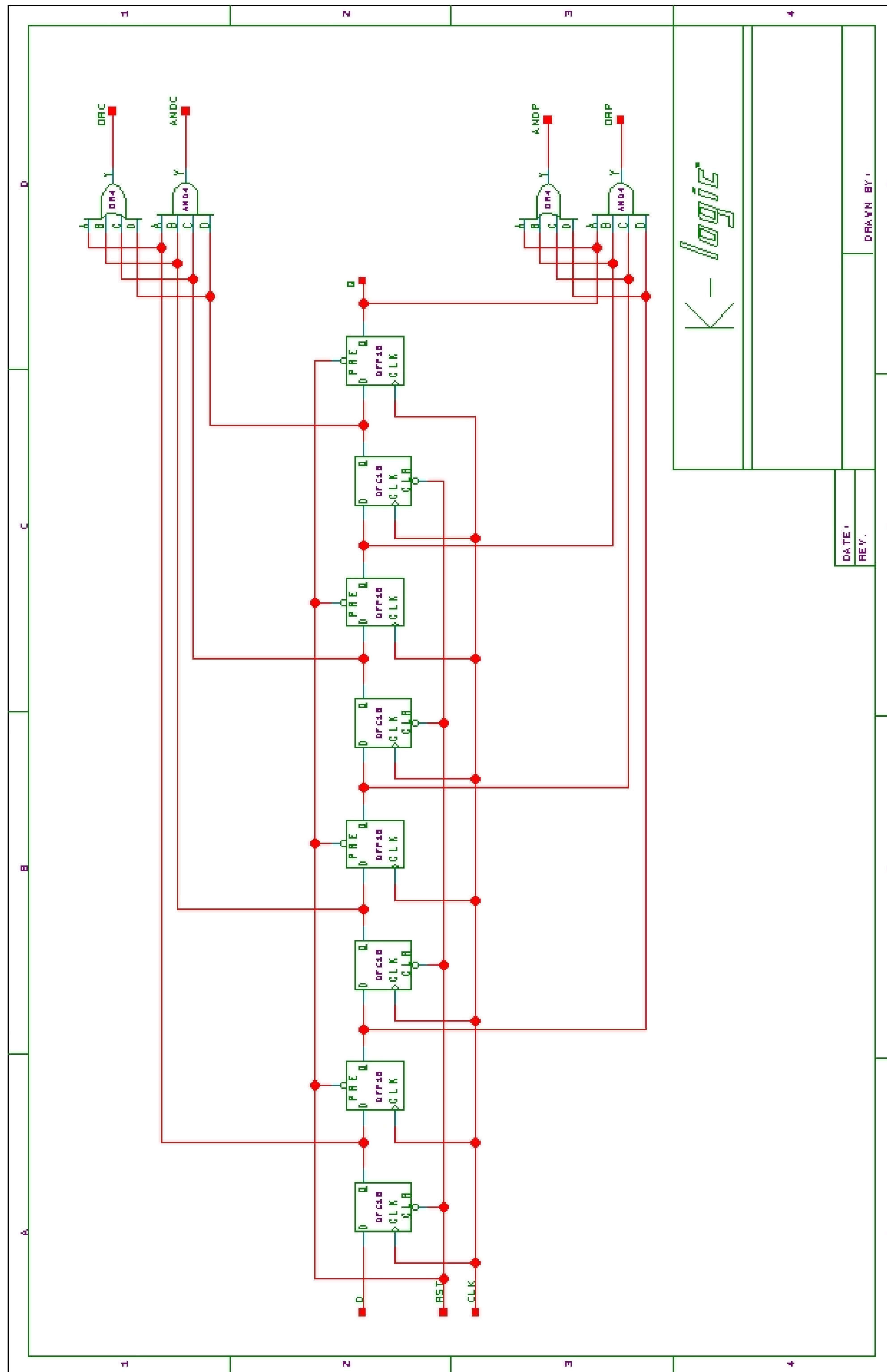

TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
INX1
INX2
INBUF
PAD
Y

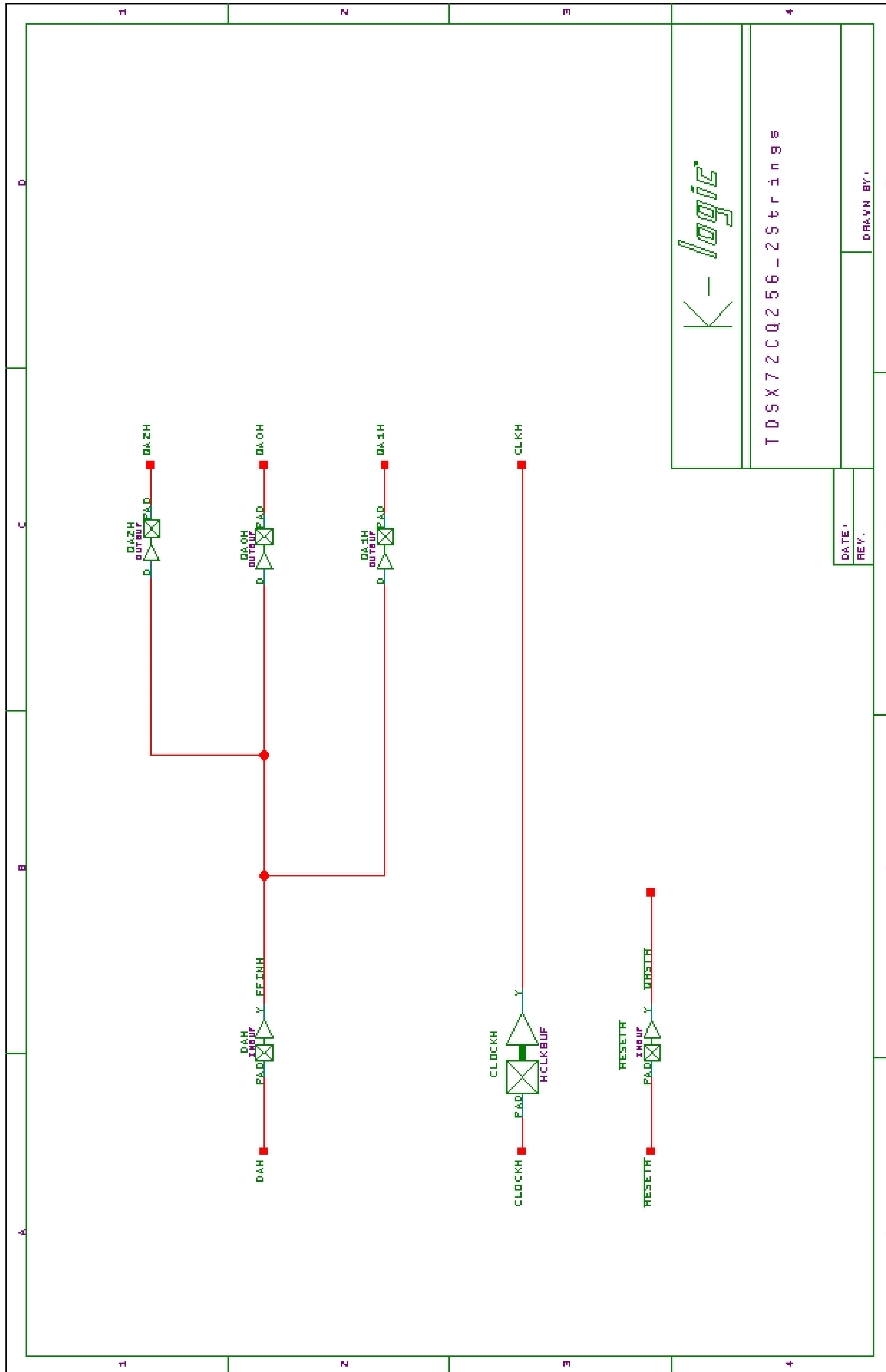

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

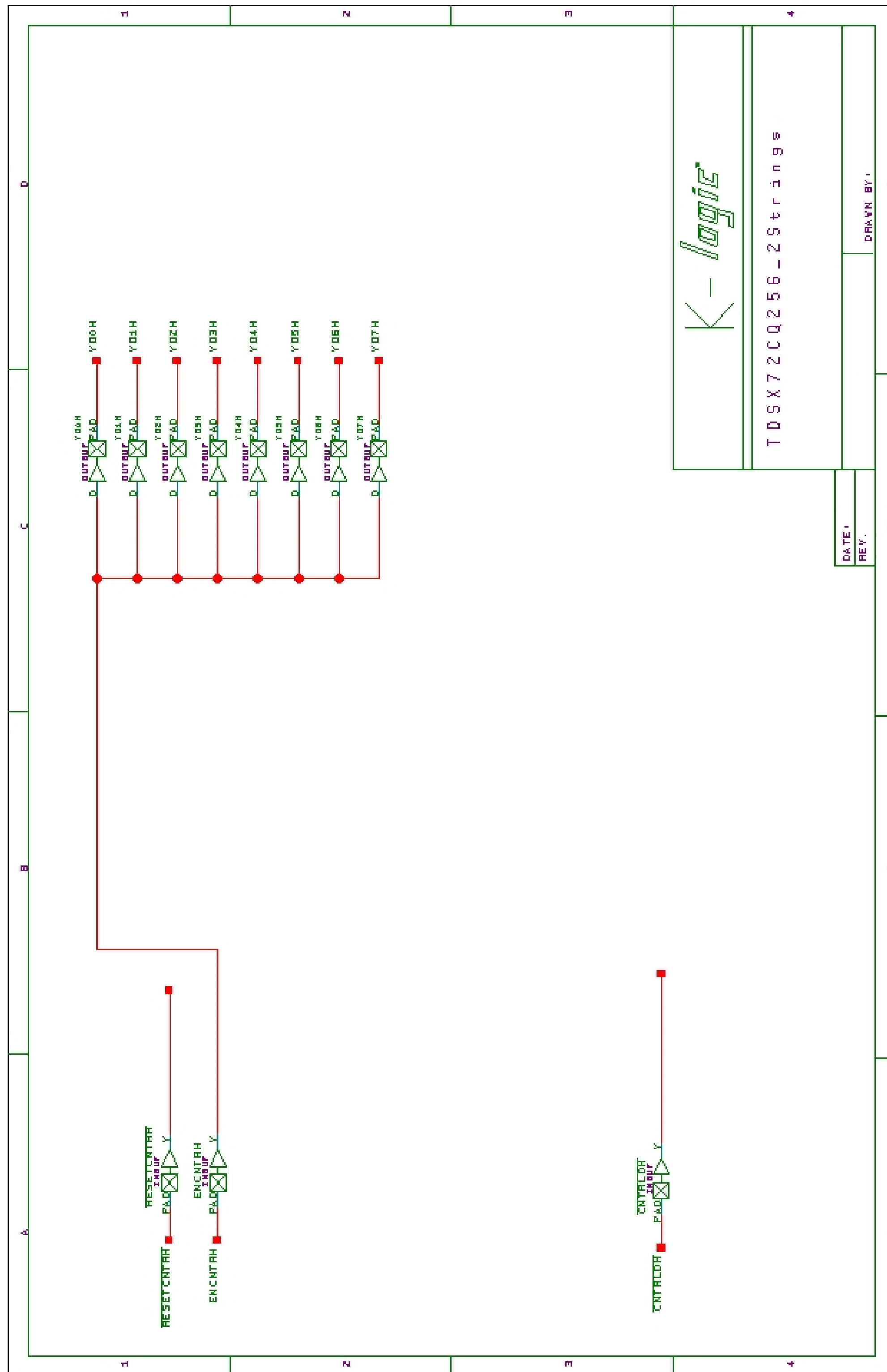


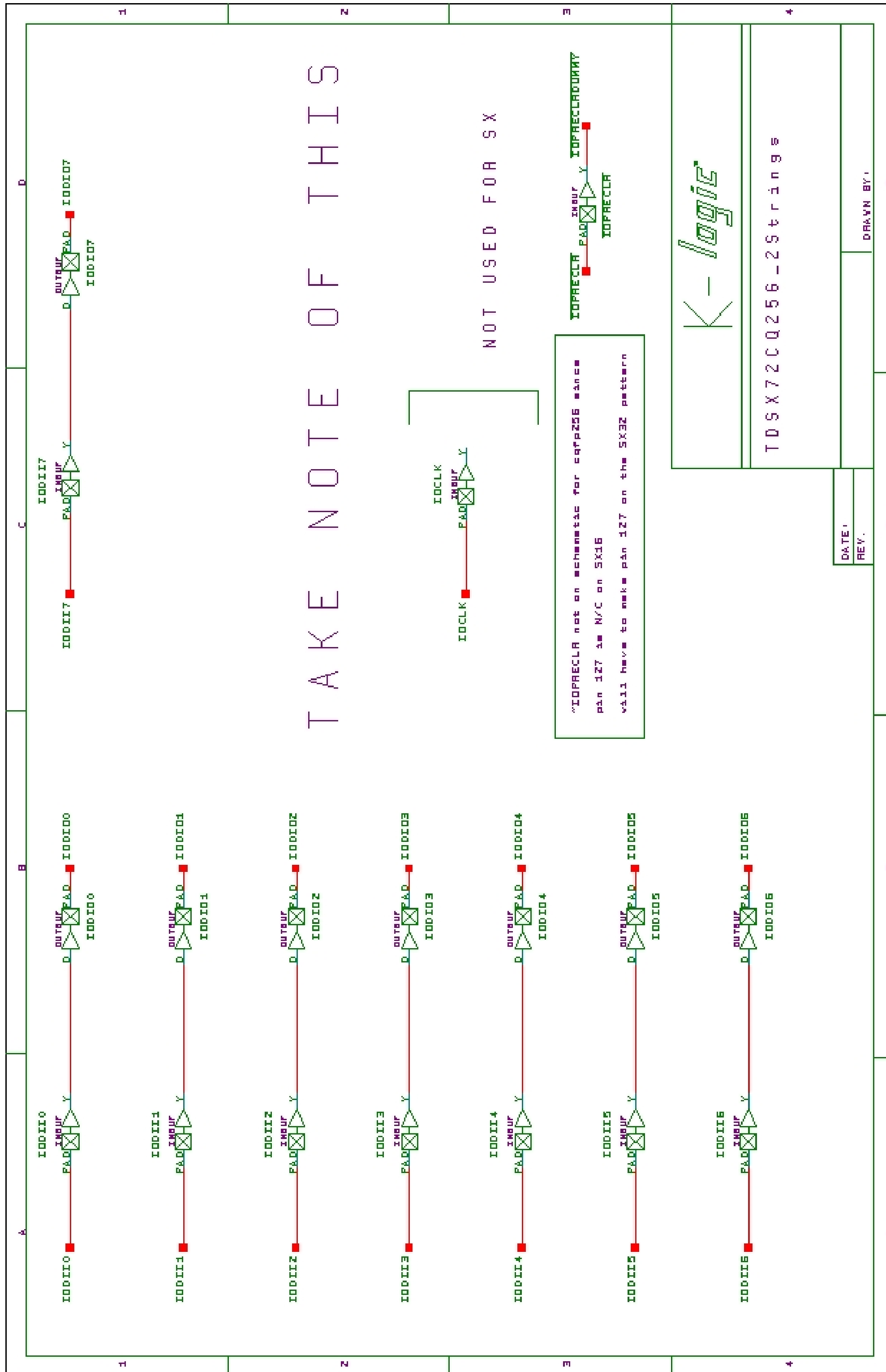

ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr32
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV:


ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DATE:
REV.
DRAWN BY:
K - logic

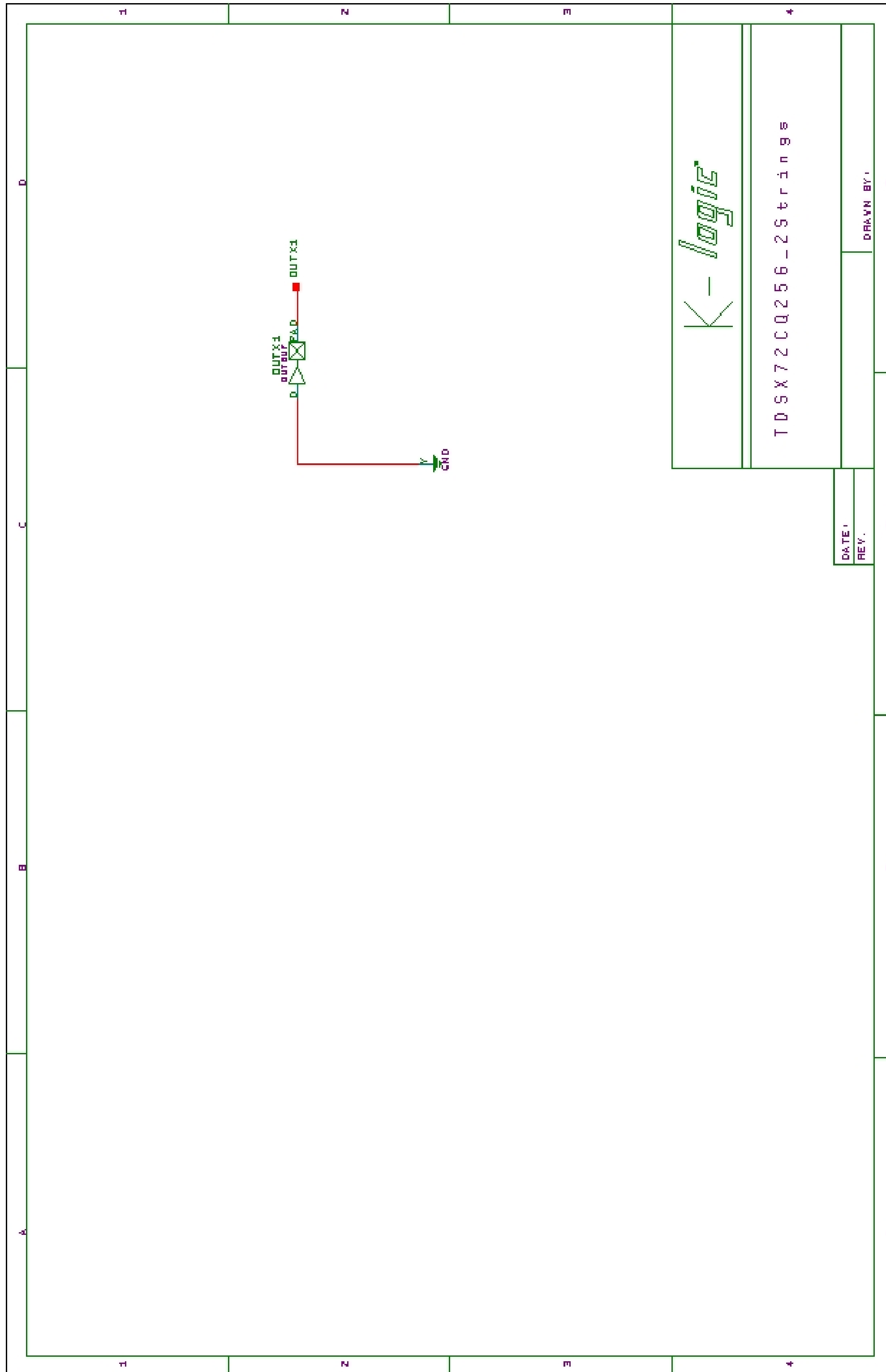



TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:
DA2H
DA0H
DA1H
CLKH
DAH
CLOCKH
RESETH





TAKE NOTE OF THIS
NOT USED FOR SX
TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.



TDSX72CQ256_2Strings
K-logic
OUTX1
PAD
OUTBUF
GND
DRAWN BY:
DATE:
REV.

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