TOTAL IONIZING DOSE TEST REPORT

No. 06T-RTSX32SU-D1N8F1(rev.1)
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 73 krad (Si) per 25-mA spec. Post 100 krad (Si) and after room temperature annealing: average I_{CCA} = 153.7 mA, and average I_{CCI} = 54.3 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/ and http://www.actel.com) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 81978 is irradiated to 60 krad; DUT 82036, 82050, and 82133 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D1N8F1
Quantity Tested	6
Serial Number	60 krad: 81978 100 krad: 82036, 82050, 82133
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

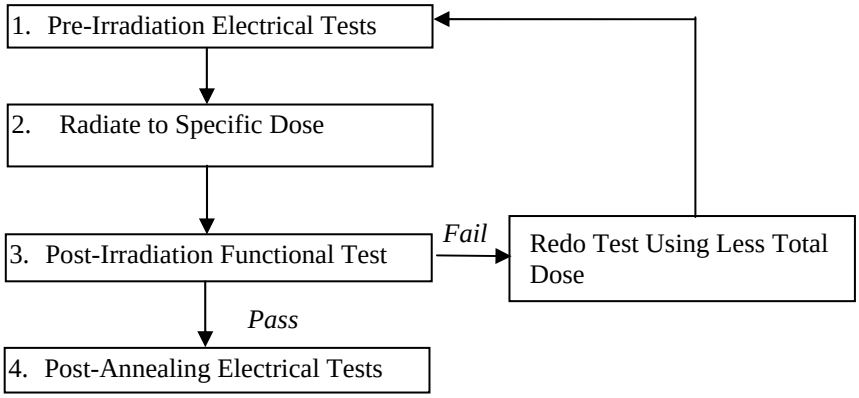


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs in both the 60-krad group and 100-krad group are bias-annealed for 15 days after the irradiation.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) are measured on twelve combinational nets listed in Table 2. The output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTR/YO0, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is probably due to the state changes during irradiation. However, this transition does not affect the functionality since each DUT passed the gross functionality test right after the irradiation.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
81978	60 krad	29	NA	60	NA
82036	100 krad	253	150	189	51
82050	100 krad	282	152	214	55
82133	100 krad	357	159	244	72

A semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 82133, the tolerance is extracted as 73 krad for 10-year mission.

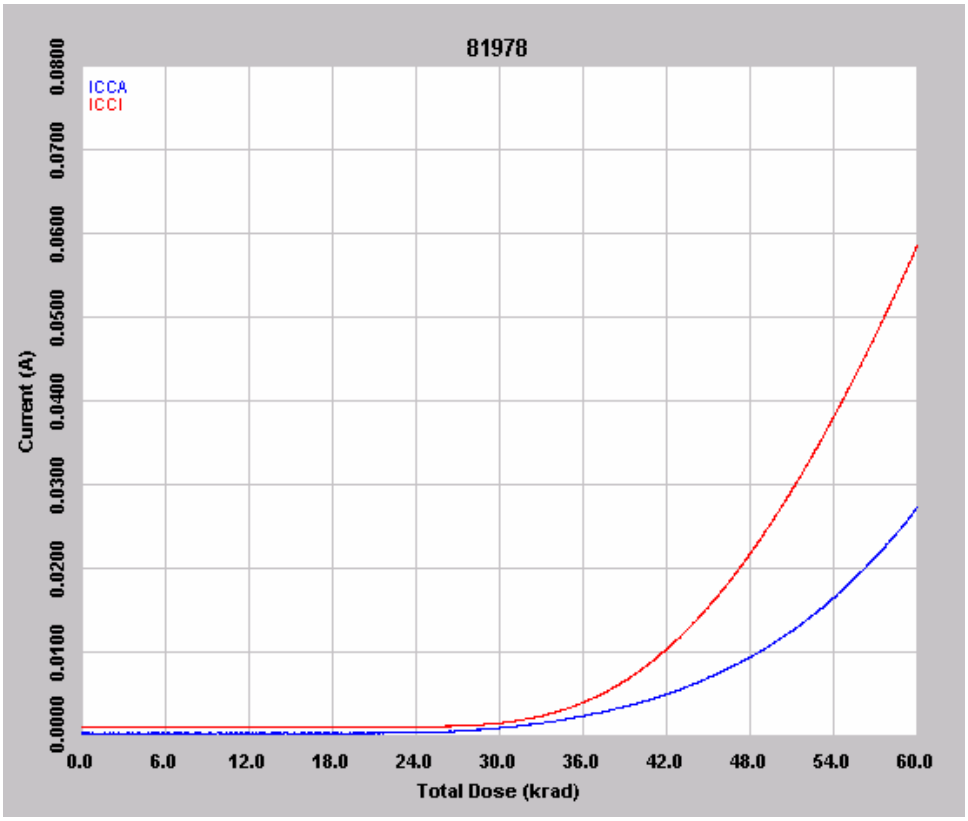


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 81978, 60 krad total dose

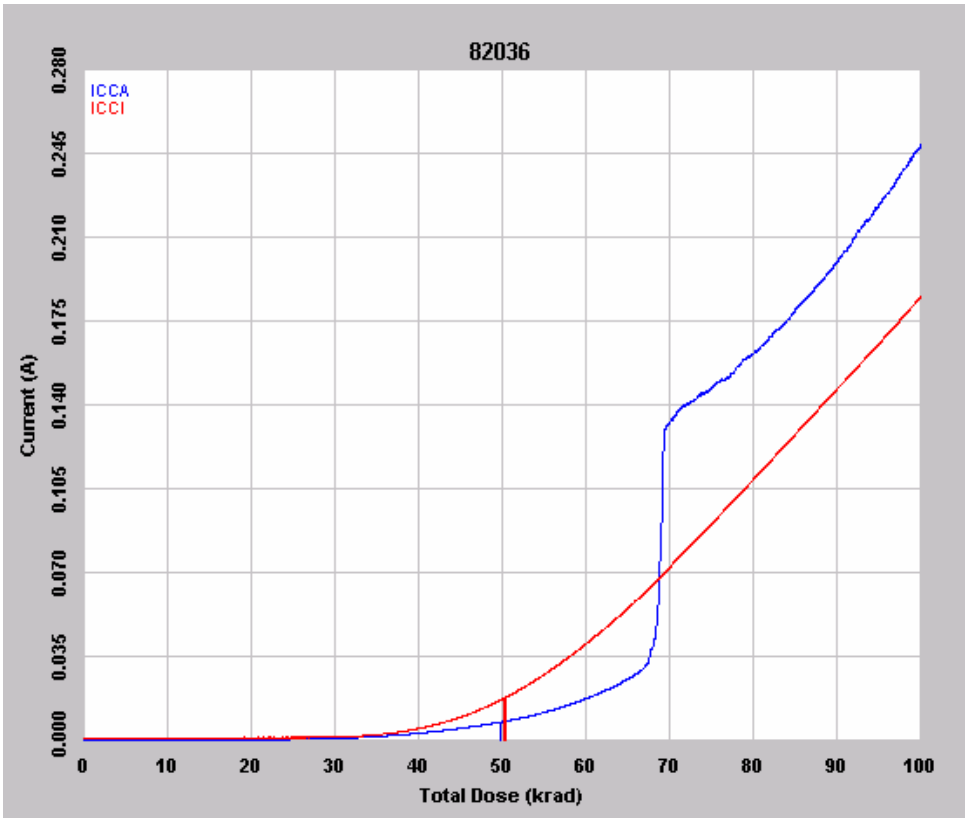


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 82036, 100 krad total dose

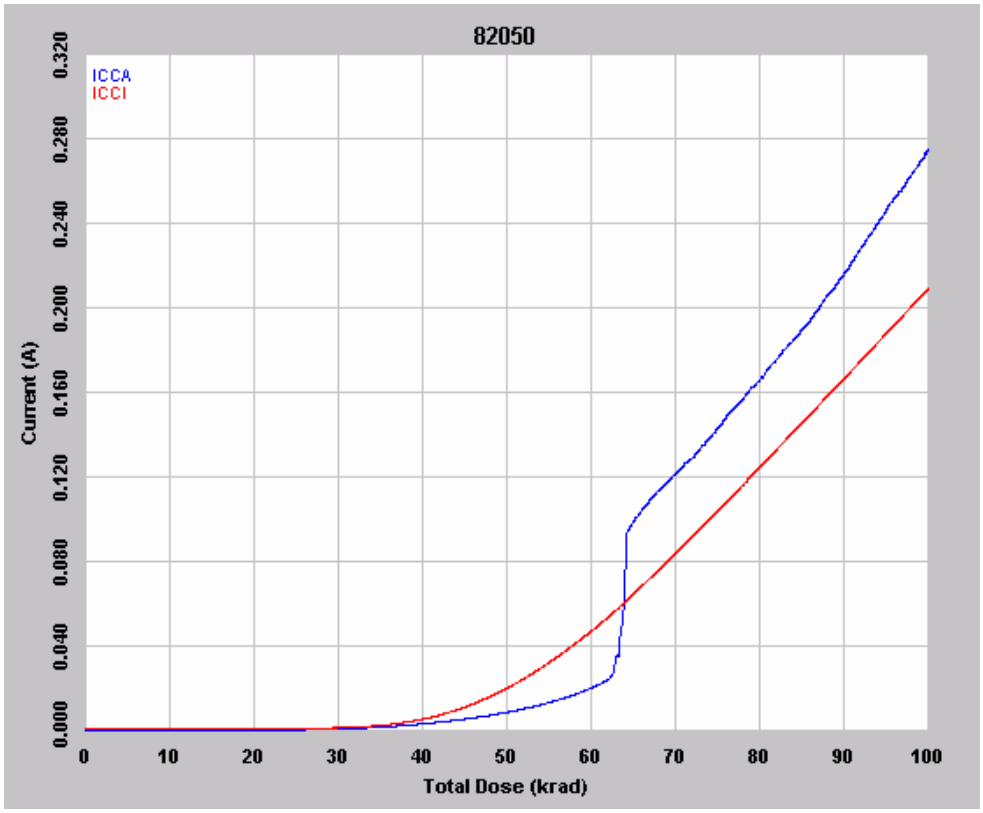


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 82050, 100 krad total dose

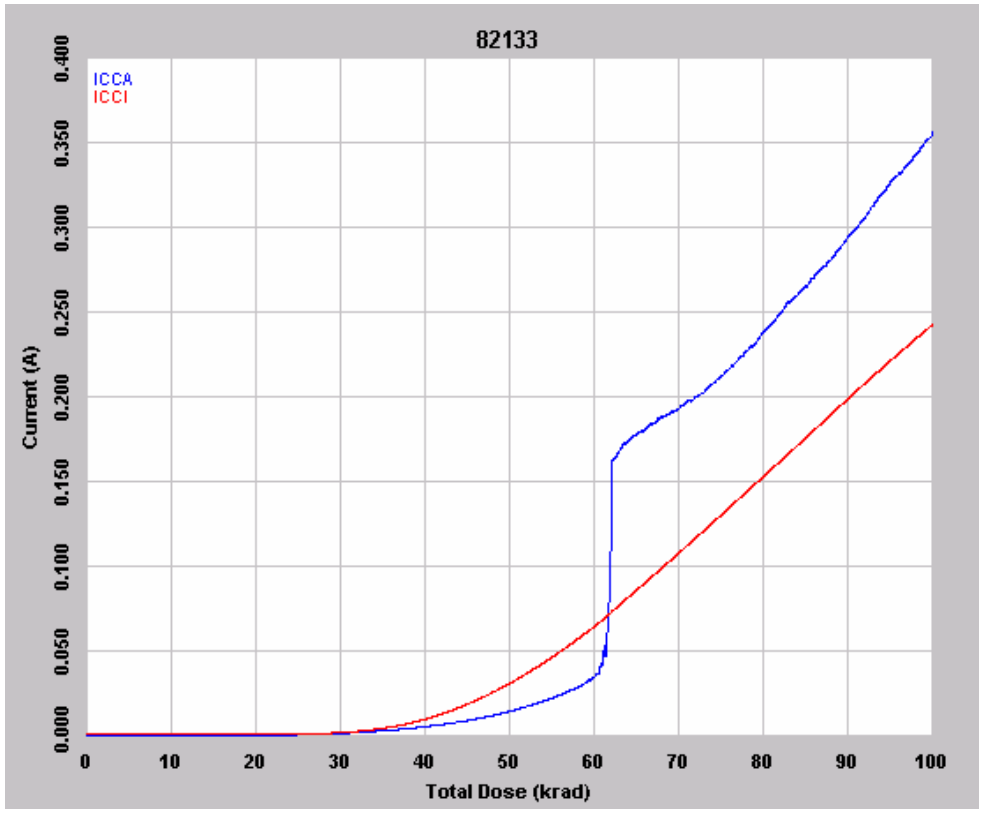


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 82133, 100 krad total dose

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA / QA0				DAH / QA0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
81978	60 krad	1.46	1.39	1.58	1.31	1.36	1.30	1.43	1.35
82036	100 krad	1.45	1.34	1.58	1.43	1.35	1.25	1.42	1.30
82050	100 krad	1.45	1.35	1.59	1.45	1.35	1.25	1.42	1.30
82133	100 krad	1.00	1.33	1.59	1.26	1.35	1.28	1.43	1.31

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR / YO0				ENCNTRH / YO0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
81978	60 krad	0.85	0.81	1.97	1.91	1.17	1.27	1.57	1.48
82036	100 krad	0.79	0.86	1.94	1.87	1.19	1.20	1.55	1.40
82050	100 krad	0.79	0.87	1.95	1.88	1.19	1.19	1.56	1.39
82133	100 krad	0.78	0.78	1.94	1.84	1.19	1.10	1.56	1.41

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0 / IDIO0				IDII1/ IDIO1			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
81978	60 krad	1.41	1.45	1.42	1.41	1.43	1.19	1.41	1.42
82036	100 krad	1.42	1.36	1.41	1.40	1.24	1.22	1.40	1.37
82050	100 krad	1.41	1.44	1.40	1.43	1.25	1.24	1.42	1.37
82133	100 krad	1.42	1.42	1.41	1.40	1.42	1.18	1.40	1.40

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2 / IDIO2				IDII3 / IDIO3			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
81978	60 krad	1.45	1.43	1.40	1.40	1.43	1.43	1.42	1.40
82036	100 krad	1.43	1.43	1.39	1.38	1.42	1.42	1.43	1.37
82050	100 krad	1.43	1.31	1.38	1.37	1.41	1.40	1.39	1.38
82133	100 krad	1.43	1.28	1.39	1.41	1.42	1.42	1.43	1.38

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4 / IDIO4				IDII5 / IDIO5			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
81978	60 krad	1.38	1.37	1.43	1.43	1.40	1.40	1.43	1.42
82036	100 krad	1.37	1.43	1.37	1.36	1.38	1.39	1.40	1.40
82050	100 krad	1.38	1.36	1.42	1.36	1.38	1.38	1.41	1.41
82133	100 krad	1.40	1.37	1.38	1.42	1.40	1.40	1.43	1.42

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6 / IDIO6				IDII7 / IDIO7			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
81978	60 krad	1.36	1.42	1.40	1.41	1.44	1.44	1.40	1.43
82036	100 krad	1.37	1.40	1.39	1.43	1.42	1.42	1.39	1.40
82050	100 krad	1.42	1.40	1.38	1.40	1.42	1.40	1.39	1.39
82133	100 krad	1.36	1.38	1.39	1.39	1.44	1.42	1.39	1.41

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
81978	60 krad	0.143	0.144	0.222	0.222	0.279	0.280	0.501	0.500	0.955	0.955
82036	100 krad	0.143	0.143	0.221	0.222	0.279	0.279	0.499	0.500	0.951	0.953
82050	100 krad	0.143	0.143	0.221	0.223	0.280	0.280	0.500	0.501	0.954	0.956
82133	100 krad	0.139	0.140	0.217	0.217	0.273	0.274	0.488	0.490	0.925	0.931

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
81978	60 krad	4.82	4.81	4.73	4.73	4.59	4.58	4.02	4.00	2.64	2.59
82036	100 krad	4.82	4.81	4.73	4.73	4.58	4.58	4.02	4.00	2.64	2.55
82050	100 krad	4.82	4.82	4.74	4.73	4.59	4.58	4.03	4.01	2.68	2.60
82133	100 krad	4.82	4.81	4.73	4.73	4.59	4.58	4.02	3.99	2.65	2.53

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage. In every case the DUT passes the 10% degradation criterion.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (ns)	Post-Annealing (ns)	Degradation
81978	60 krad	531	536	0.85%
82036	100 krad	522	526	0.86%
82050	100 krad	516	525	1.75%
82133	100 krad	517	525	1.65%

F. Transition Time

Figures 6 to 13 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

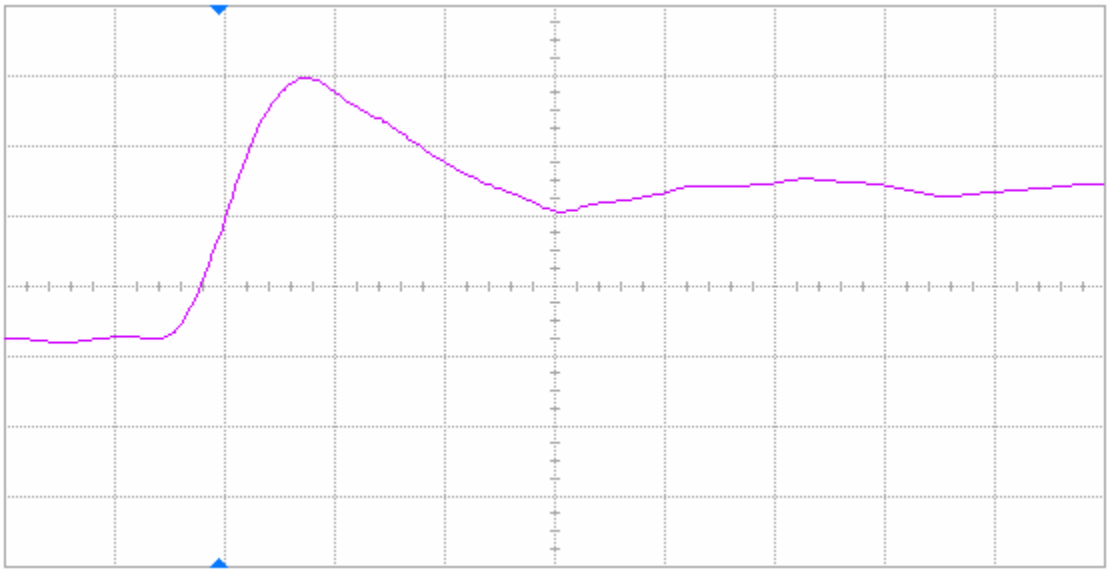


Figure 6(a) DUT 81978 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

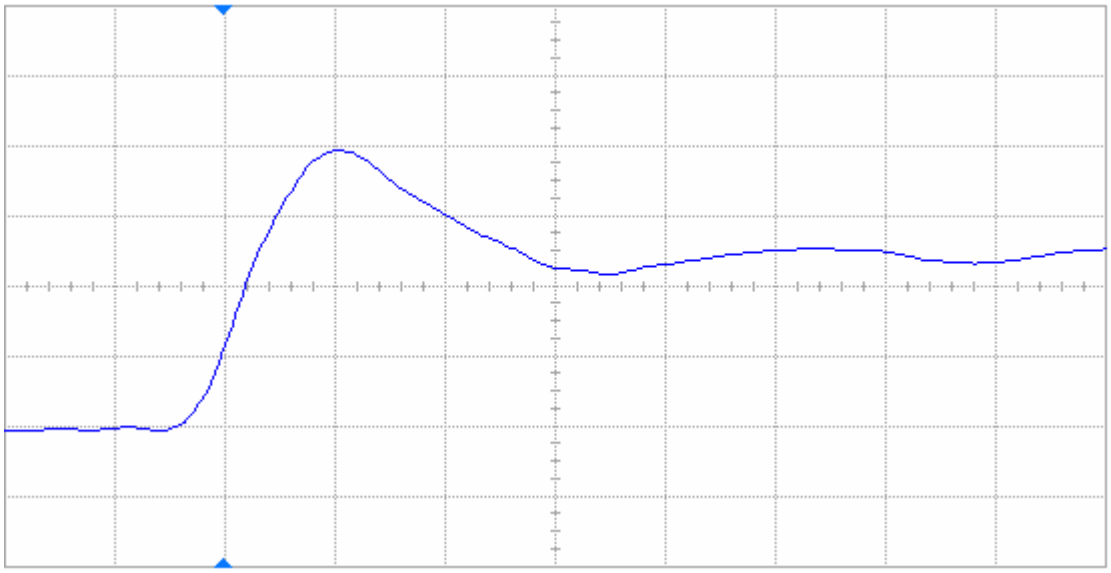


Figure 6(b) DUT 81978 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

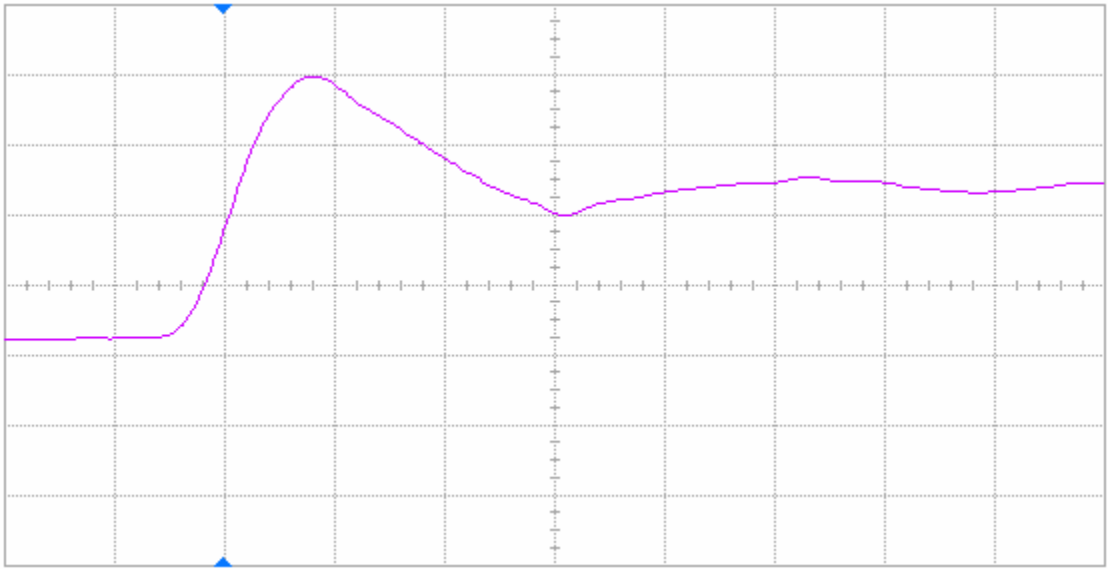


Figure 7(a) DUT 82036 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

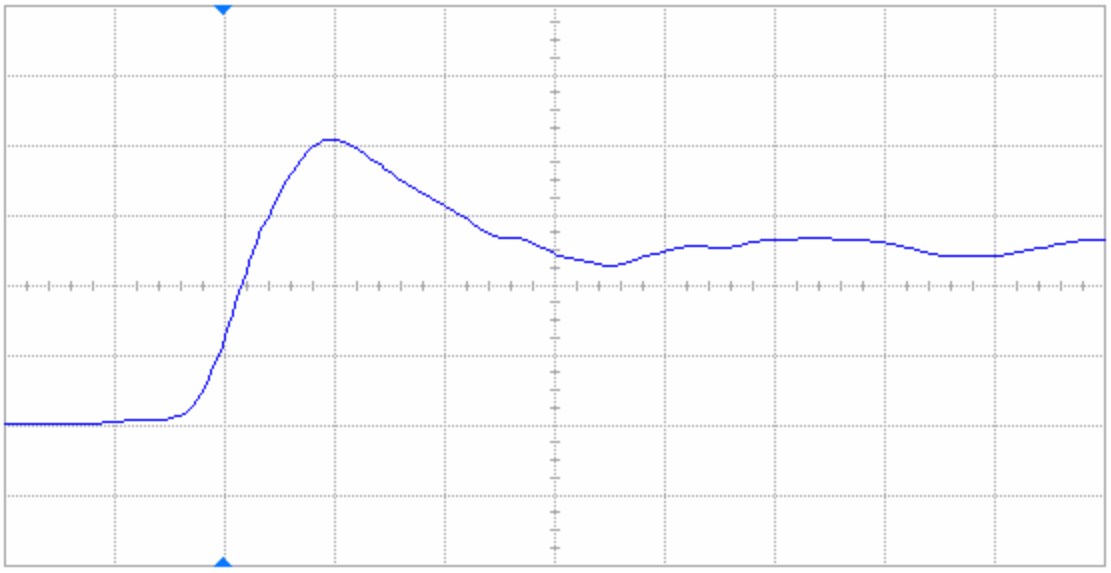


Figure 7(b) DUT 82036 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

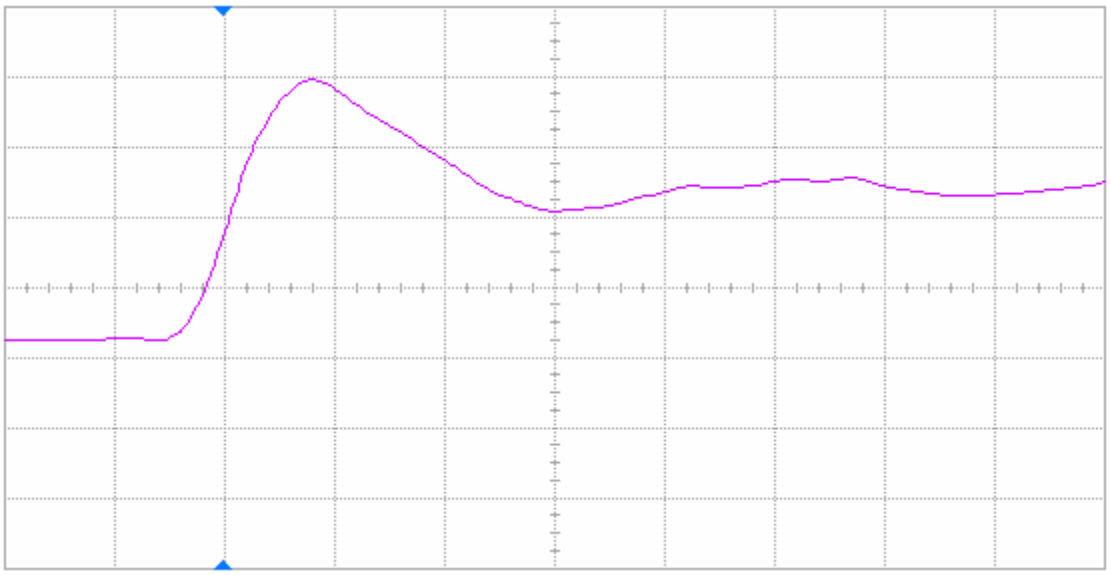


Figure 8(a) DUT 82050 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

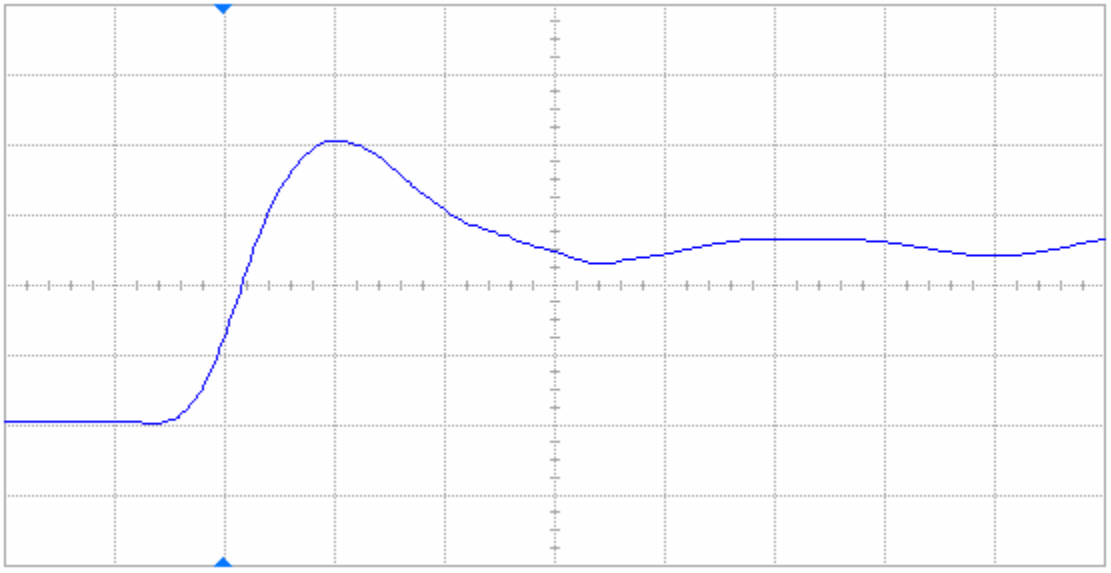


Figure 8(b) DUT 82050 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

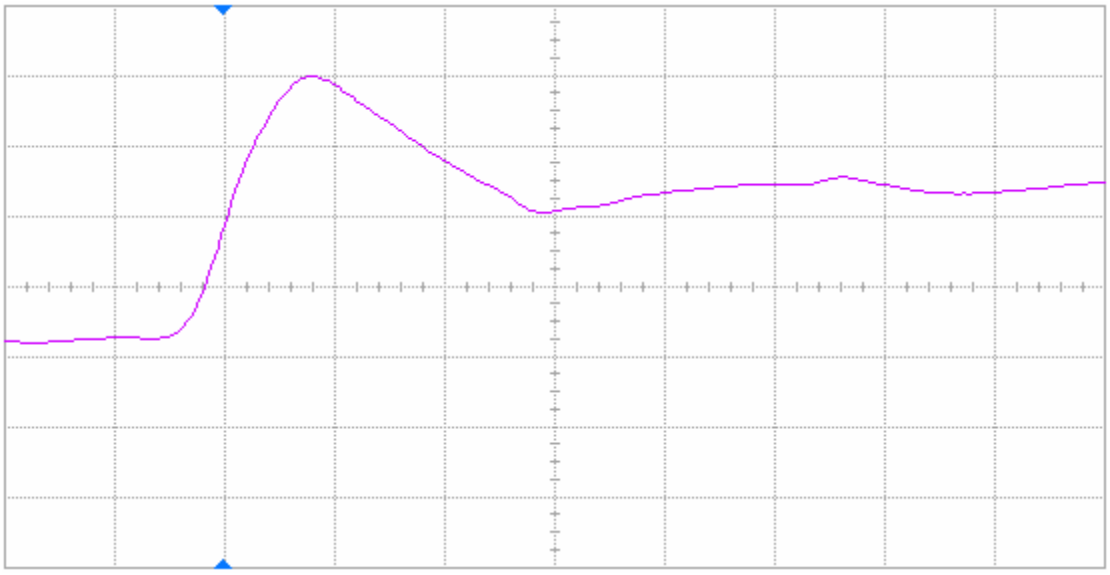


Figure 9(a) DUT 82133 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

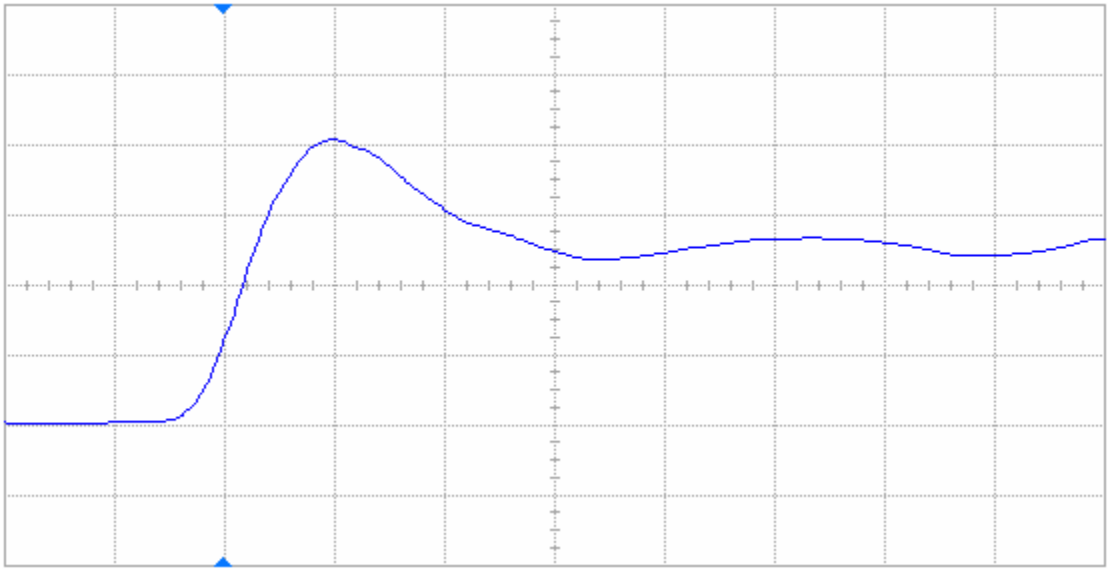


Figure 9(b) DUT 82133 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

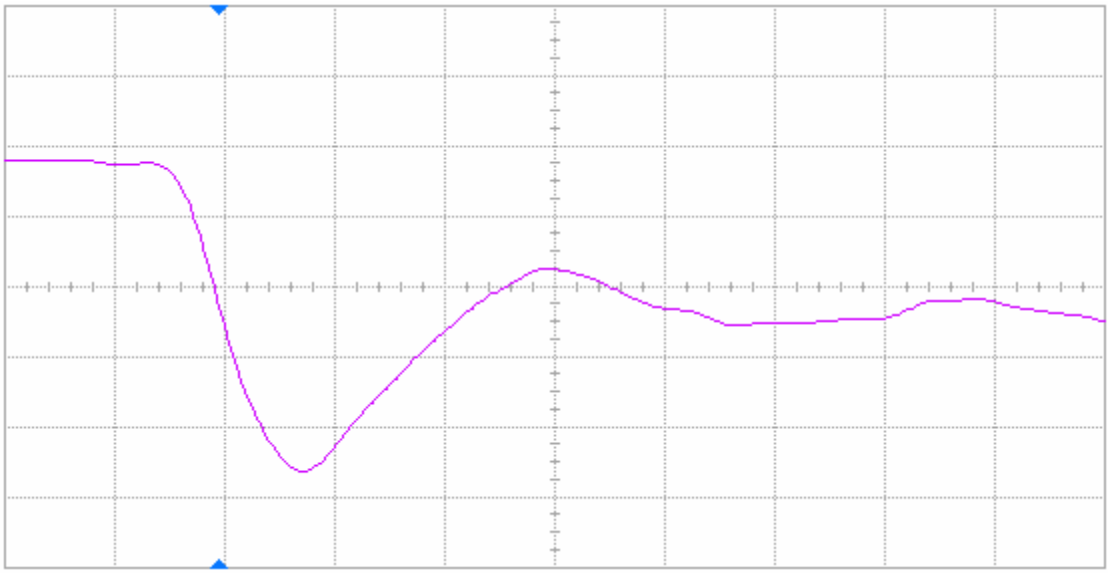


Figure 10(a) DUT 81978 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

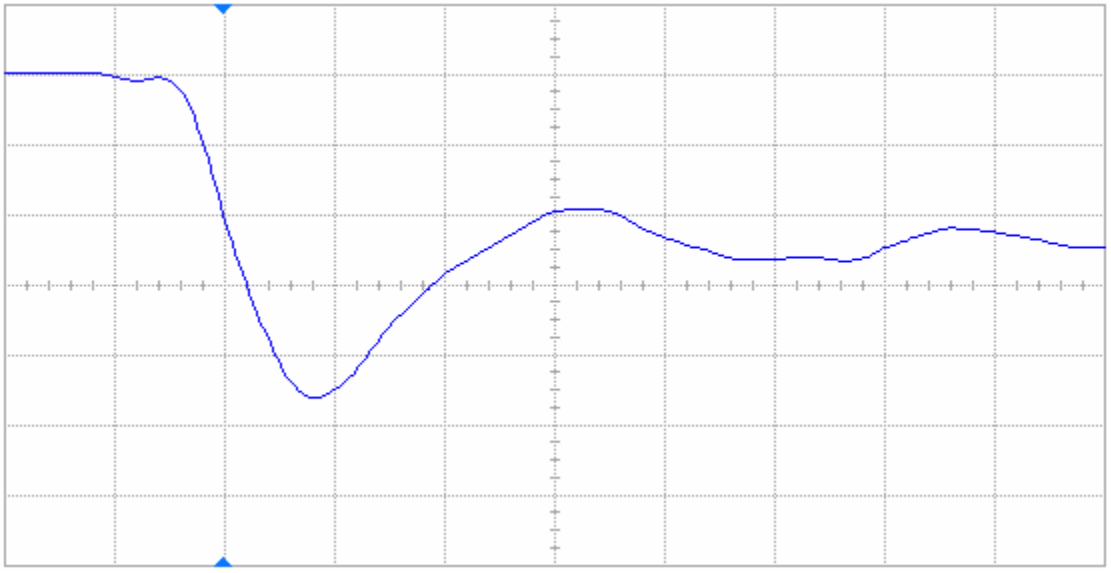


Figure 10(b) DUT 81978 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

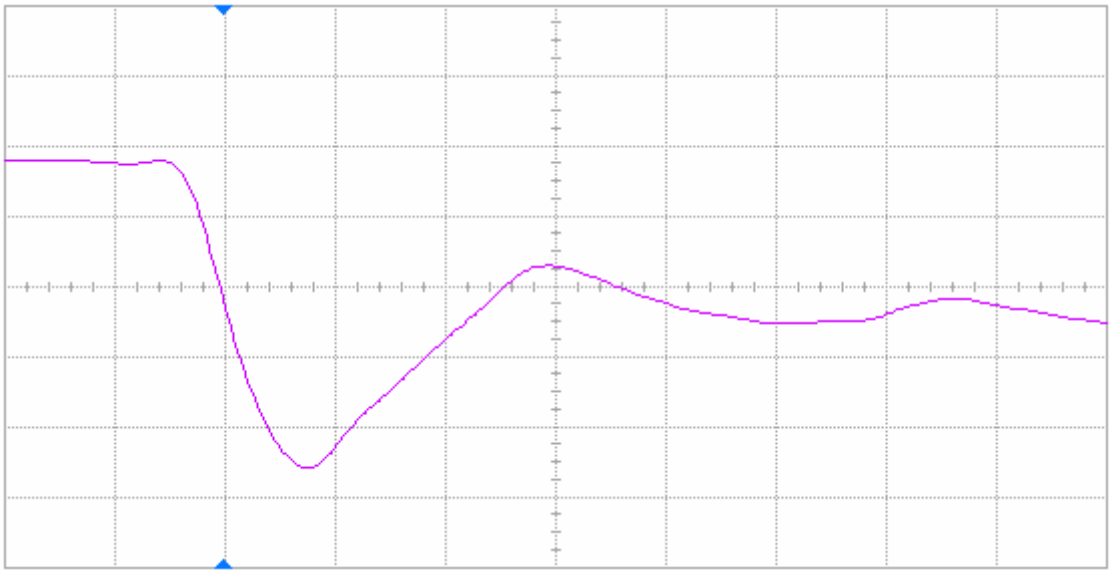


Figure 11(a) DUT 82036 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

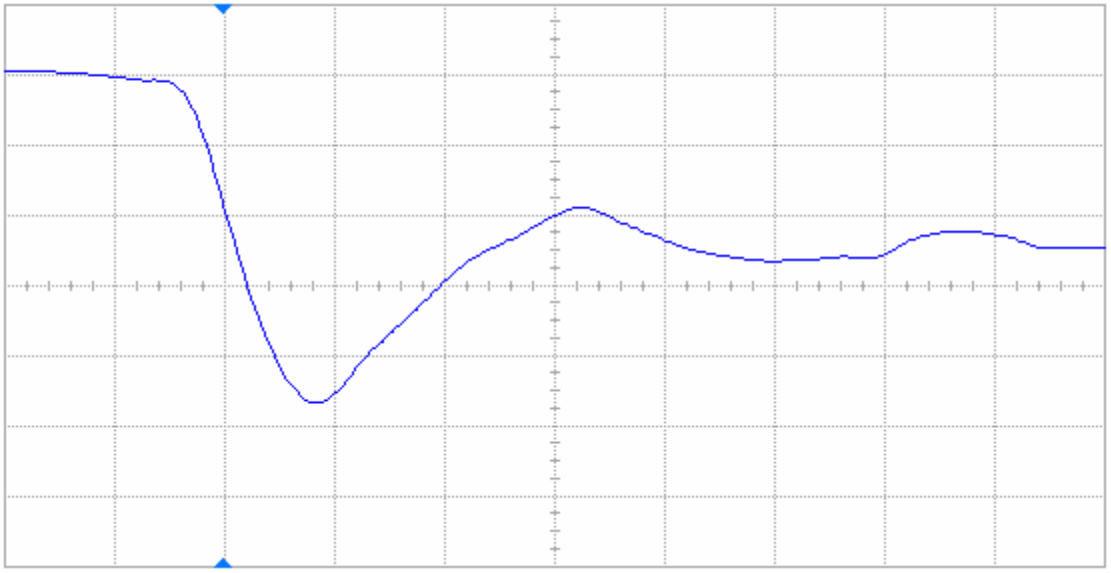


Figure 11(b) DUT 82036 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

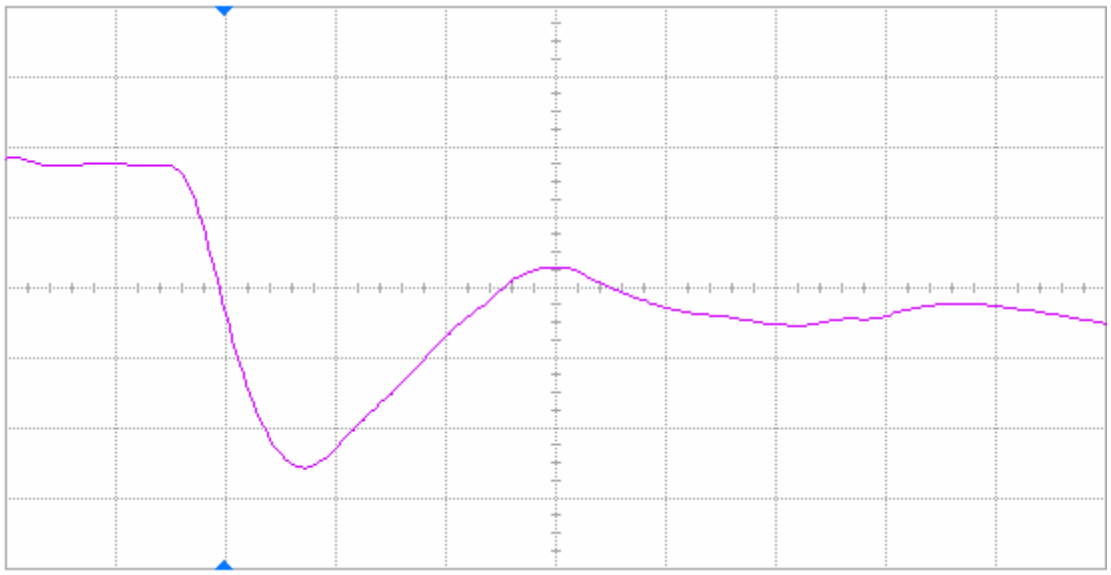


Figure 12(a) DUT 82050 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

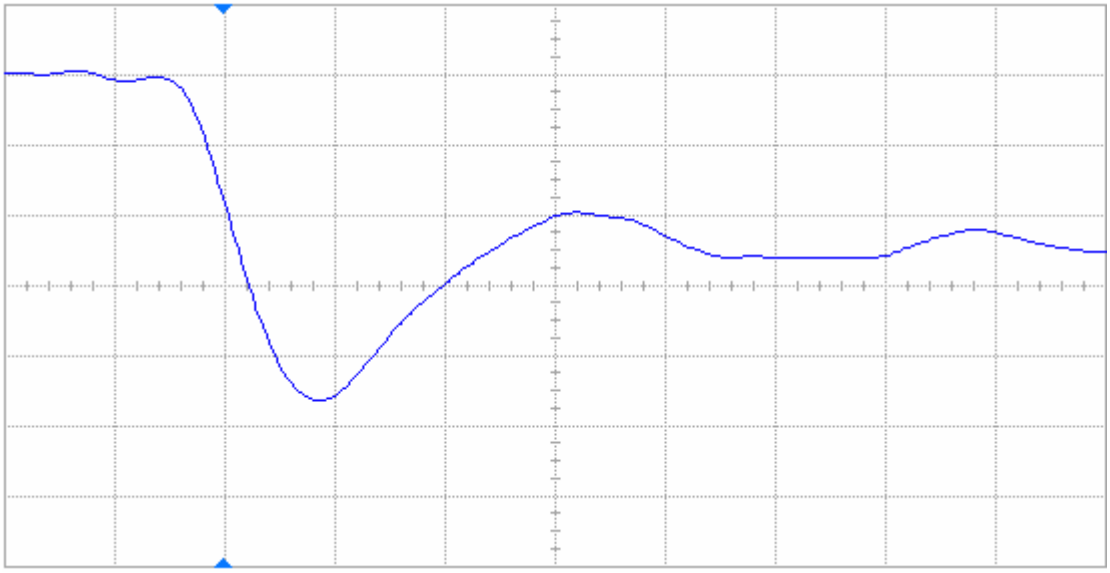


Figure 12(b) DUT 82050 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

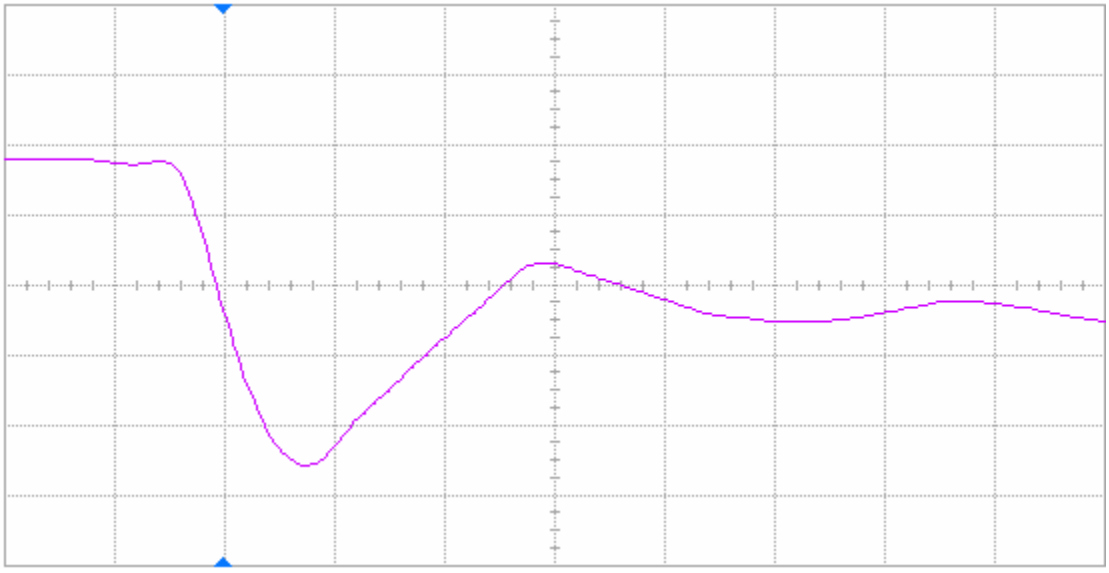


Figure 13(a) DUT 82133 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

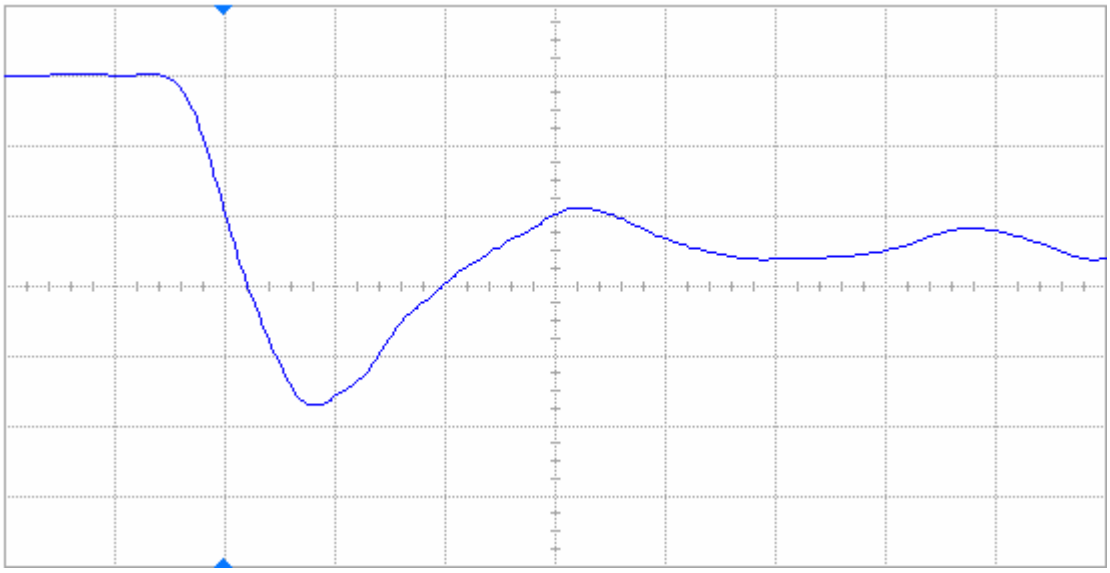
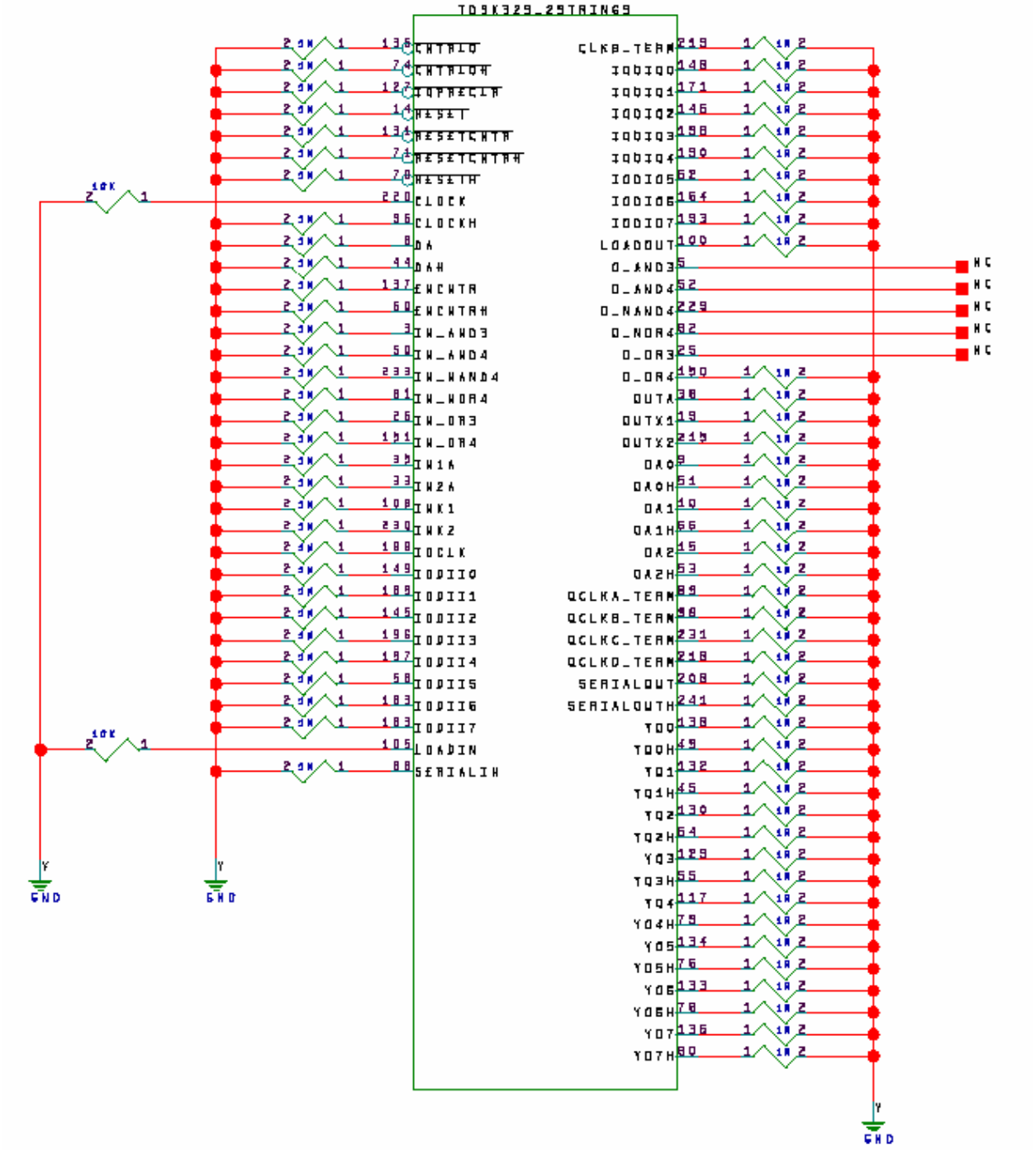
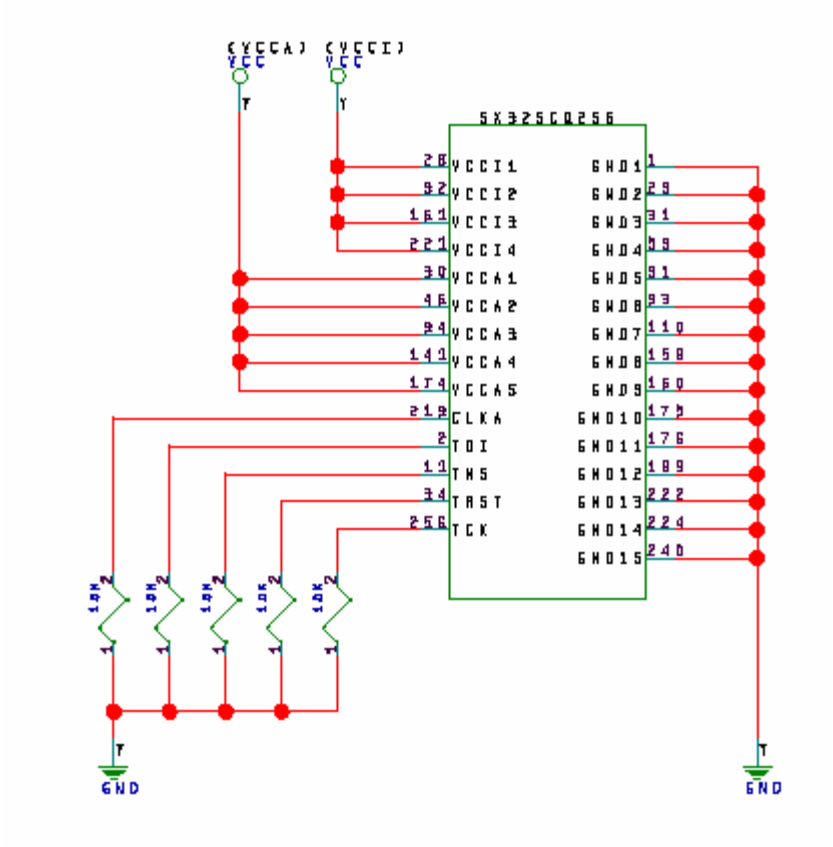


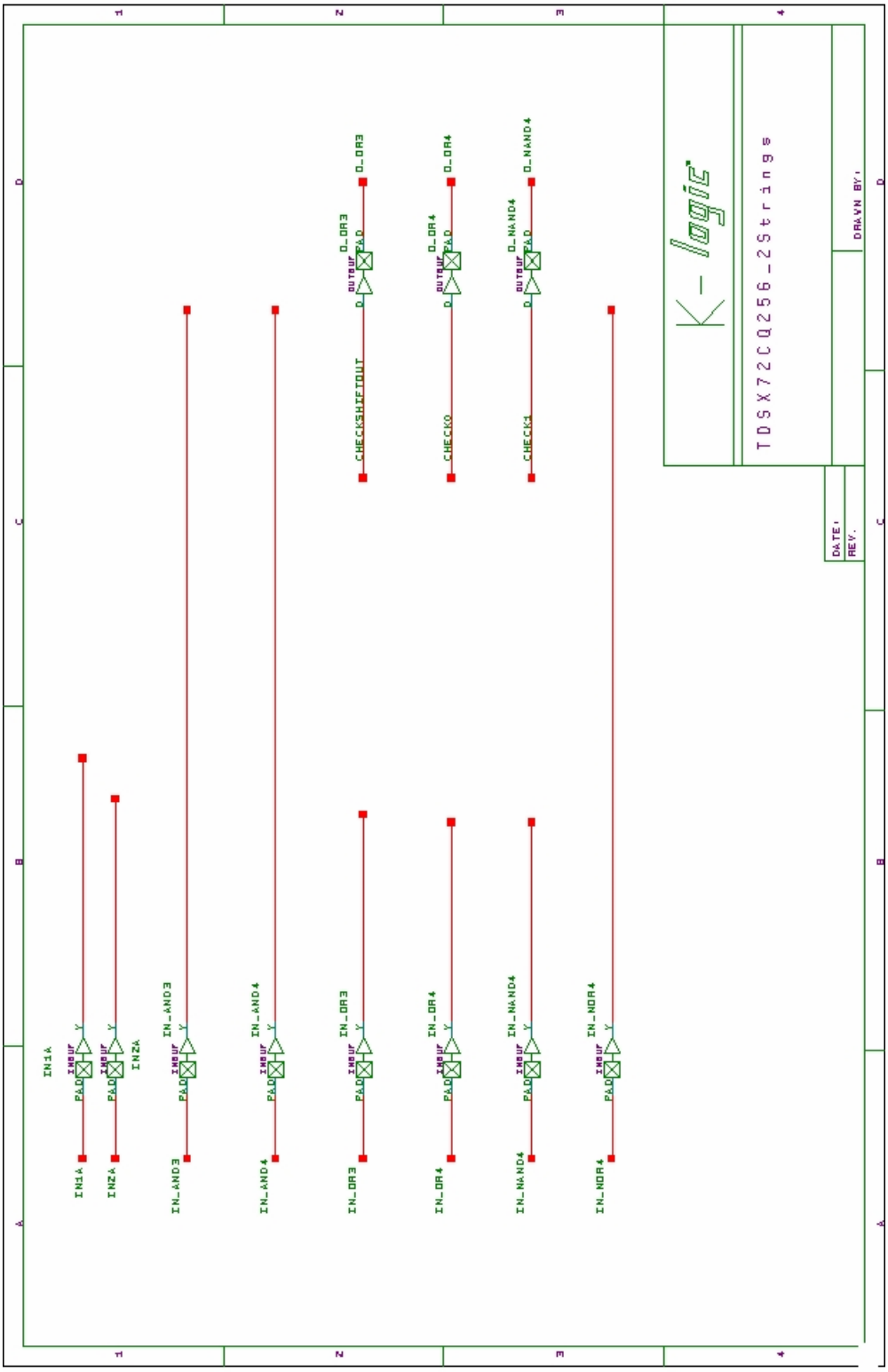
Figure 13(b) DUT 82133 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

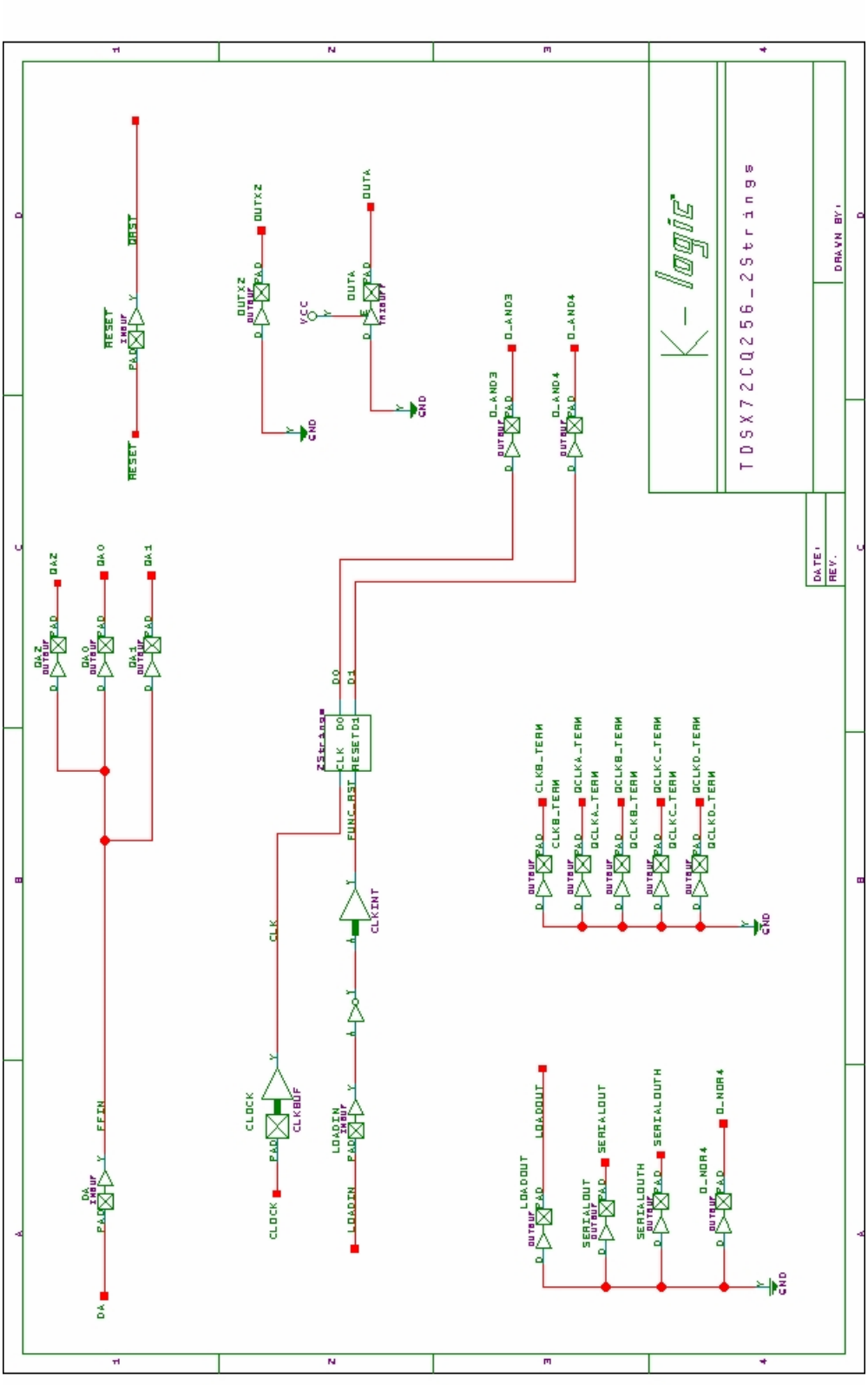
Appendix A DUT Bias

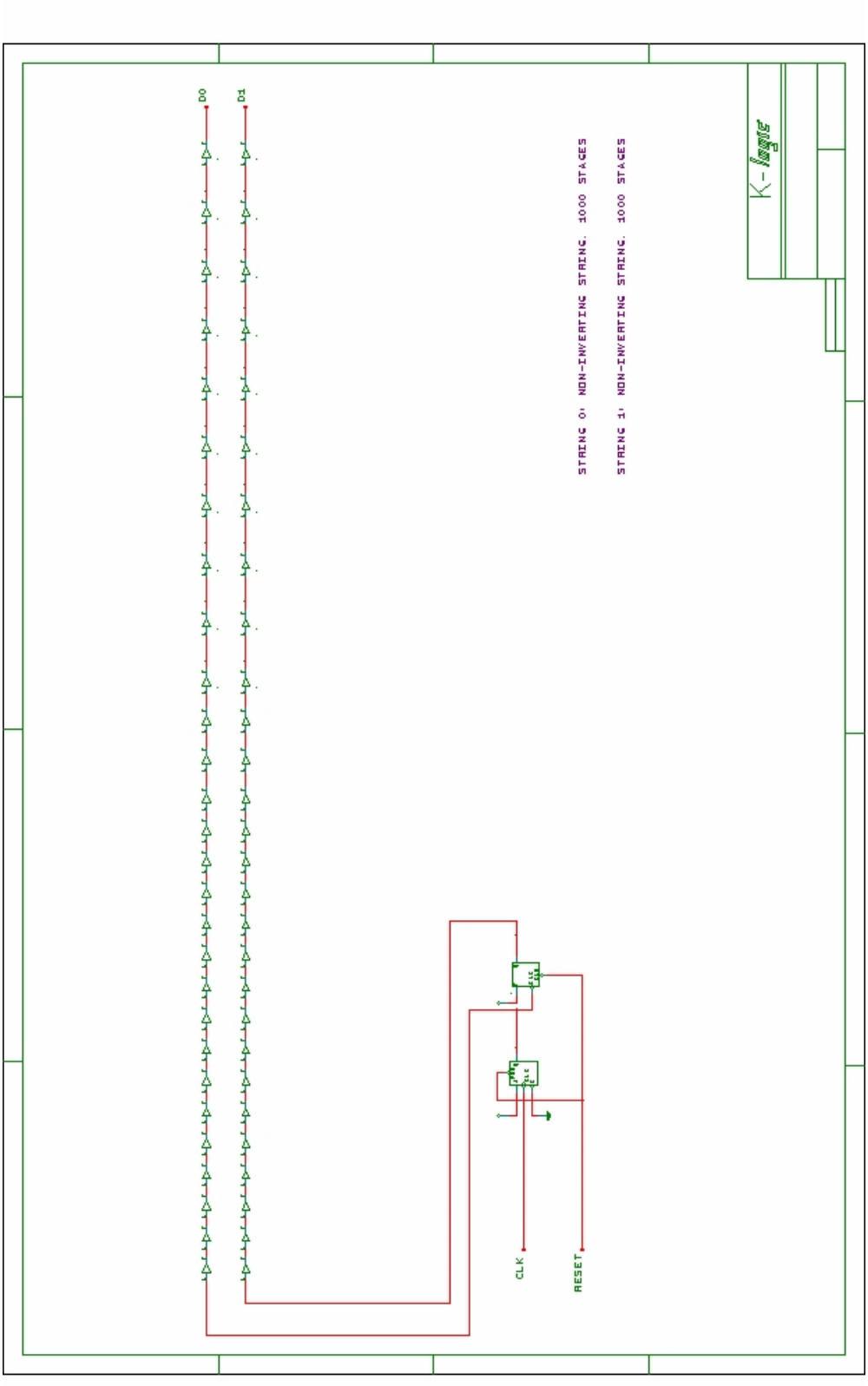



(VCCA)
(VCCI)
VCC
VCC
5X325CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
CLKA
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
10K
10K
10K
10K
10K
GND
GND

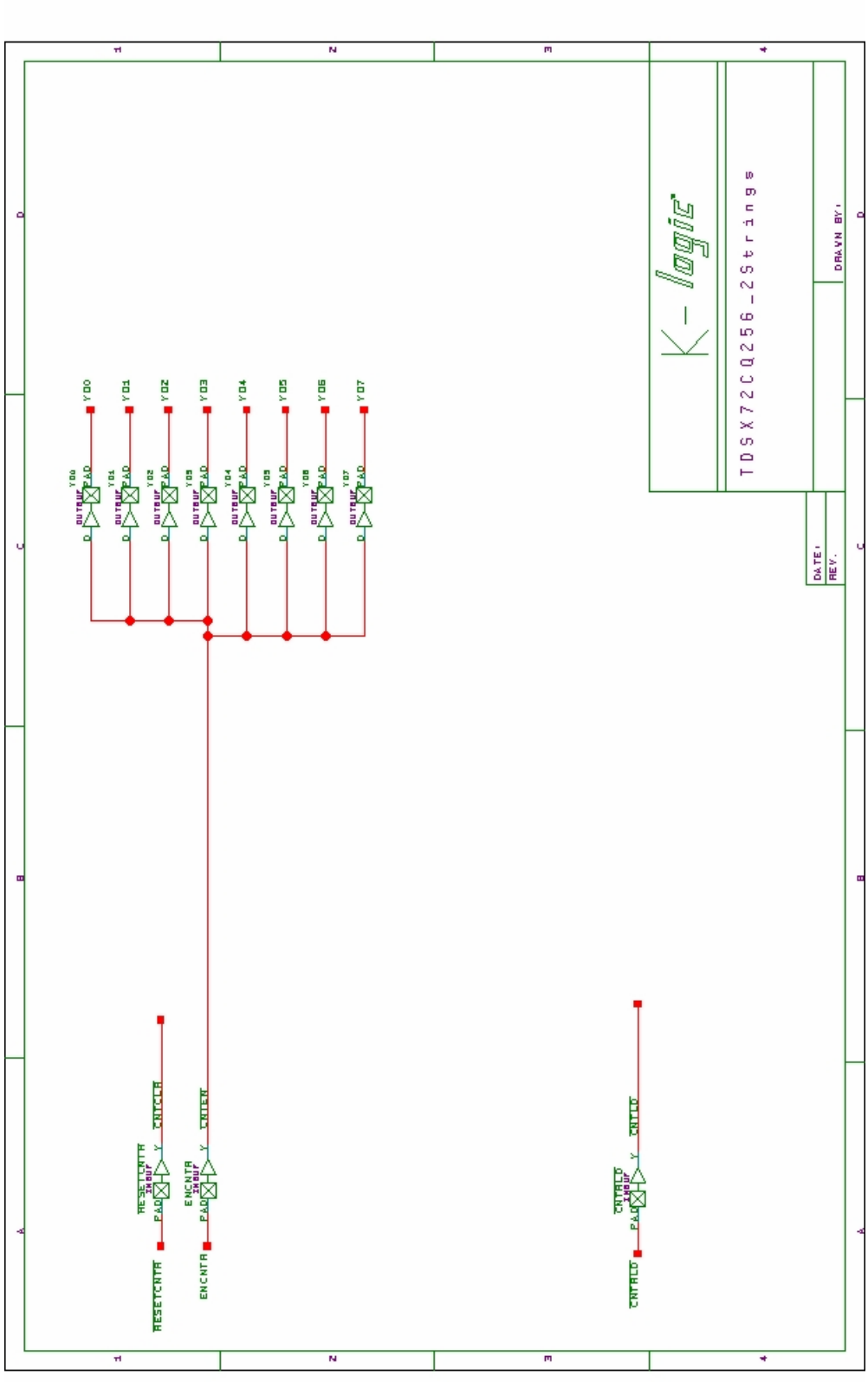
APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

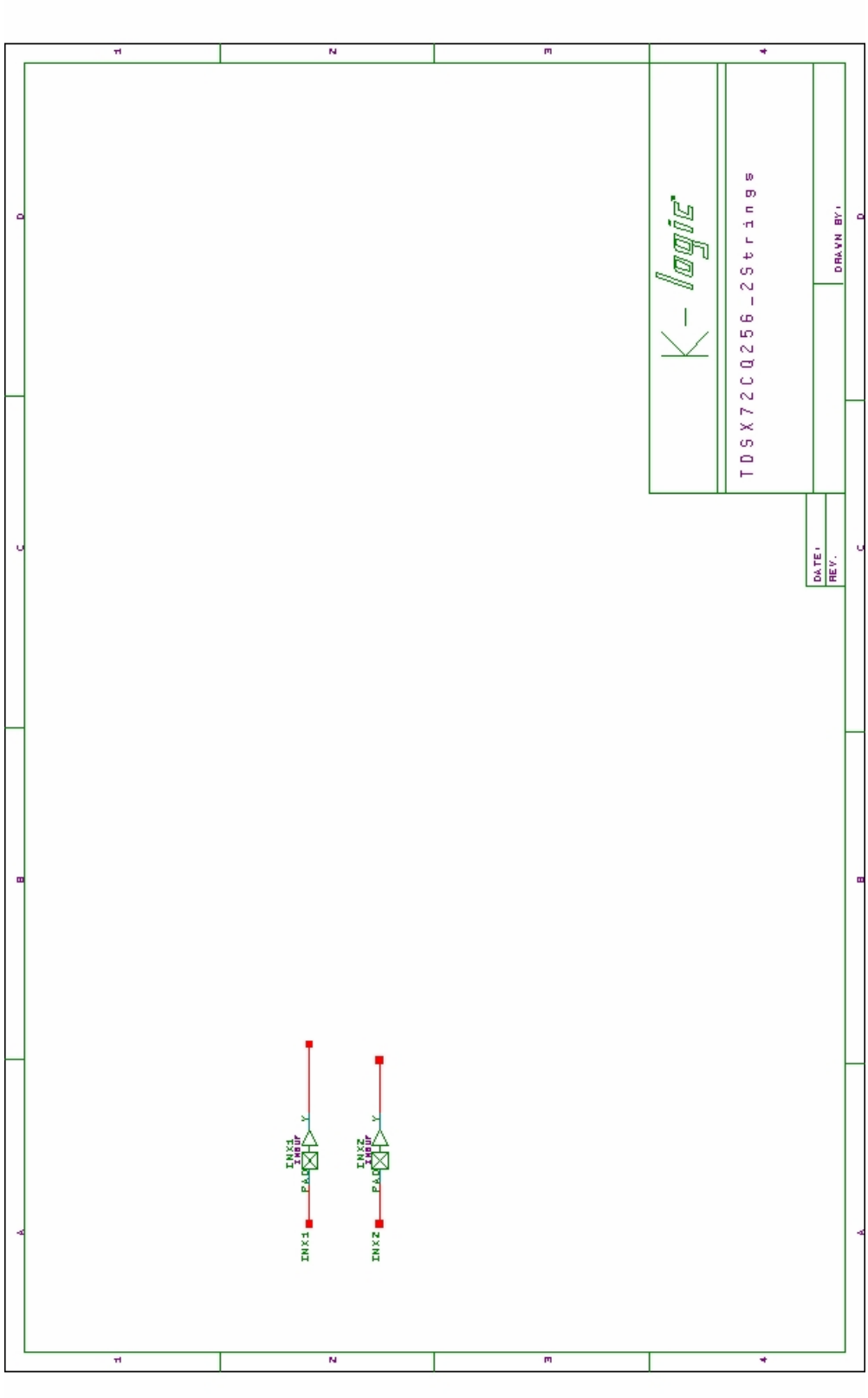


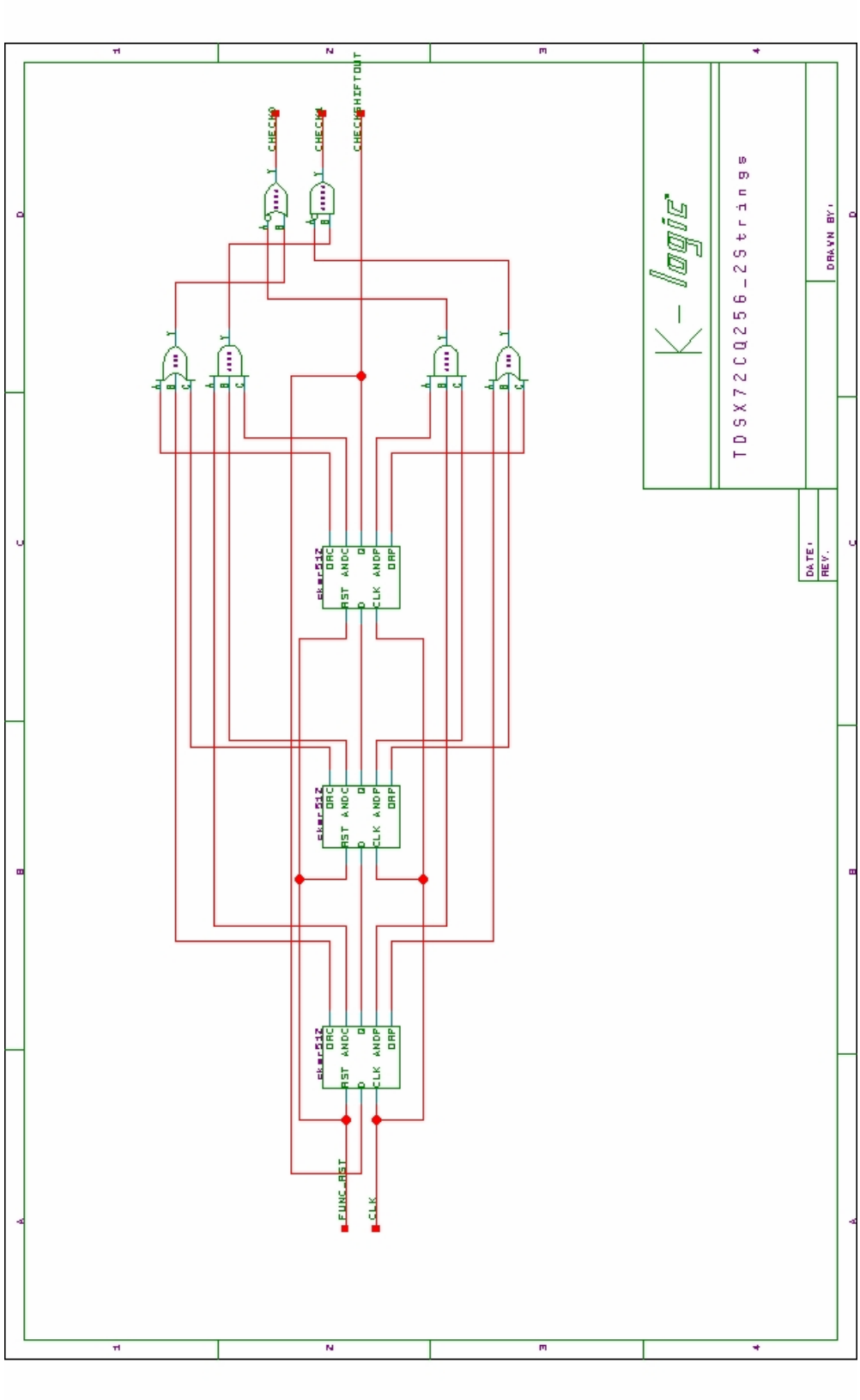

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
CLOCK
CLKBUF
LOADIN
CLK
CLKINT
2Strings
CLK DO
RESET D1
DO
D1
FUNC_RST
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

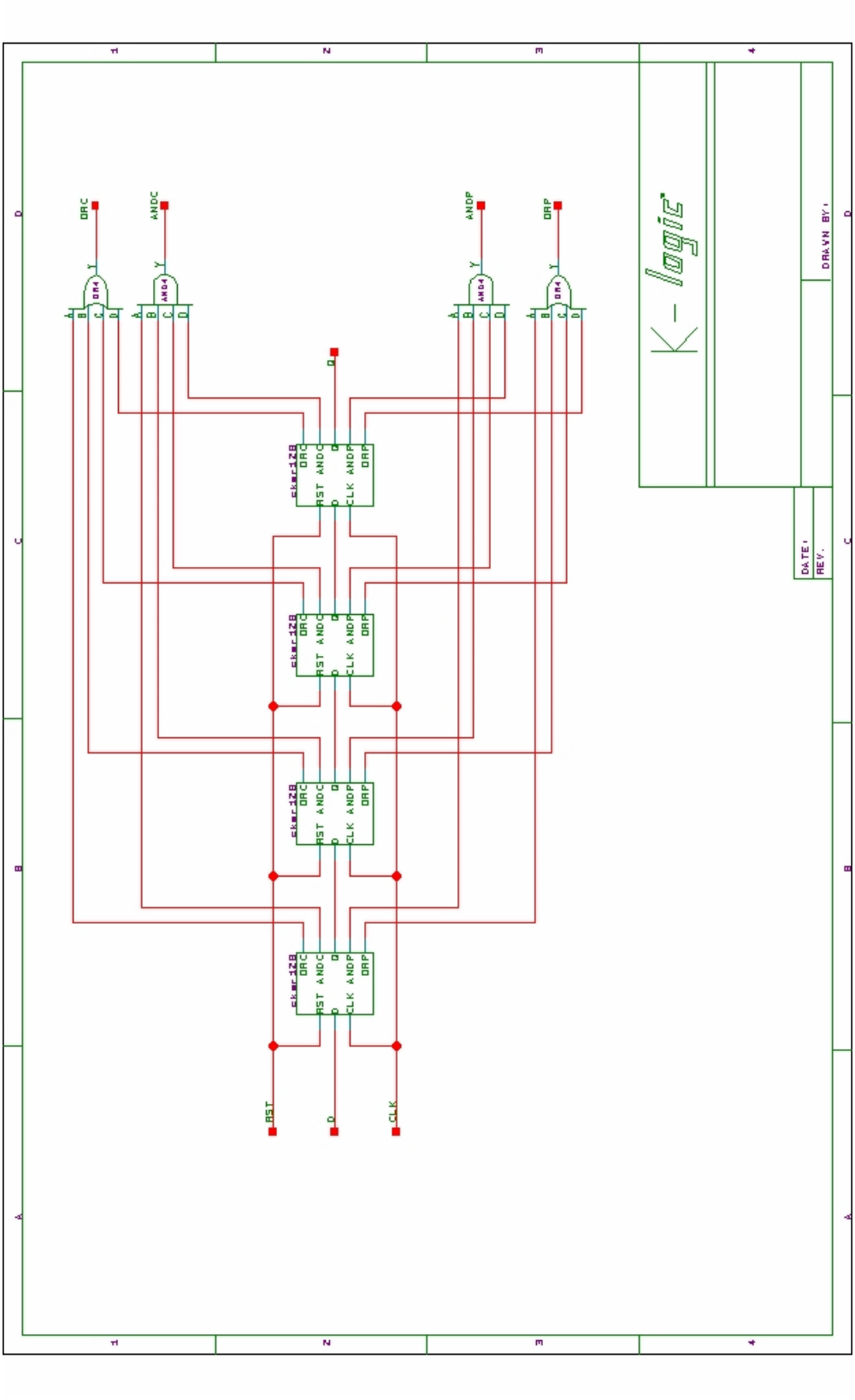

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-Logic
CLK
RESET

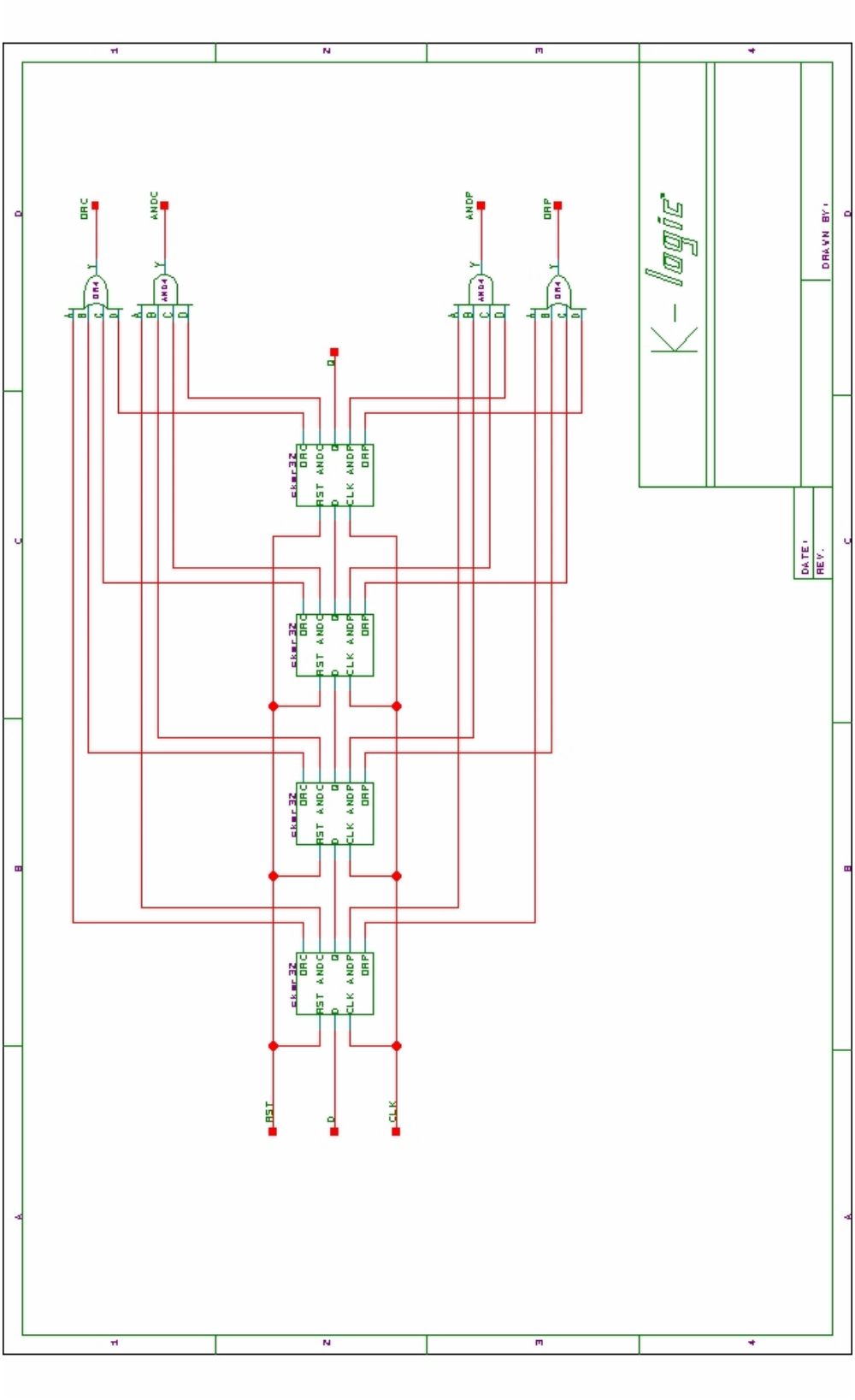

K- logic
T D A C T 3 5 X C Q \ B U F 5 0 N I N V
DRAWN BY: A B K
DATE:
REV:
Y:PRESERVE

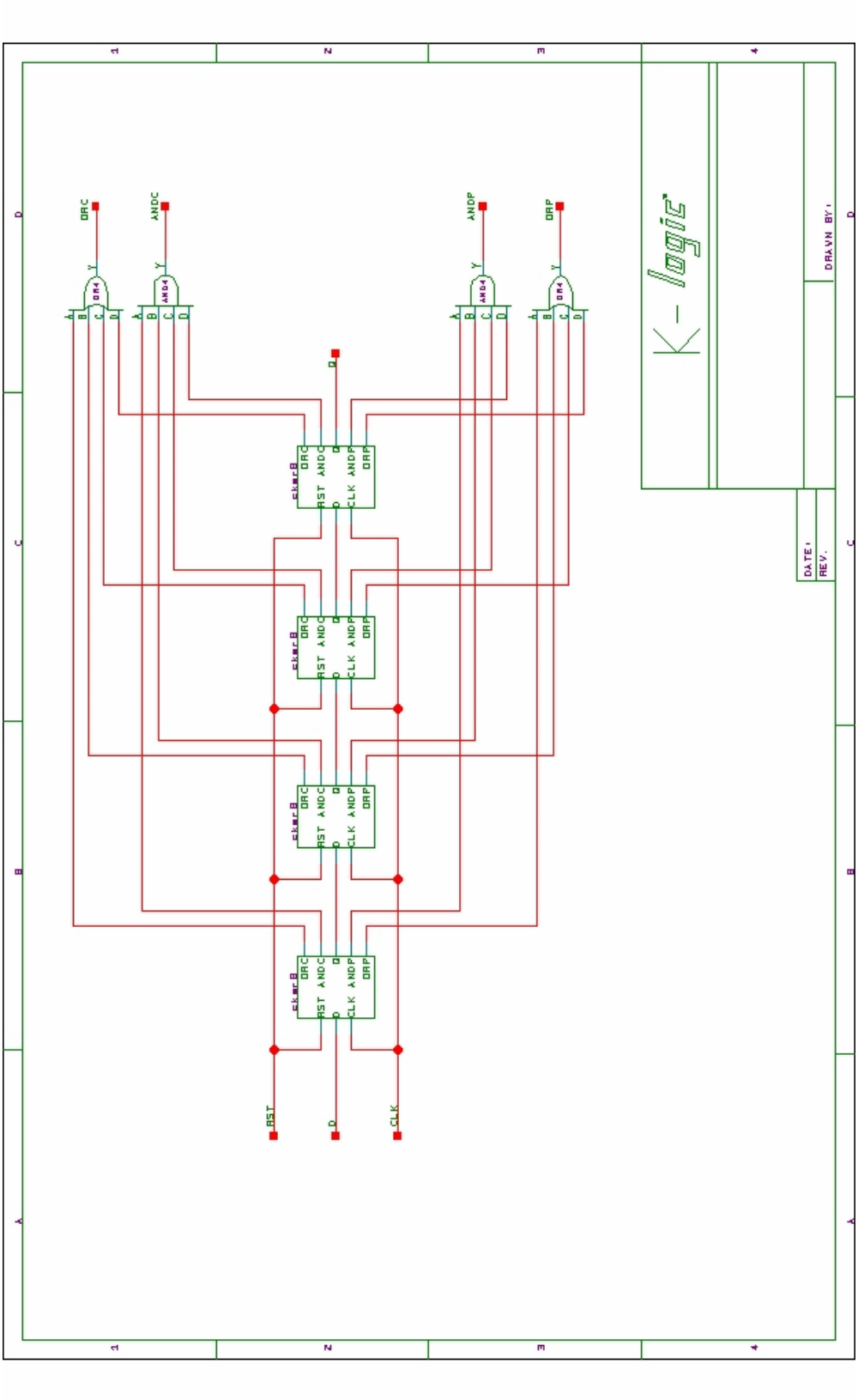

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRLD
CNTCLR
CNTEN
CNTLD

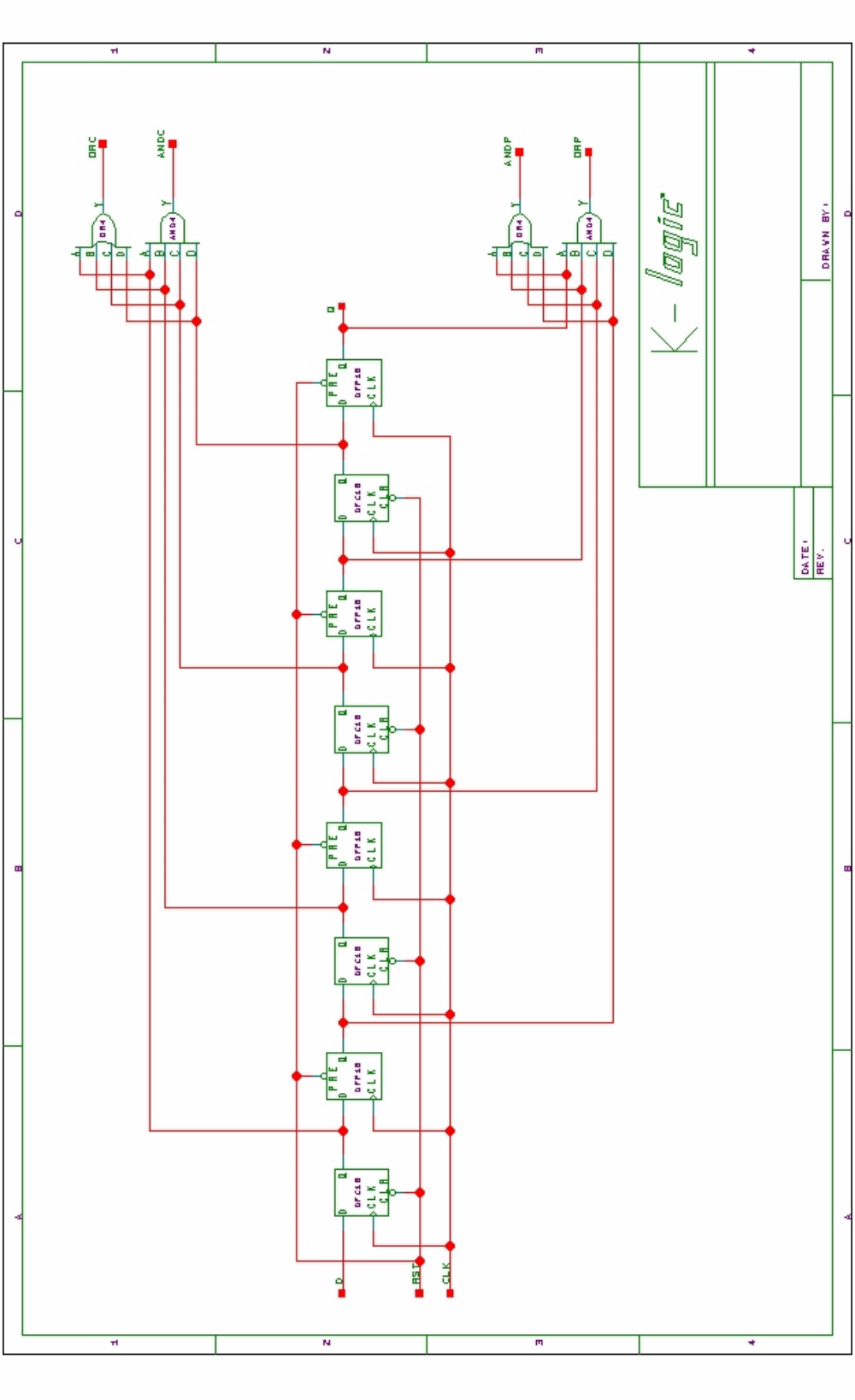

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

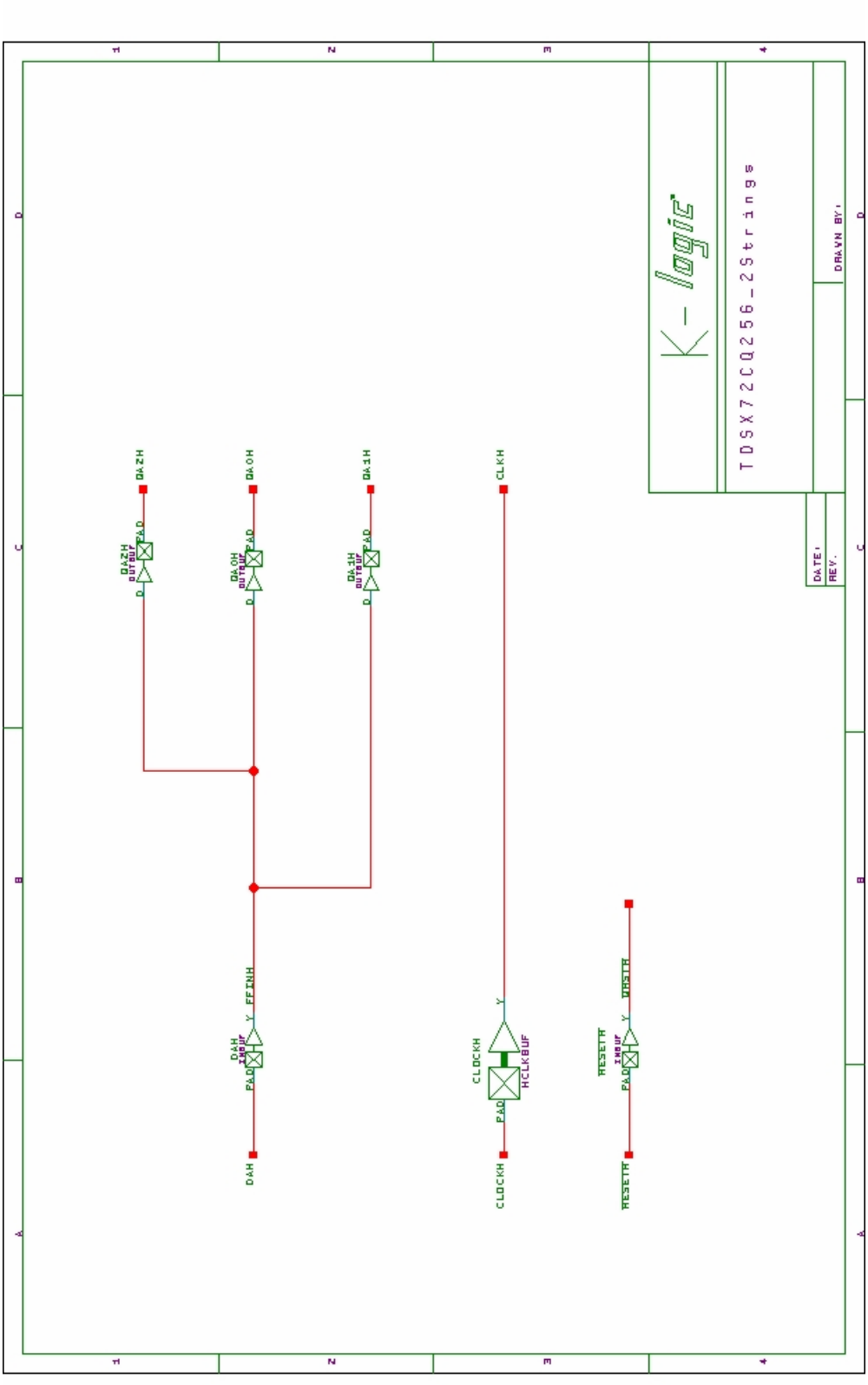

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
CHECKSHIFTOUT
CHECK0
CHECK1
FUNC_RST
CLK

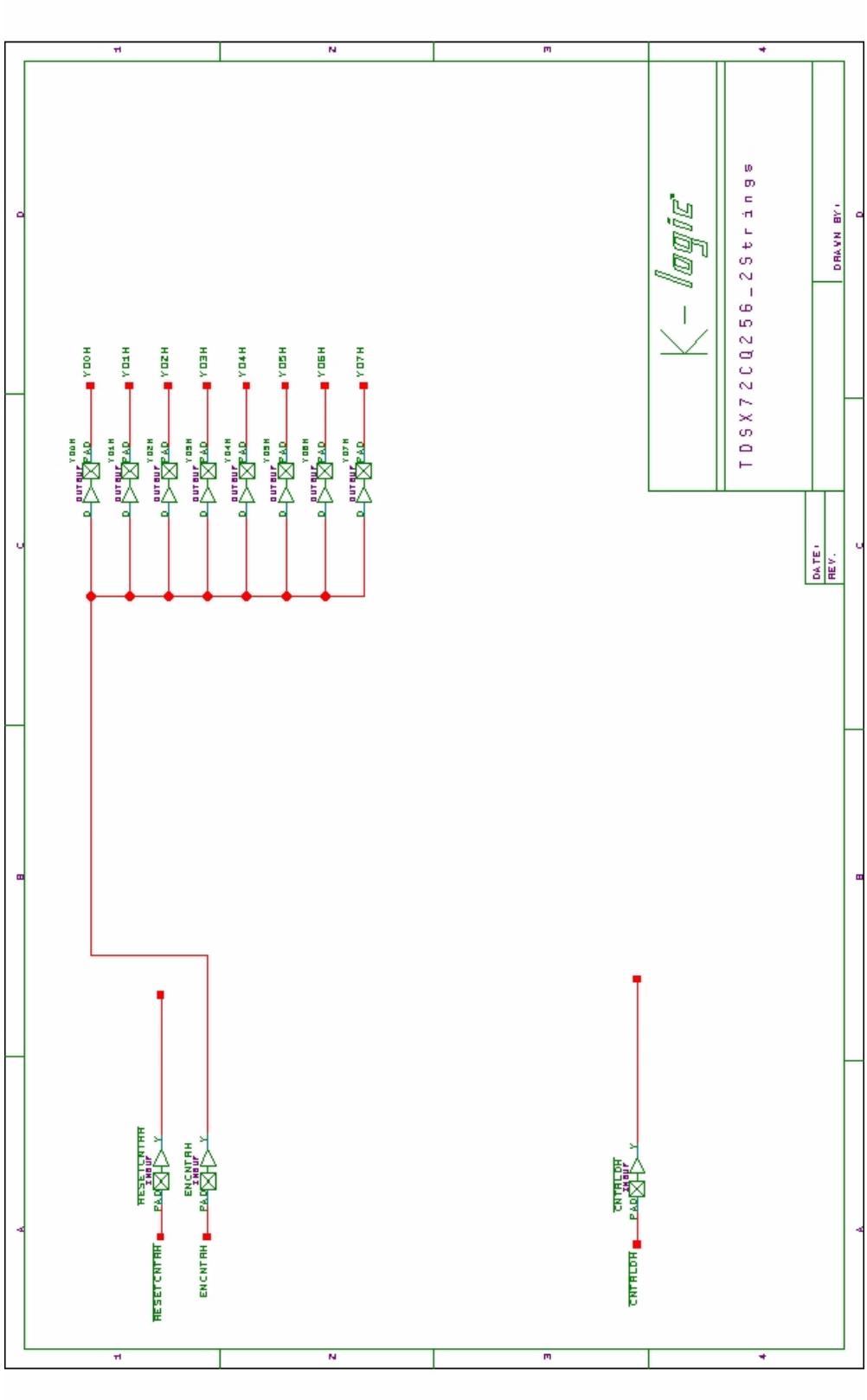

DRC
ANDC
ANDP
DRP
K- logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

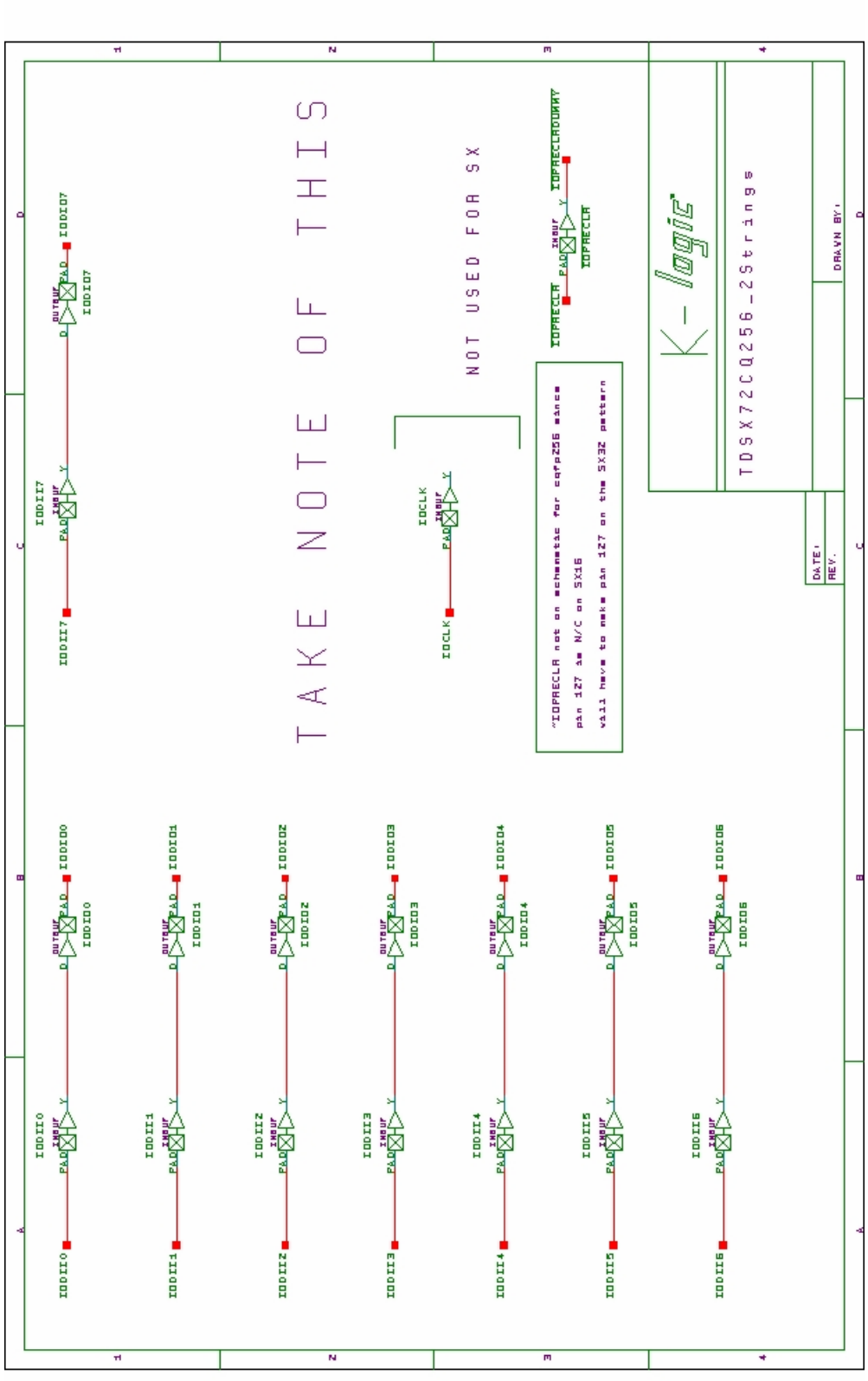

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDP
DRP
AND4
OR4
RST
D
CLK
Q

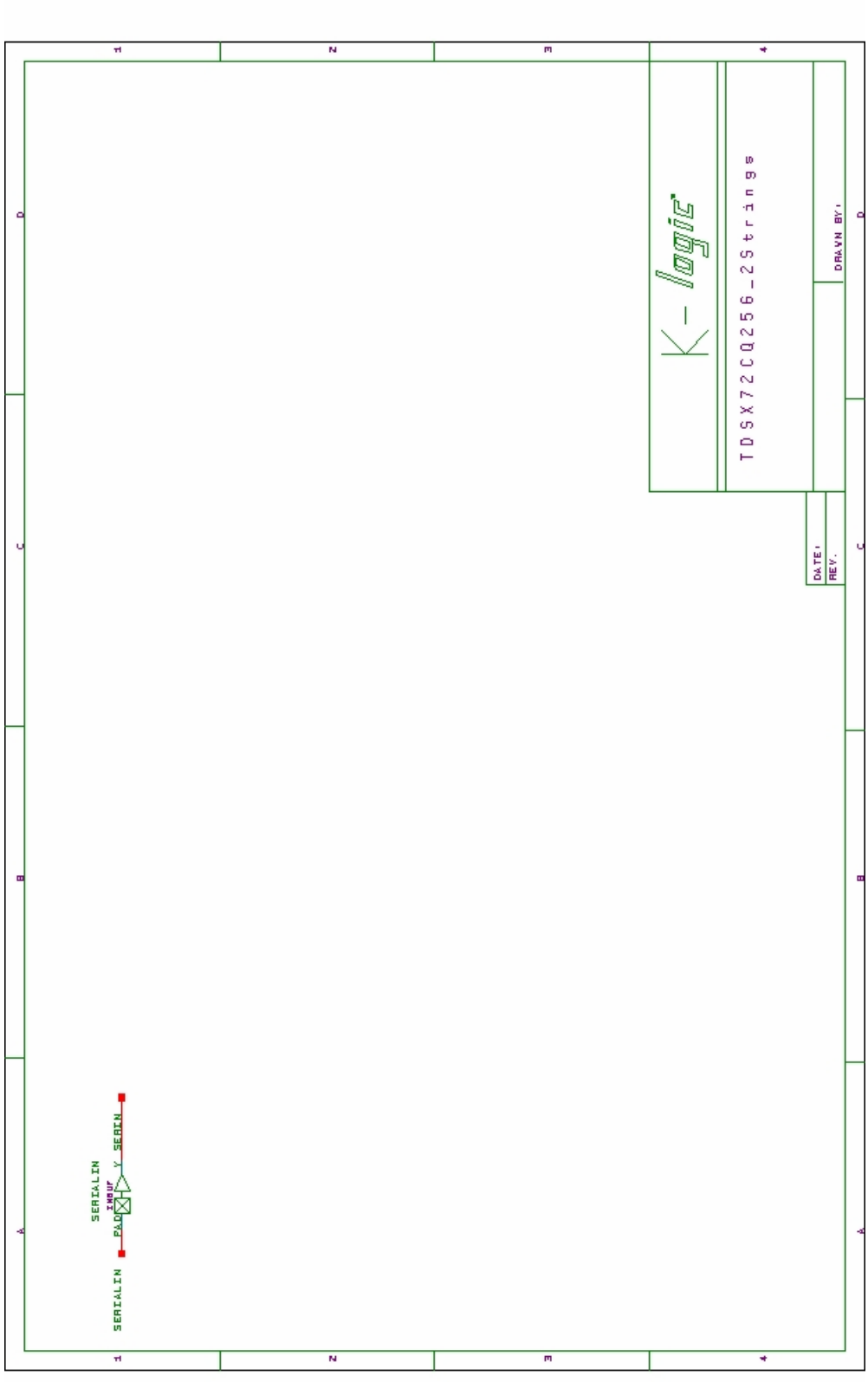

DRC
ANDC
ANDP
DRP
AND4
DR4
Y
A
B
C
D
Q
Dff8rB
RST
CLK
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

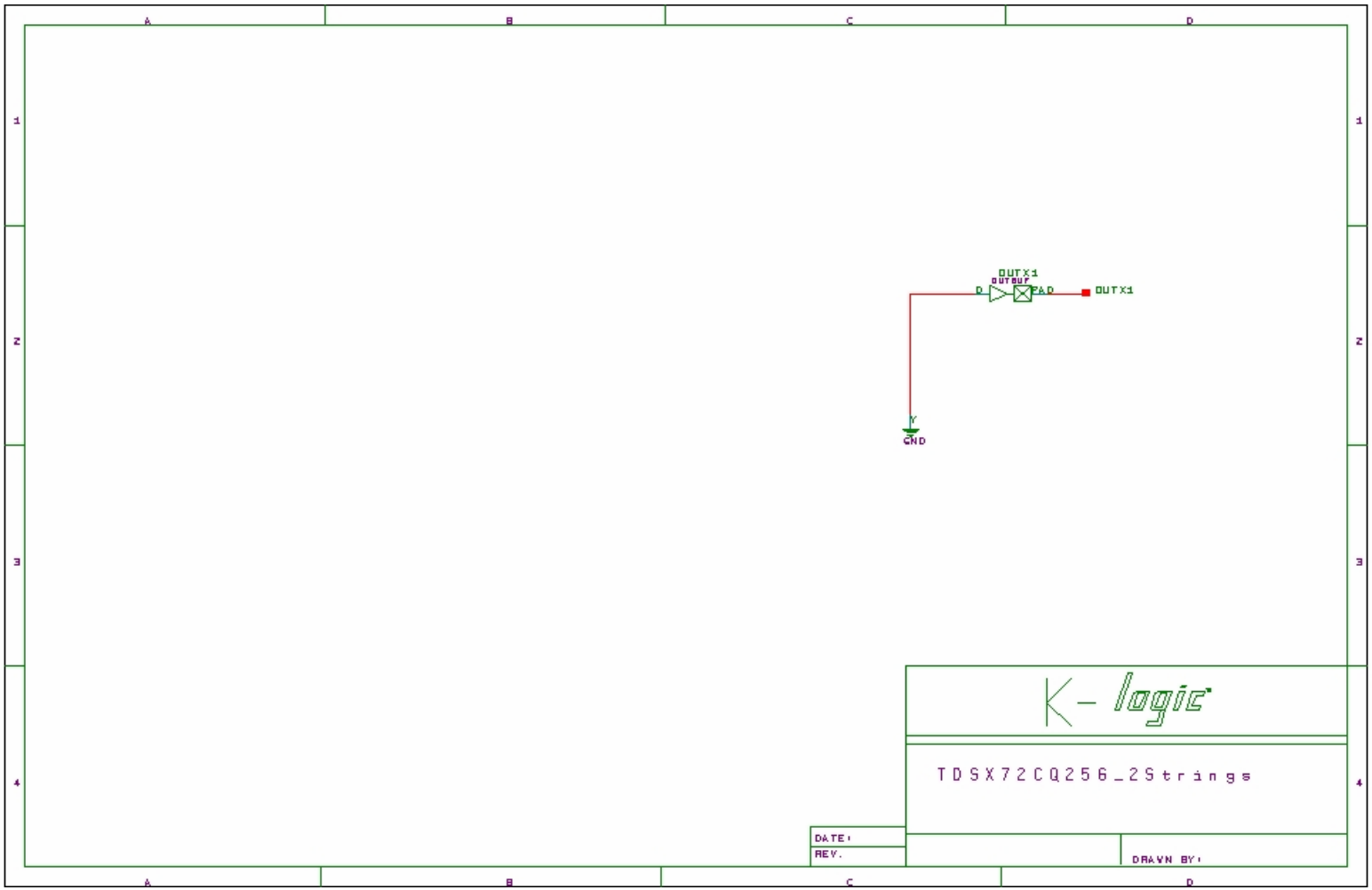

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDF
DRF
CLK
RST


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
RESETH
DA2H OUTBUF PAD
DA0H OUTBUF PAD
DA1H OUTBUF PAD
DAH INBUF PAD Y FFXNH
CLOCKH HCLKBUF PAD Y
RESETH INBUF PAD Y WRSTH
DAH
CLOCKH
RESETH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTAH
ENCNTAH
CNTALOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRDUMMY
IODII7
IODIO7
IODII0
IODIO0
IODII1
IODIO1
IODII2
IODIO2
IODII3
IODIO3
IODII4
IODIO4
IODII5
IODIO5
IODII6
IODIO6
INBUF
OUTBUF
PAD


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV:
SERIALIN
SERIALIN
Y SERIN
IMAGE
PAD


A
B
C
D
1
2
3
4
OUTX1
OUTBUF
D
PAD
OUTX1
Y
GND
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY: