TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX32SU-D1AYJ1
March 14, 2005
J.J. Wang
(650) 318-4576
jih-jong.wang@actel.com

I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 88 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 5 days room temperature annealing: average I_{CCA} = 52 mA, and average I_{CCI} = 42 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) for 10% degradation criterion.
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/ and http://www.actel.com) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement offers lower noise, better accuracy and more flexibility. In this test, the threshold of most of the available inputs is measured.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. There are two groups: DUT 65401, 65402 and 65403 are irradiated to 60 krad; DUT 65404, 65503 and 65504 are irradiated to 100 krad. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX32SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D1AYJ1
Quantity Tested	6
Serial Number	60 krad: 65401, 65402, 65403 100 krad: 65404, 65503, 65504
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

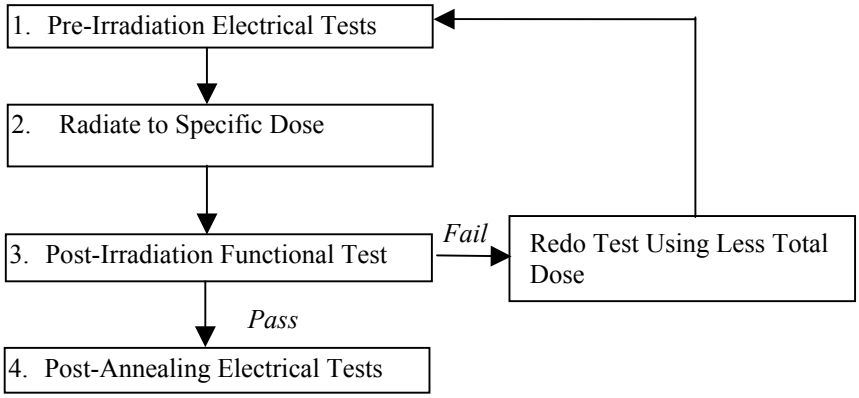


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs in both the 60-krad group and 100-krad group are bias-annealed for 5 days after the irradiation.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) are measured on twelve combinational nets listed in Table 2. The output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTR/YO0, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation and post-irradiation-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 6 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition near 60 krad. This transition is due to the temporary degradation of the charge pump because the radiation-induced leakage current overloads the output of the charge pump. After the pump degrading to a certain voltage, the array logic changes to another state and logic outputs are disabled; this causes the I_{CCA} transition. However, the temporary degradation of the charge pump is only a testing artifact because the logic outputs recover after few hours of room temperature annealing.

By technicality, TM1019 doesn't allow further irradiation after disabling of the logic outputs. However, in this case, because the logic state of the DUT is still well defined, further irradiation is still valid. Every DUT was irradiated to 100 krad; after few hours of room temperature annealing, the logic outputs in every DUT were recovered.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data are compared with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
65401	60 krad	19.3	11	39.3	16
65402	60 krad	18.6	12	38.5	17
65403	60 krad	16.4	10	36.6	13
65404	100 krad	306	47	195	38
65503	100 krad	308	58	162	41
65504	100 krad	283	51	184	47

The 60 krad group shows the post-annealed I_{CC} passing the 25 mA spec. For the 100-krad group, a semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 65404, the tolerance is extracted as 88 krad for 10 years mission.

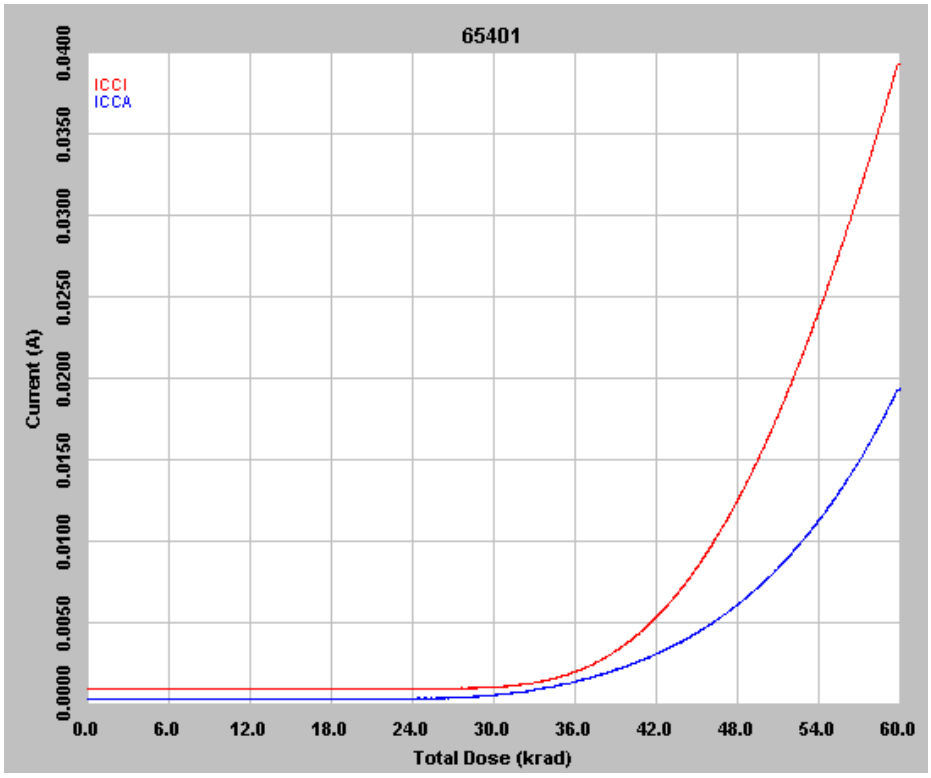


Figure 2 In flux I_{CCA} and I_{CCI} of DUT 65401, 60-krad total dose

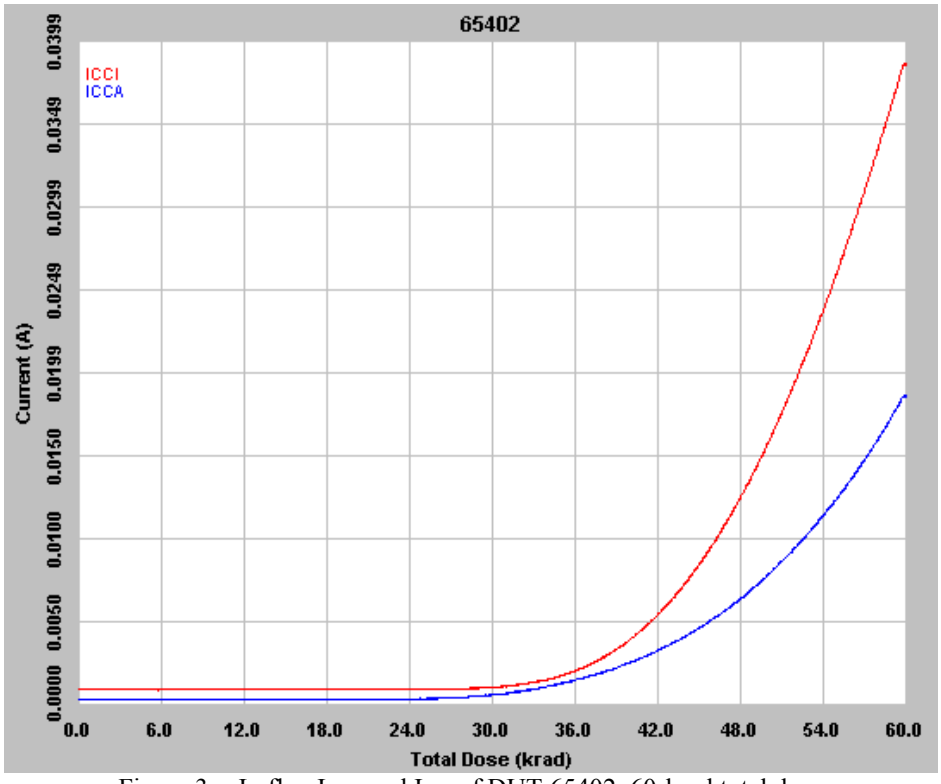


Figure 3 In flux I_{CCA} and I_{CCI} of DUT 65402, 60-krad total dose

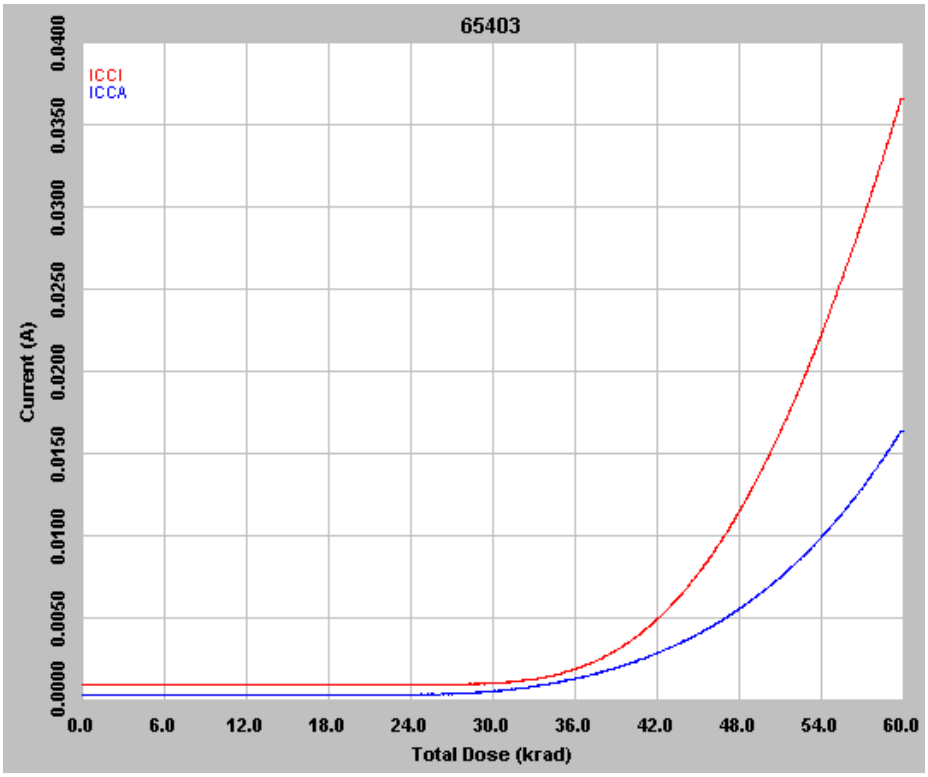


Figure 4 In flux I_{CCA} and I_{CCI} of DUT 65403, 60-krad total dose

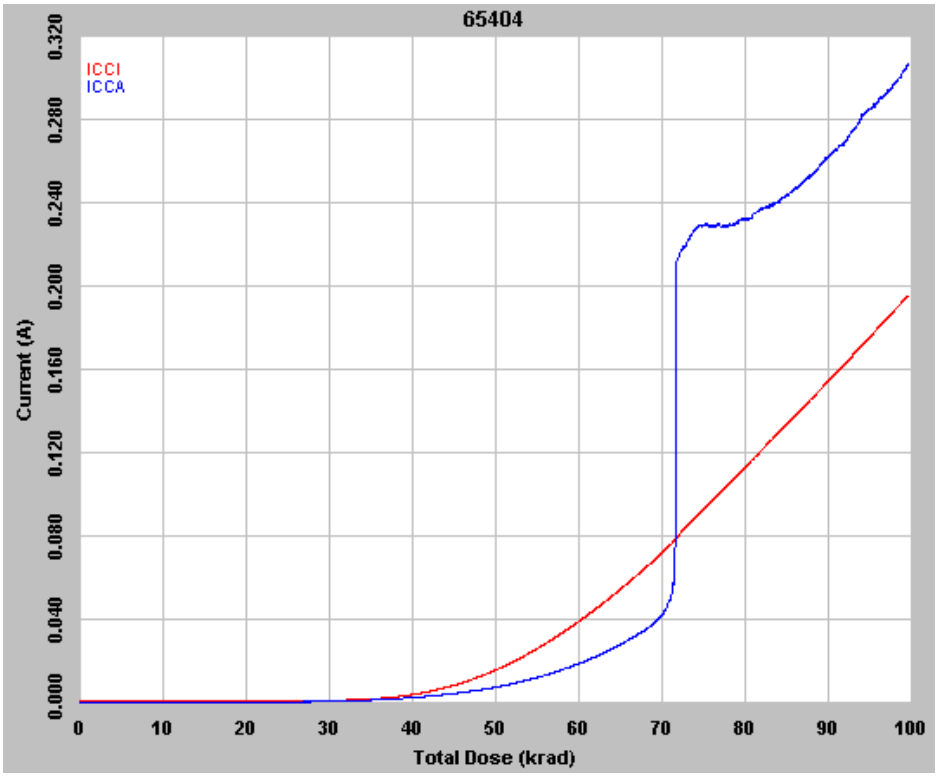


Figure 5 In flux I_{CCA} and I_{CCI} of DUT 65404, I_{CCA} shows a transition near 71 krad that indicates the temporary disabling of the outputs

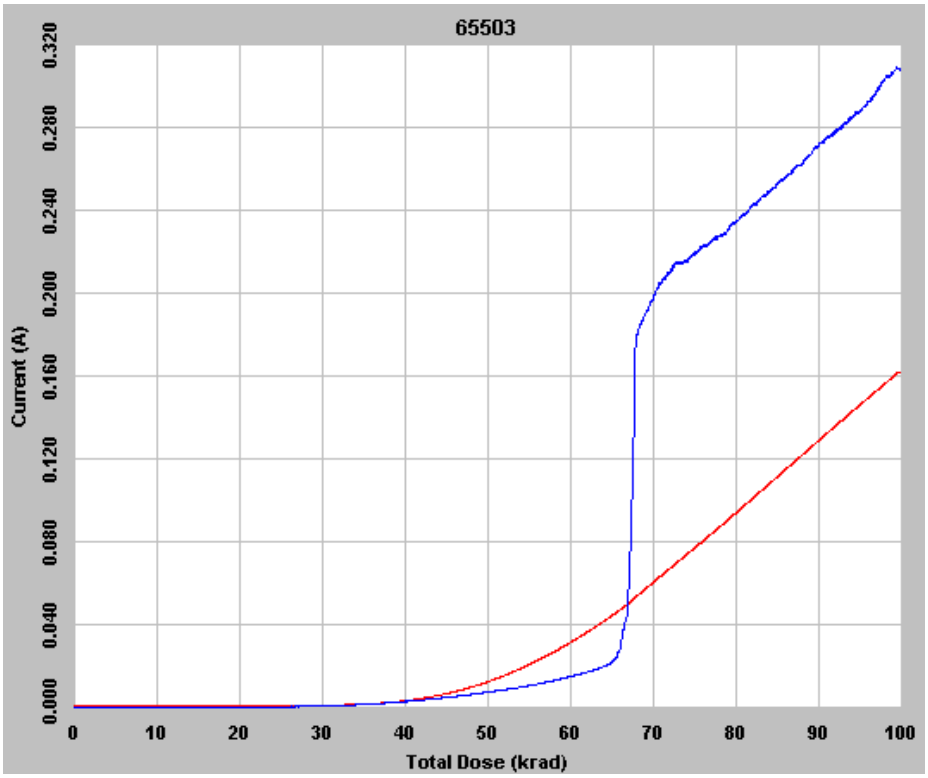


Figure 6 In flux I_{CCA} and I_{CCI} of DUT 65503, I_{CCA} shows a transition near 67 krad that indicates the temporary disabling of the outputs.

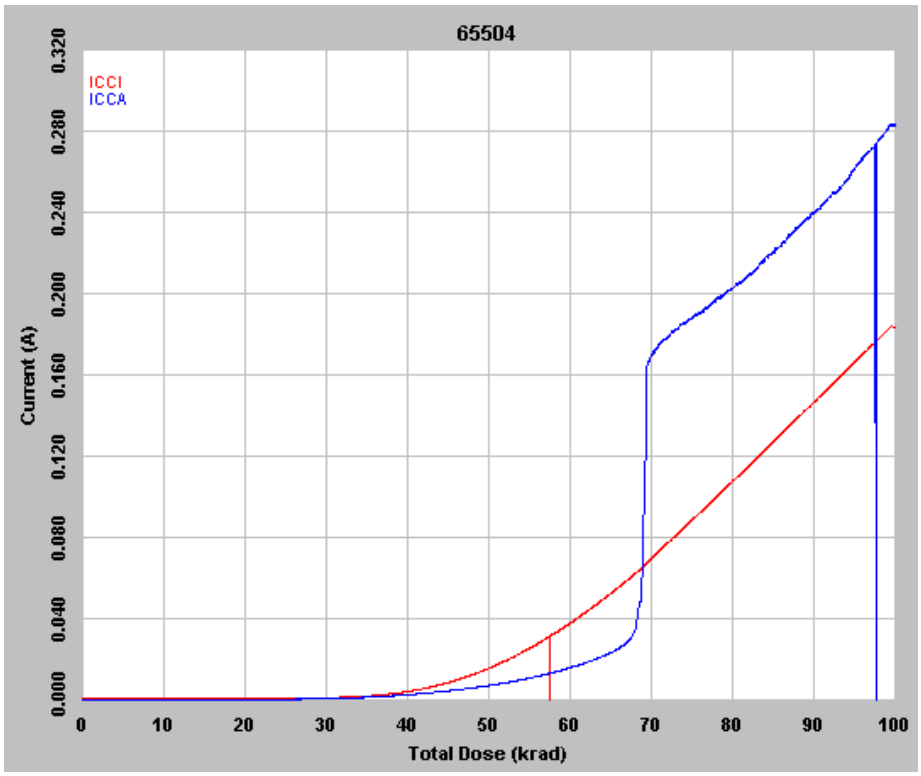


Figure 7 In flux I_{CCA} and I_{CCI} of DUT 65504, I_{CCA} shows a transition near 69 krad that indicates the temporary disabling of the outputs.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. In every case the data are within the spec limits, and the radiation effect is negligible.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA/QA0				DAH/QA0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
65401	60 krad	1.38	1.38	1.44	1.45	1.37	1.41	1.44	1.46
65402	60 krad	1.38	1.21	1.44	1.50	1.37	1.36	1.45	1.50
65403	60 krad	1.37	1.39	1.44	1.45	1.37	1.40	1.45	1.47
65404	100 krad	1.37	1.40	1.45	1.48	1.37	1.46	1.44	1.54
65503	100 krad	1.38	1.41	1.45	1.47	1.38	1.40	1.44	1.50
65504	100 krad	1.37	1.40	1.44	1.63	1.38	1.41	1.44	1.49

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR/YO0				ENCNTRH/YO0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
65401	60 krad	1.39	1.39	1.45	1.46	1.38	1.41	1.44	1.46
65402	60 krad	1.38	1.37	1.46	1.48	1.37	1.36	1.45	1.48
65403	60 krad	1.39	1.38	1.46	1.47	1.38	1.41	1.45	1.47
65404	100 krad	1.37	1.39	1.45	1.48	1.39	1.40	1.45	1.48
65503	100 krad	1.38	1.38	1.44	1.45	1.39	1.38	1.45	1.46
65504	100 krad	1.37	1.39	1.45	1.52	1.38	1.41	1.45	1.45

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0/IDIO0				IDII1/IDIO1			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
65401	60 krad	1.39	1.41	1.45	1.47	1.40	1.41	1.45	1.47
65402	60 krad	1.38	1.35	1.45	1.49	1.54	1.42	1.56	1.57
65403	60 krad	1.38	1.38	1.45	1.45	1.39	1.40	1.45	1.46
65404	100 krad	1.39	1.40	1.46	1.50	1.40	1.36	1.46	1.48
65503	100 krad	1.38	1.41	1.46	1.48	1.38	1.40	1.44	1.47
65504	100 krad	1.38	1.31	1.46	1.56	1.38	1.46	1.45	1.52

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2/IDIO2				IDII3/IDIO3			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
65401	60 krad	1.37	1.40	1.44	1.48	1.38	1.40	1.44	1.47
65402	60 krad	1.36	1.34	1.44	1.49	1.38	1.31	1.45	1.52
65403	60 krad	1.38	1.39	1.44	1.47	1.39	1.38	1.46	1.47
65404	100 krad	1.38	1.38	1.45	1.49	1.39	1.37	1.46	1.47
65503	100 krad	1.38	1.37	1.46	1.47	1.38	1.40	1.45	1.48
65504	100 krad	1.37	1.37	1.44	1.49	1.38	1.42	1.44	1.5

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4/IDIO4				IDII5/IDIO5			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
65401	60 krad	1.38	1.39	1.45	1.47	1.38	1.41	1.45	1.44
65402	60 krad	1.36	1.34	1.45	1.46	1.37	1.26	1.45	1.47
65403	60 krad	1.40	1.38	1.44	1.46	1.38	1.40	1.44	1.45
65404	100 krad	1.39	1.42	1.44	1.47	1.38	1.42	1.45	1.51
65503	100 krad	1.37	1.41	1.44	1.49	1.37	1.39	1.45	1.47
65504	100 krad	1.38	1.39	1.45	1.47	1.38	1.41	1.45	1.48

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6/IDIO6				IDII7/IDIO7			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
65401	60 krad	1.39	1.41	1.46	1.48	1.39	1.42	1.45	1.48
65402	60 krad	1.40	1.36	1.46	1.49	1.38	1.37	1.44	1.46
65403	60 krad	1.39	1.37	1.46	1.46	1.38	1.38	1.45	1.44
65404	100 krad	1.39	1.41	1.44	1.49	1.38	1.37	1.45	1.48
65503	100 krad	1.37	1.40	1.44	1.48	1.38	1.40	1.44	1.46
65504	100 krad	1.37	1.43	1.45	1.52	1.38	1.41	1.44	1.48

D. *Output-Drive Voltage (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
65401	60 krad	0.009	0.009	0.104	0.106	0.173	0.176	0.437	0.440	0.900	0.914
65402	60 krad	0.009	0.009	0.102	0.104	0.170	0.175	0.430	0.437	0.884	0.899
65403	60 krad	0.009	0.009	0.104	0.104	0.173	0.173	0.437	0.437	0.889	0.898
65404	100 krad	0.009	0.009	0.103	0.104	0.172	0.174	0.435	0.438	0.894	0.901
65503	100 krad	0.009	0.009	0.105	0.106	0.175	0.176	0.441	0.440	0.906	0.912
65504	100 krad	0.009	0.009	0.103	0.105	0.172	0.174	0.434	0.440	0.894	0.904

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
65401	60 krad	4.98	4.99	4.86	4.86	4.64	4.64	4.06	4.05	2.71	2.66
65402	60 krad	4.98	4.99	4.86	4.86	4.64	4.64	4.05	4.04	2.67	2.61
65403	60 krad	4.98	4.98	4.86	4.86	4.64	4.65	4.05	4.07	2.69	2.77
65404	100 krad	4.98	4.98	4.86	4.86	4.64	4.64	4.04	4.04	2.66	2.64
65503	100 krad	4.98	4.98	4.86	4.86	4.64	4.64	4.05	4.04	2.69	2.63
65504	100 krad	4.98	4.98	4.86	4.85	4.64	4.63	4.05	4.03	2.69	2.60

E. *Propagation Delay*

Table 8 lists the pre-irradiation and post-annealing propagation delays and the radiation-induced degradations in percentage. In every case the DUT passes the 10% degradation criterion.

Table 8 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation	Post-Annealing	Degradation
65401	60 krad	515.30	525.33	1.97%
65402	60 krad	520.20	522.29	0.41%
65403	60 krad	510.01	511.79	0.36%
65404	100 krad	511.70	527.50	3.10%
65503	100 krad	507.10	516.02	1.78%
65504	100 krad	511.21	528.02	3.34%

F. Transition Time

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case the radiation effect is negligible.

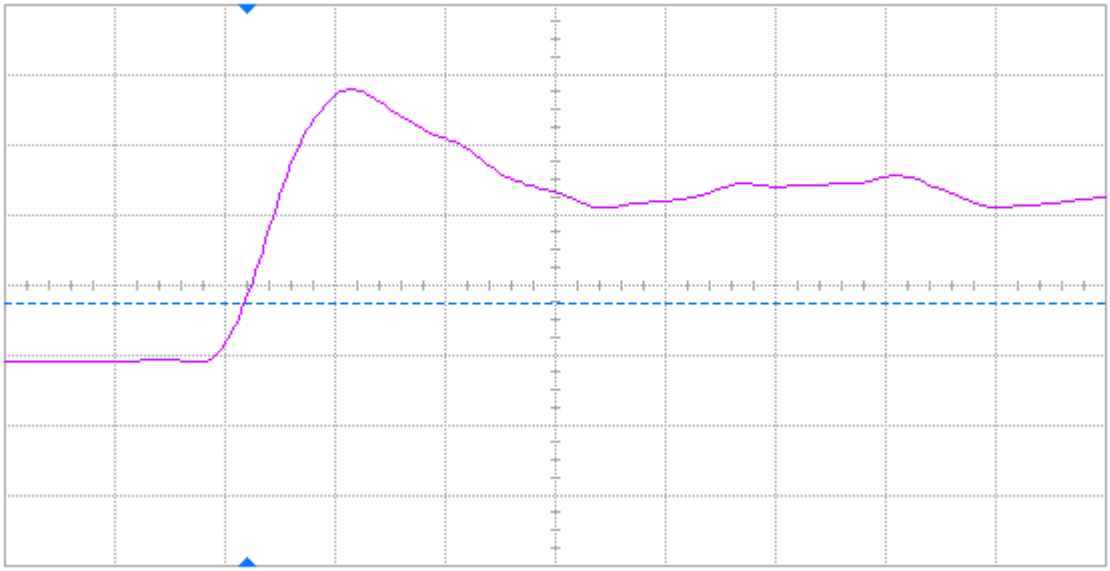


Figure 8(a) DUT 65401 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

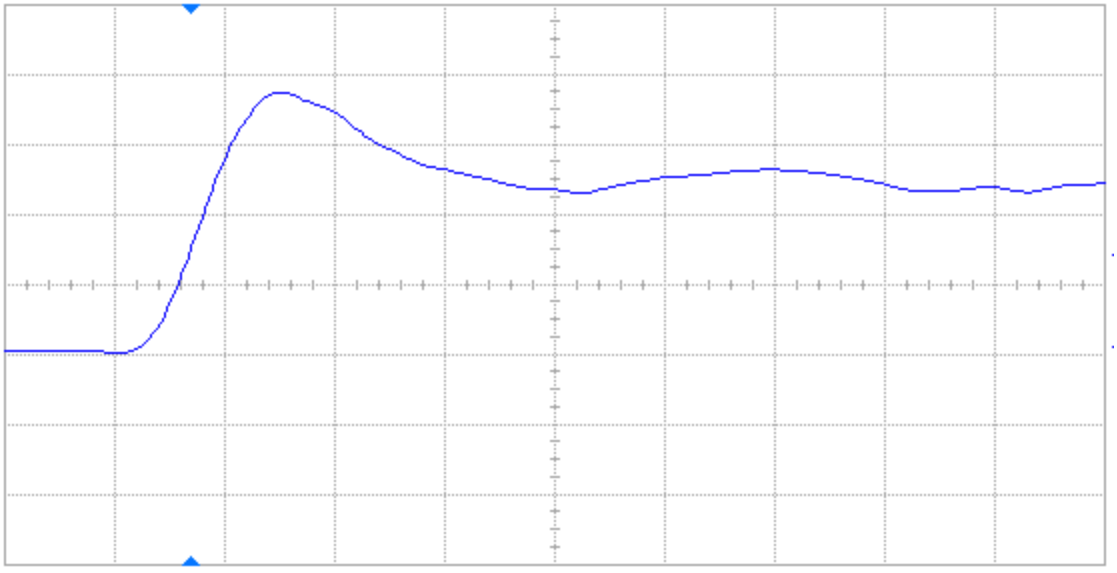


Figure 8(b) DUT 65401 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

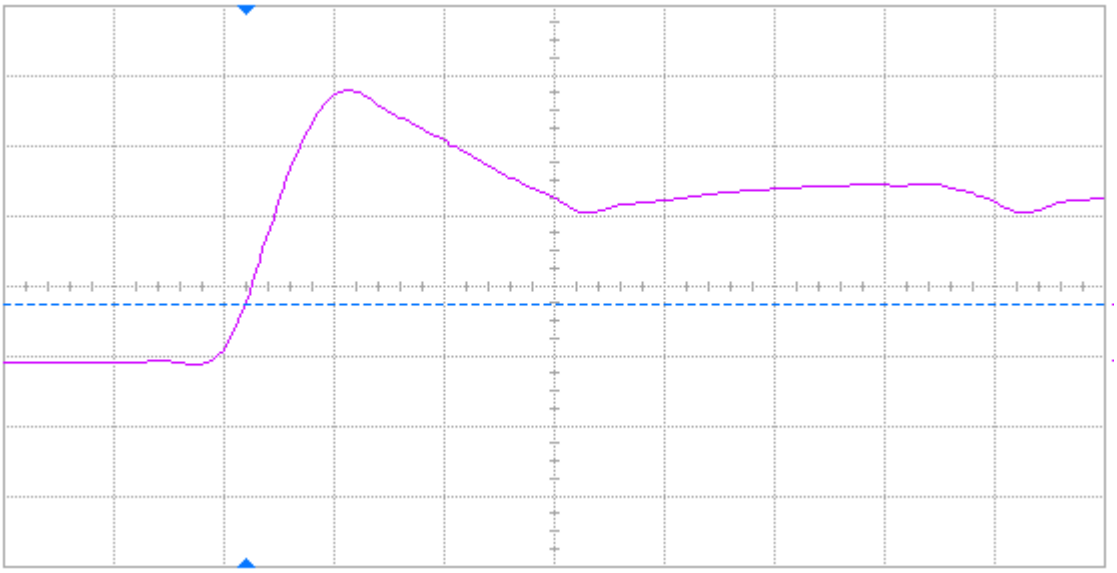


Figure 9(a) DUT 65402 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

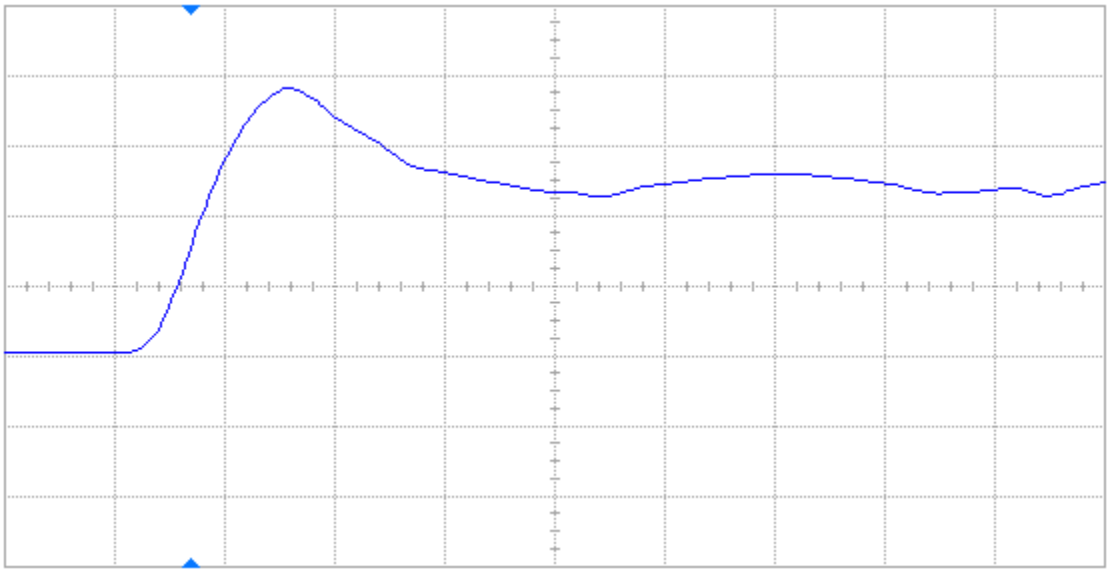


Figure 9(b) DUT 65402 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

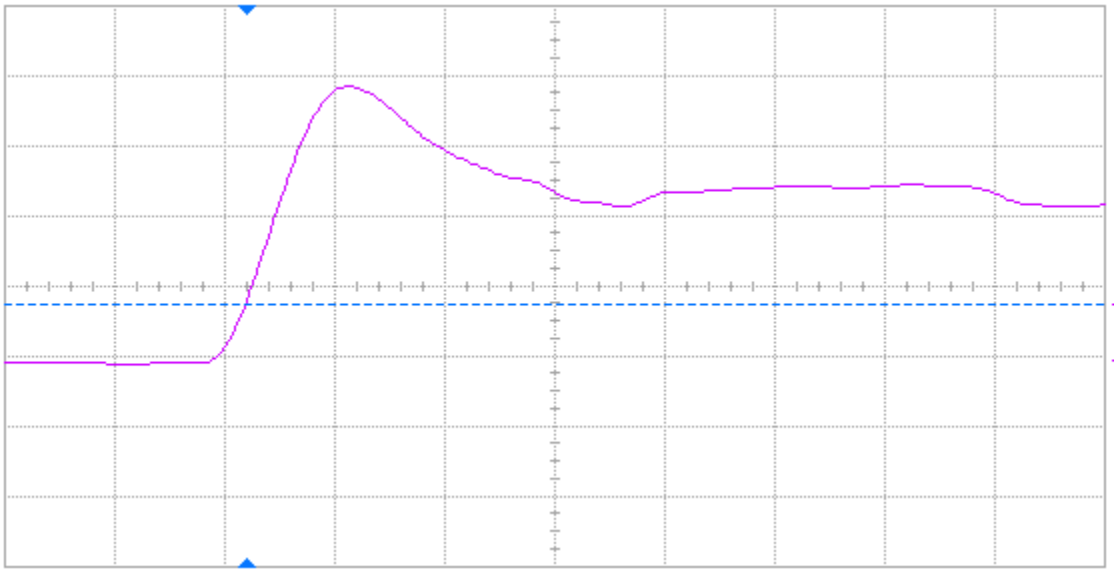


Figure 10(a) DUT 65403 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

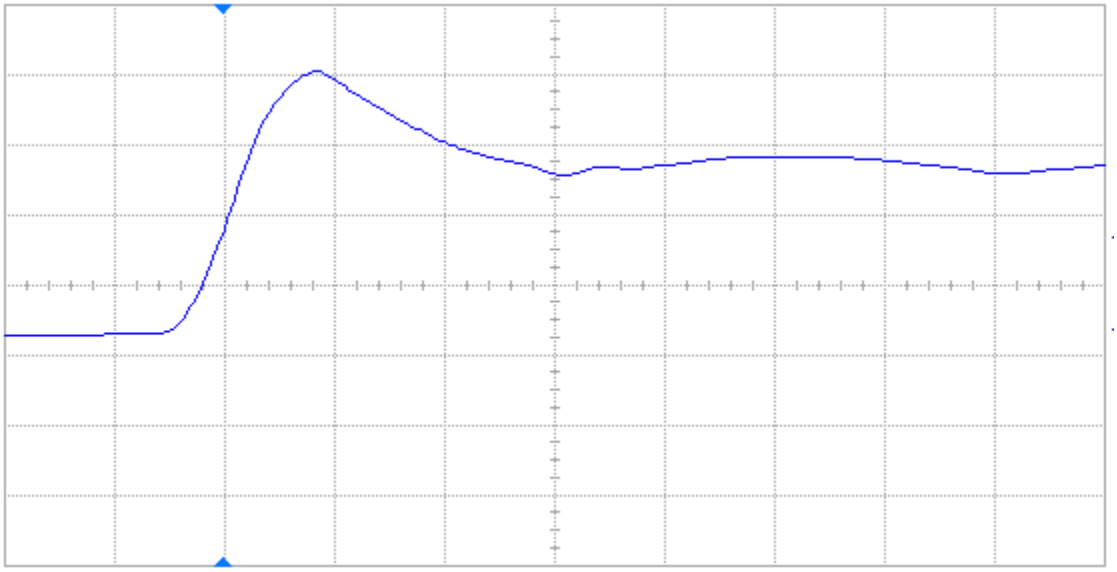


Figure 10(b) DUT 65403 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

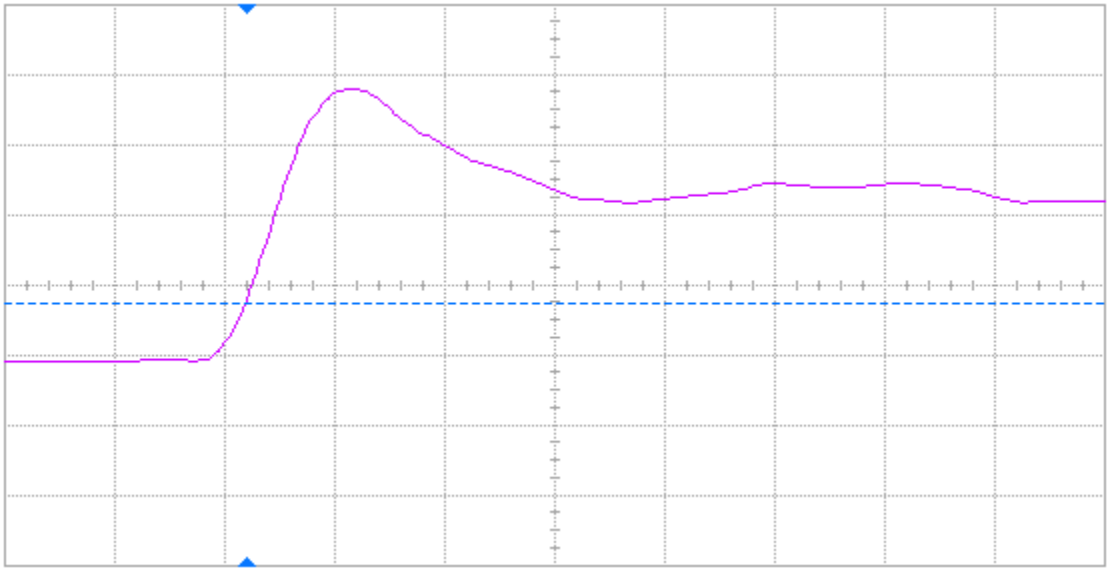


Figure 11(a) DUT 65404 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

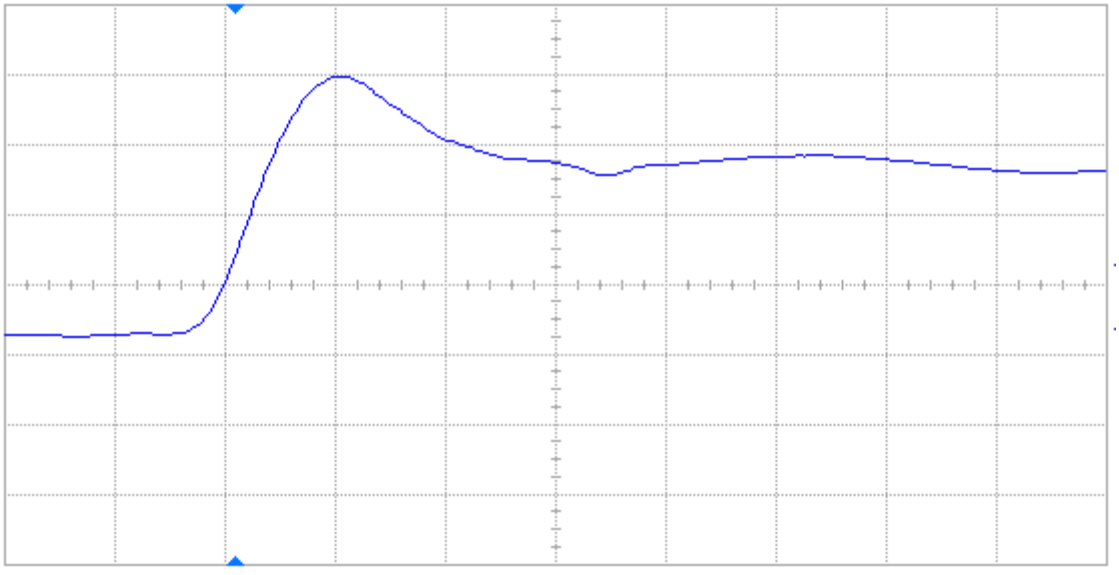


Figure 11(b) DUT 65404 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

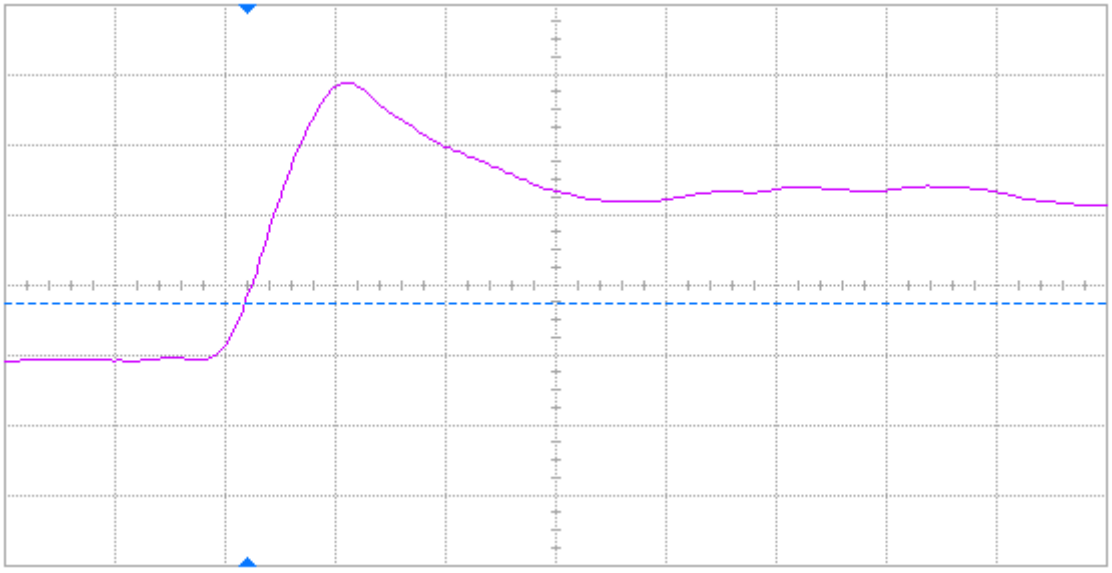


Figure 12(a) DUT 65503 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

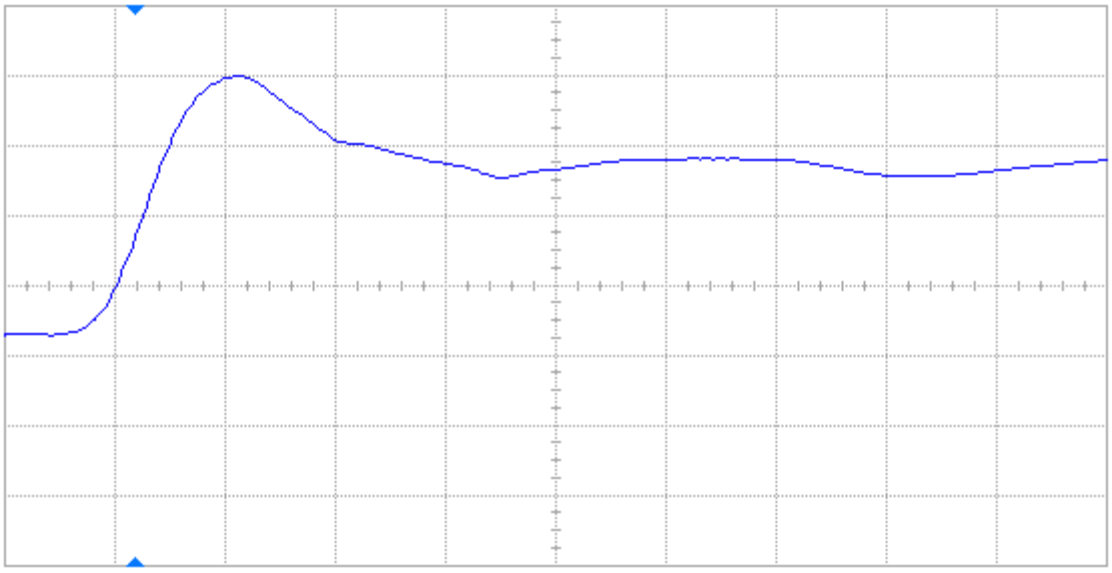


Figure 12(b) DUT 65503 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

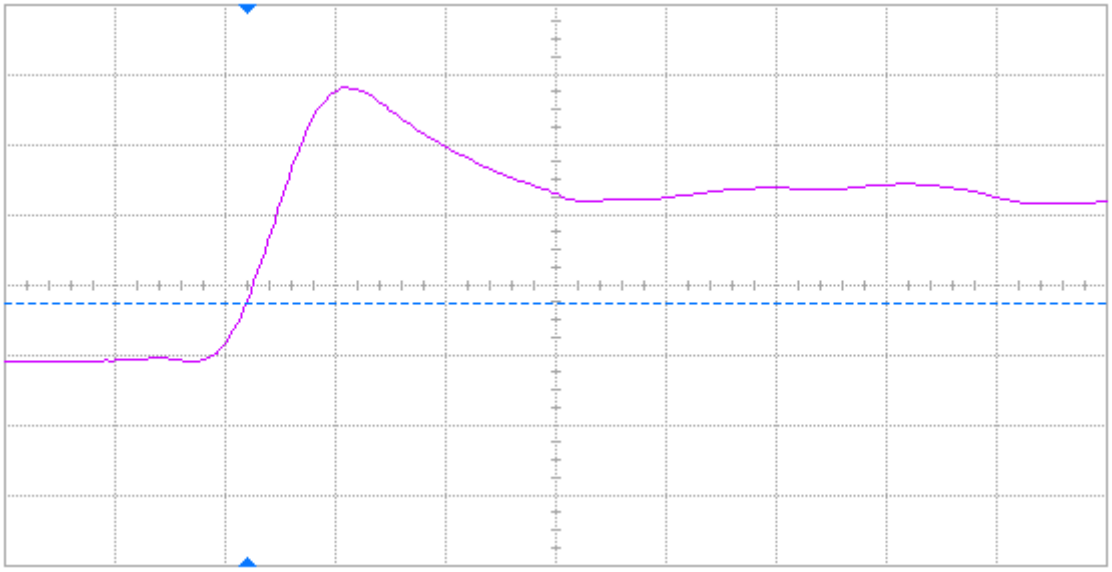


Figure 13(a) DUT 65504 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

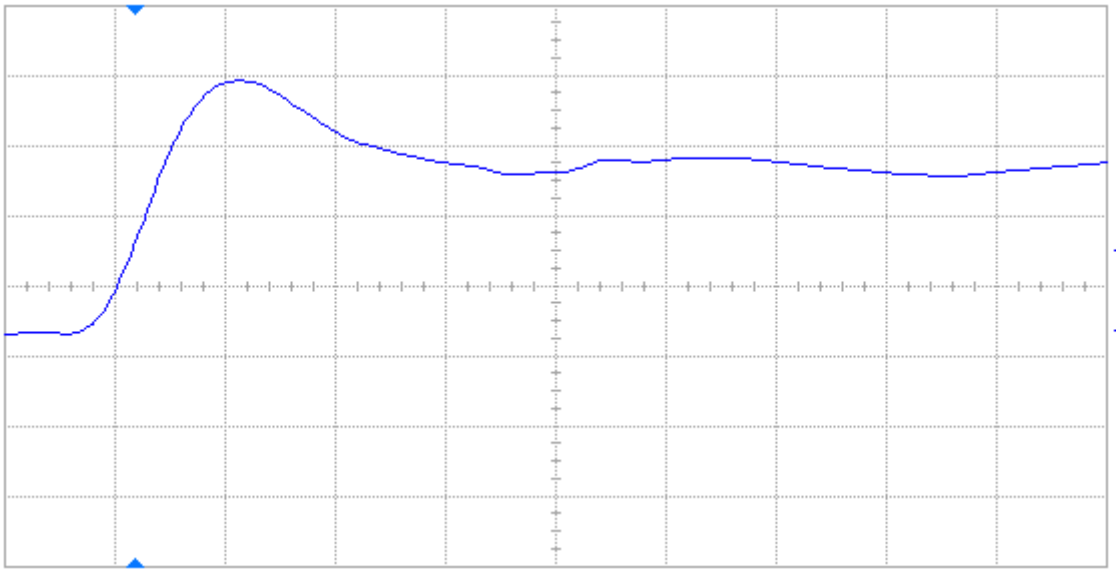


Figure 13(b) DUT 65504 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

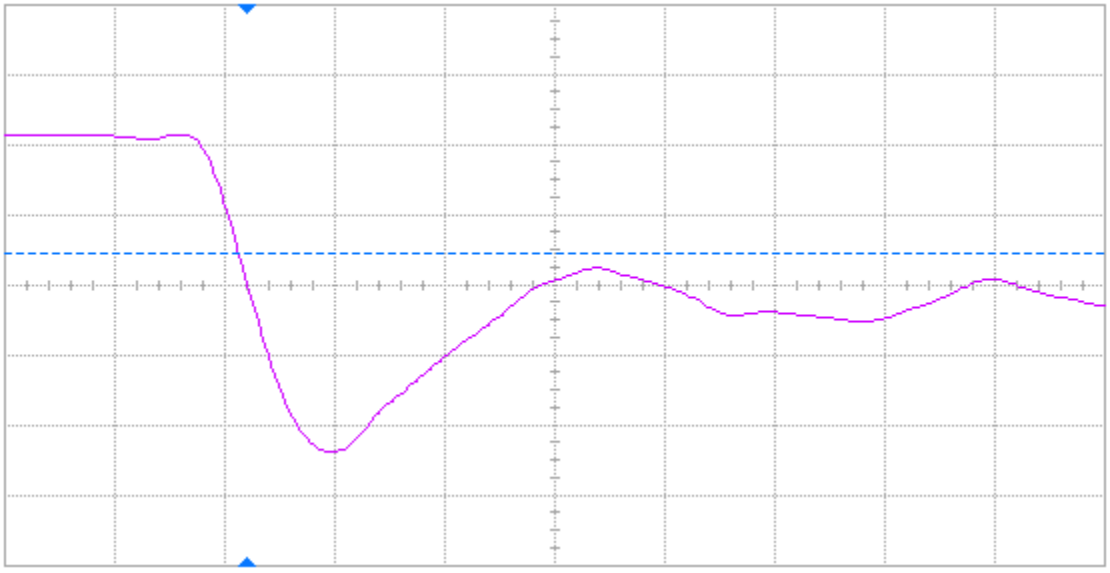


Figure 14(a) DUT 65401 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

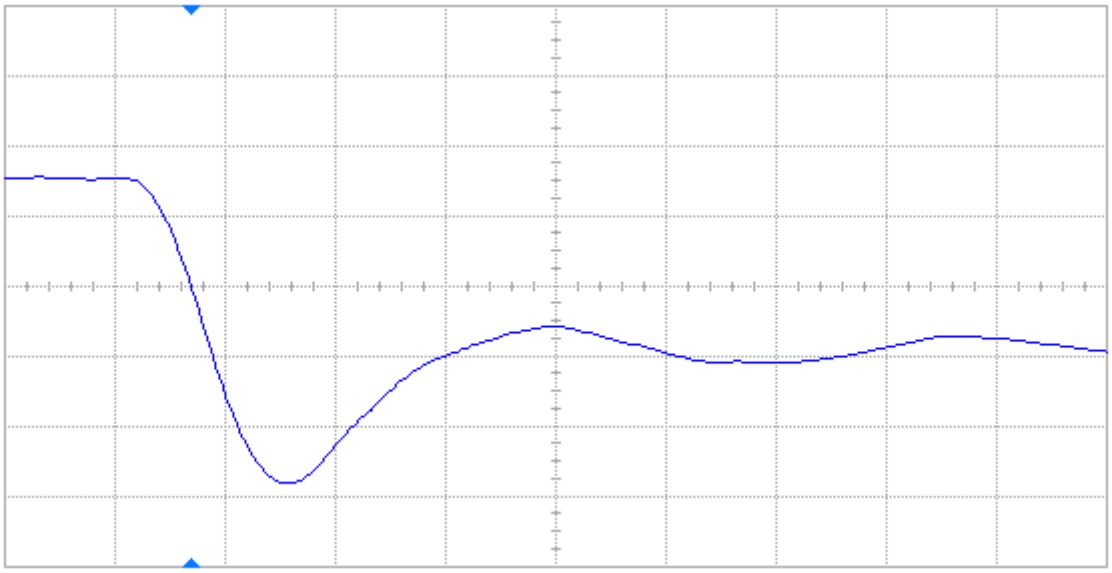


Figure 14(b) DUT 65401 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

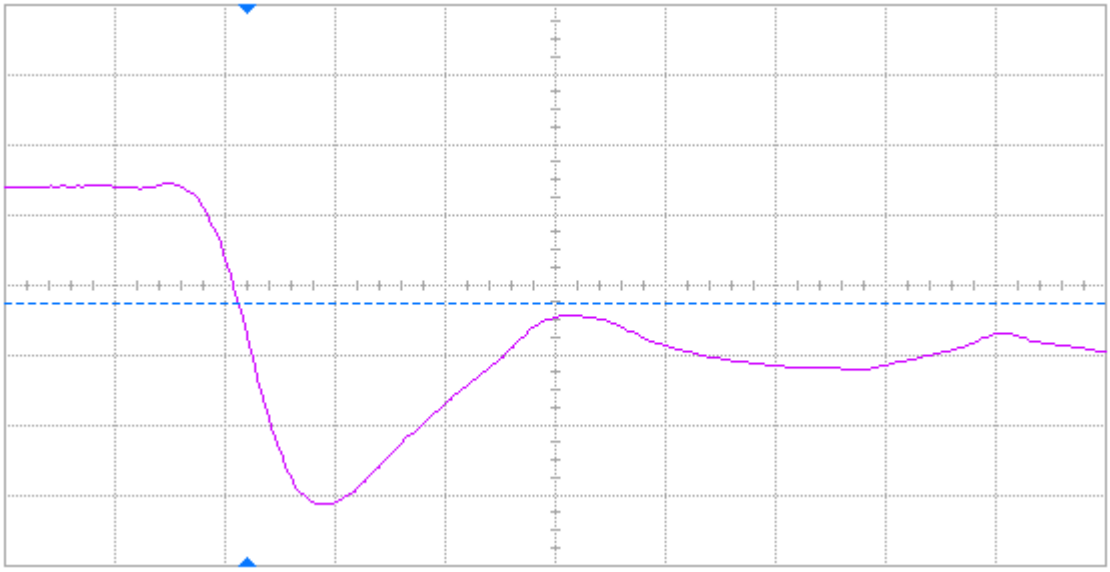


Figure 15(a) DUT 65402 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

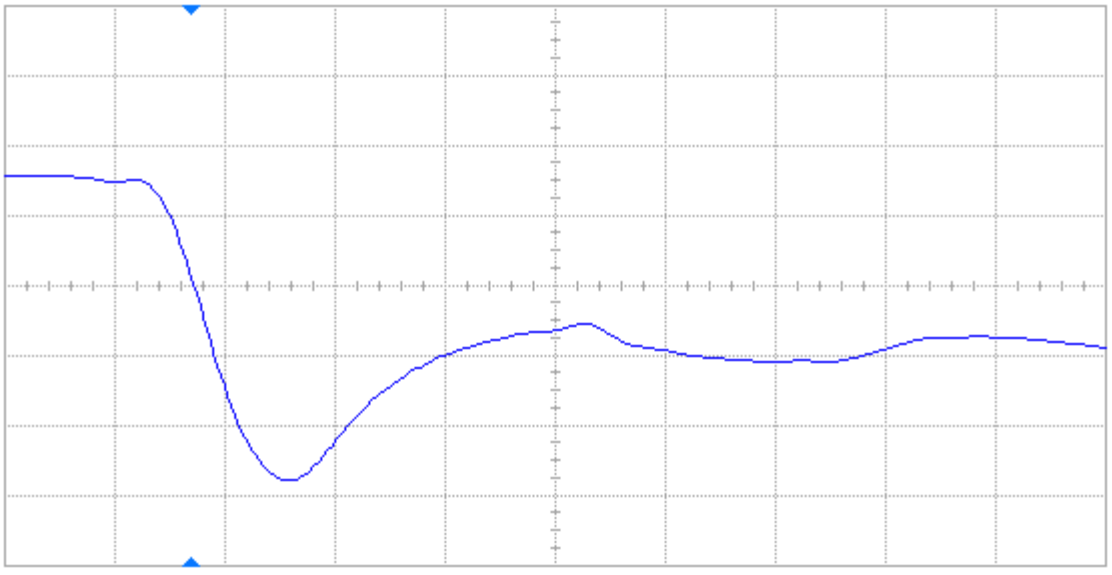


Figure 15(b) DUT 65402 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

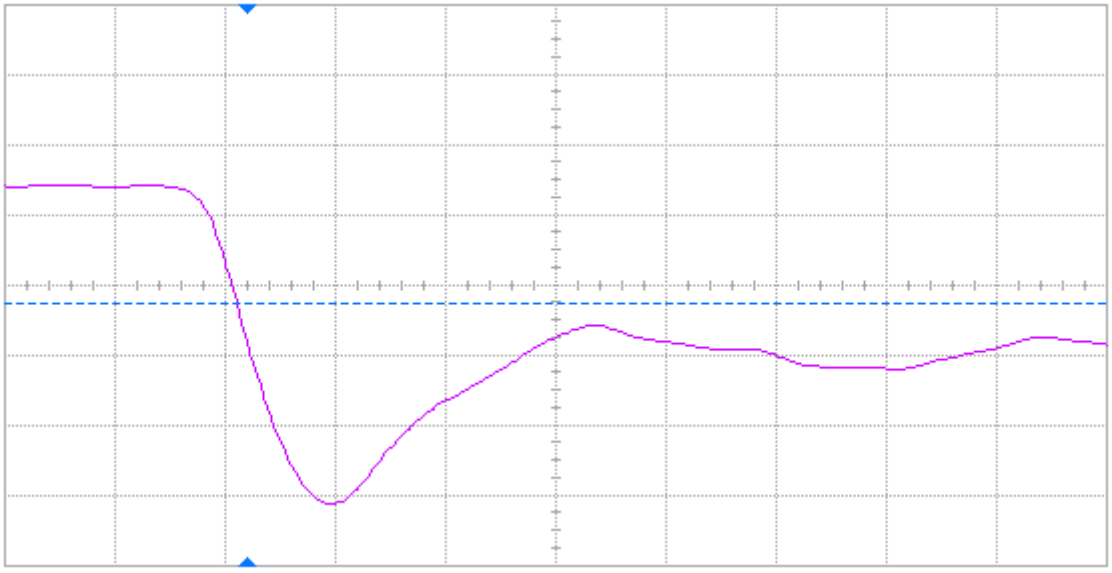


Figure 16(a) DUT 65403 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

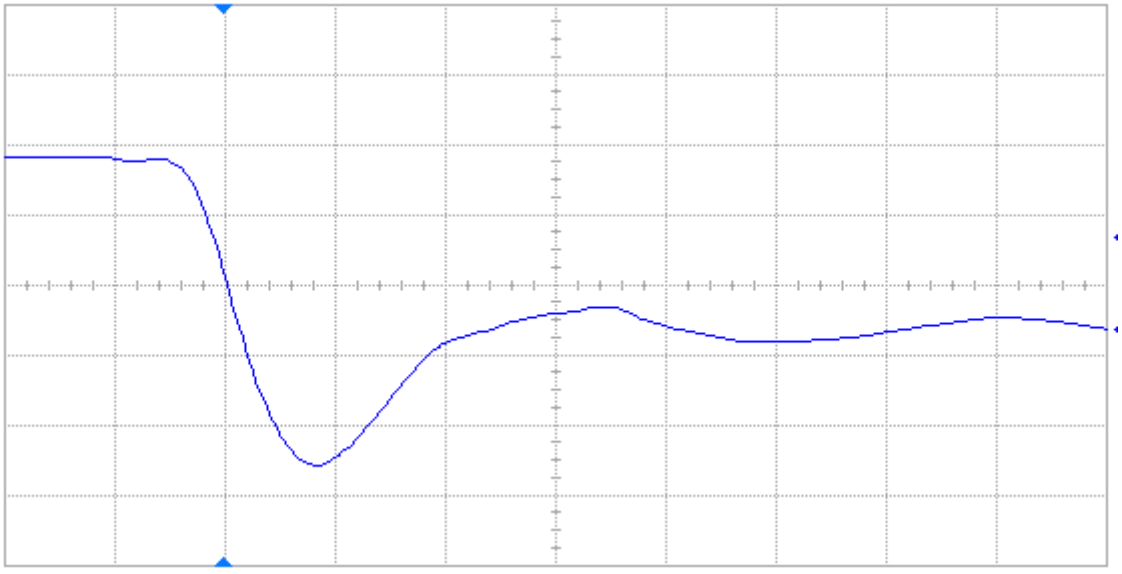


Figure 16(b) DUT 65403 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

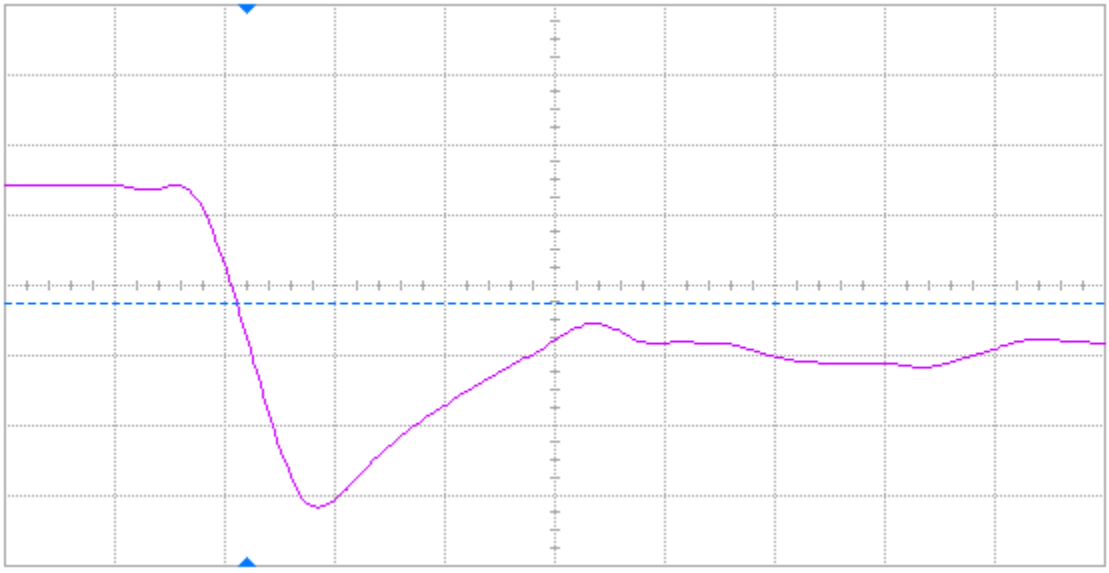


Figure 17(a) DUT 65404 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

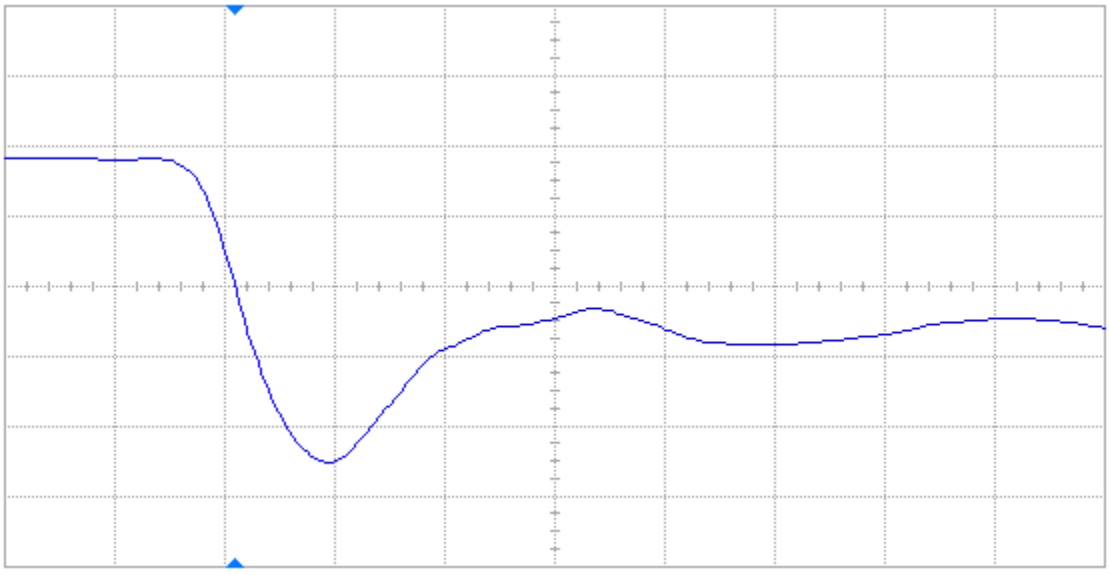


Figure 17(b) DUT 65404 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

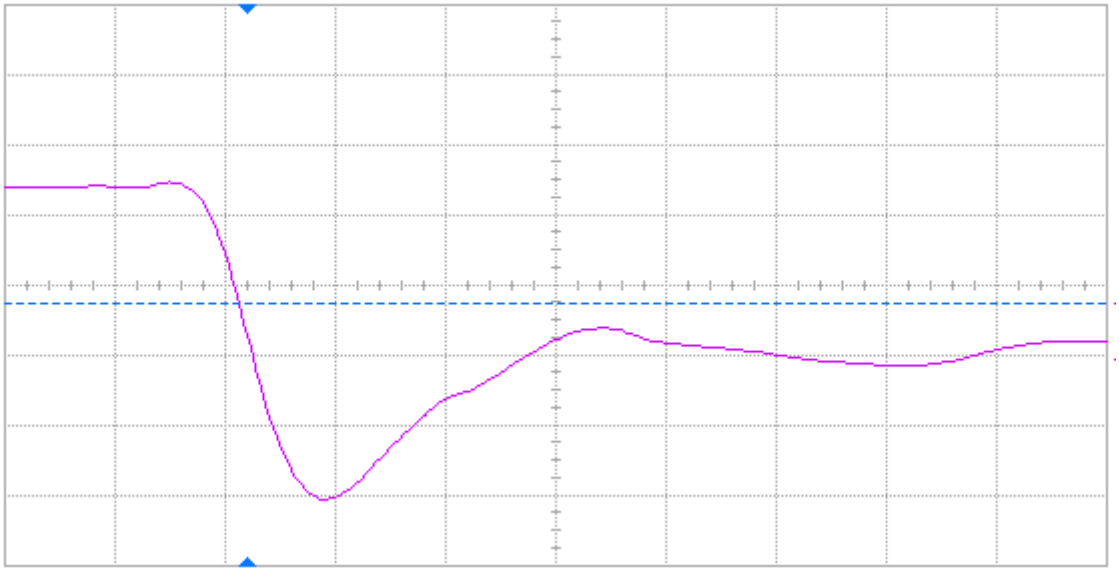


Figure 18(a) DUT 65503 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

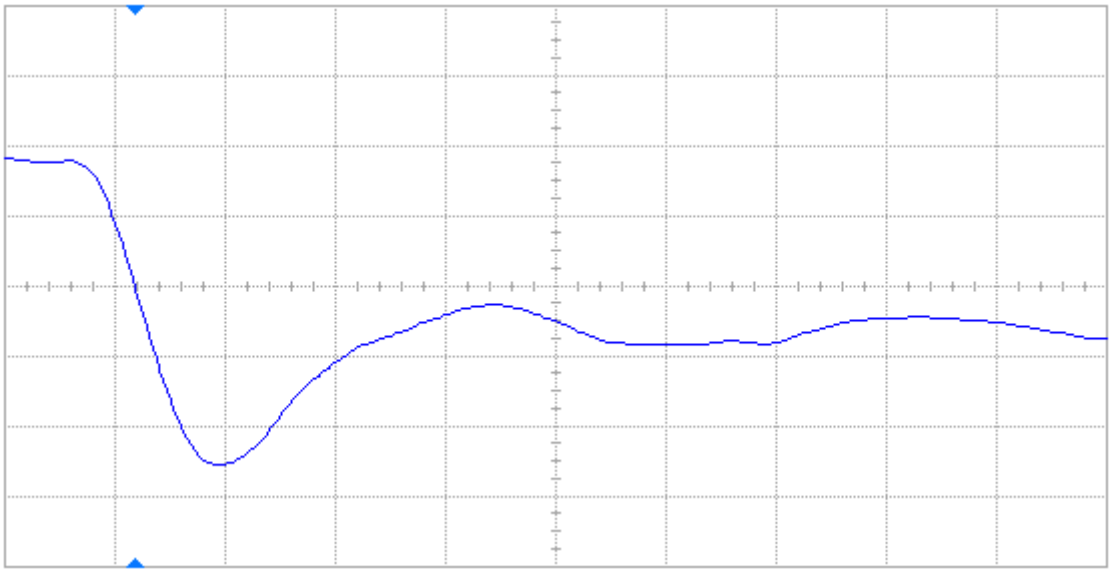


Figure 18(b) DUT 65503 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

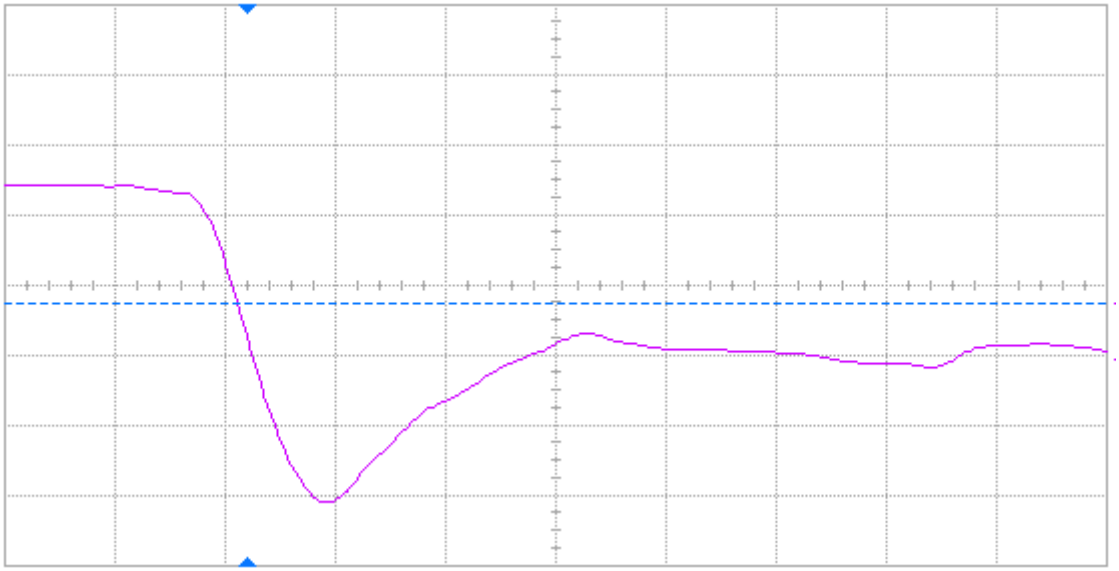


Figure 19(a) DUT 65504 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

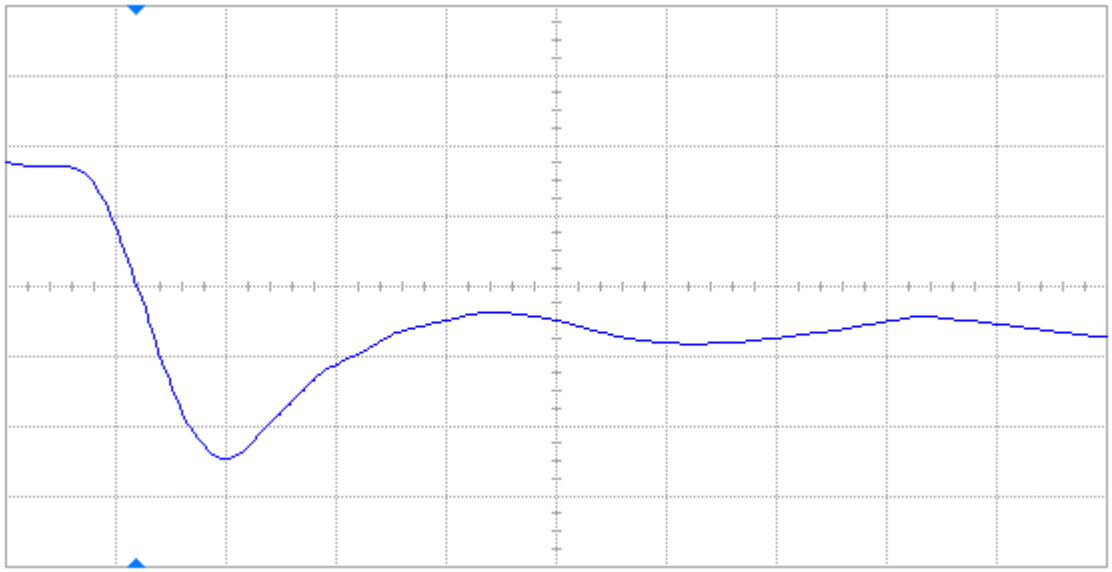
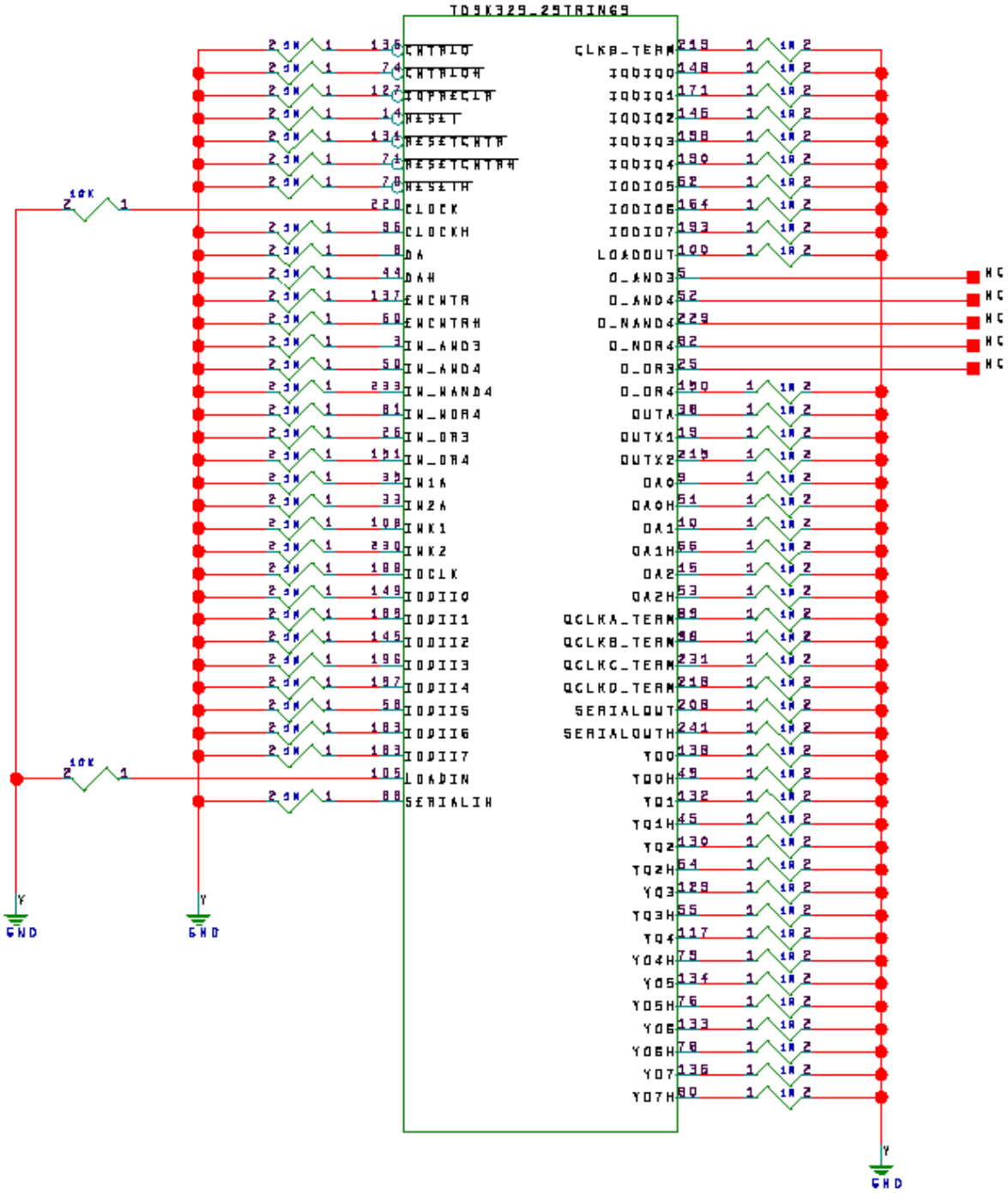
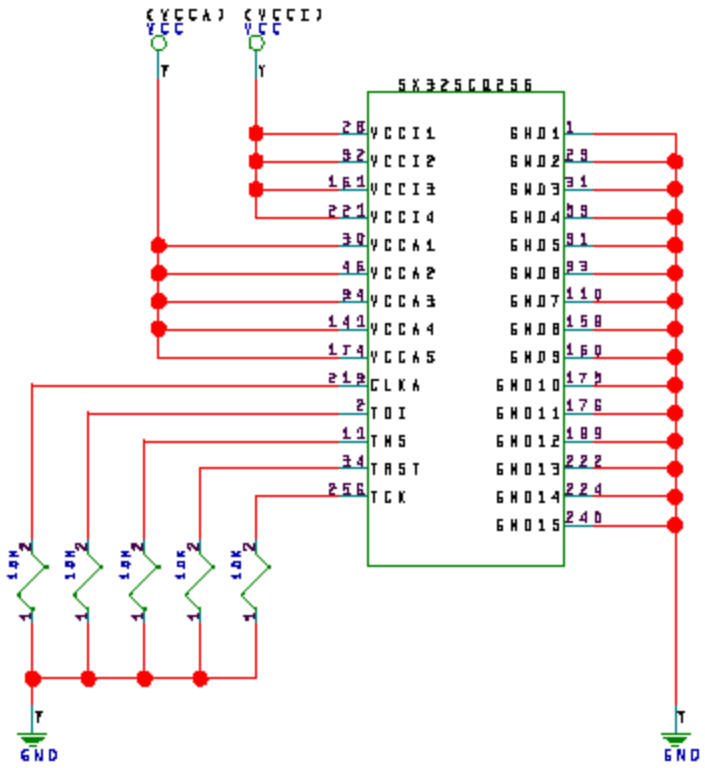


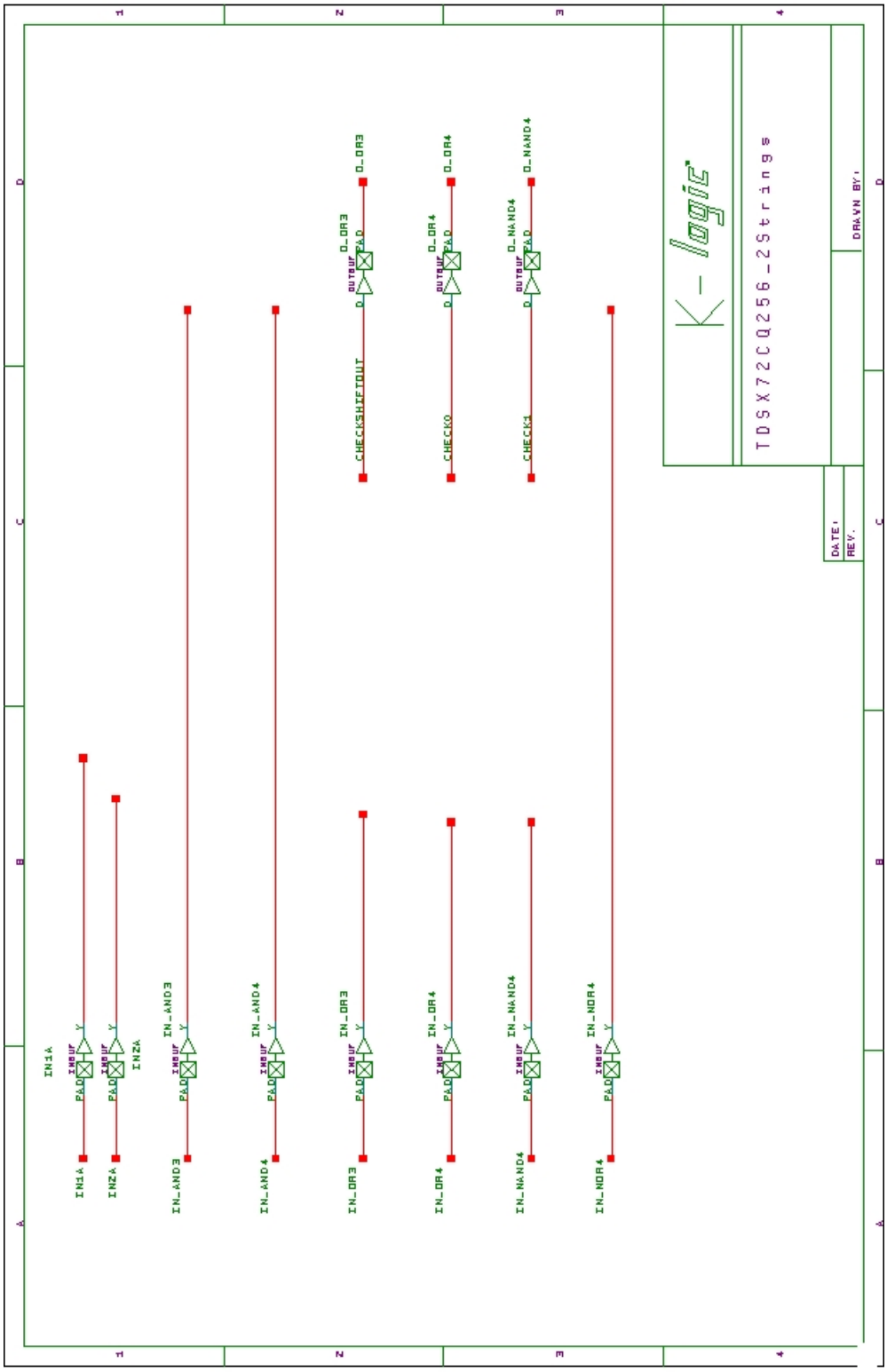
Figure 19(b) DUT 65504 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

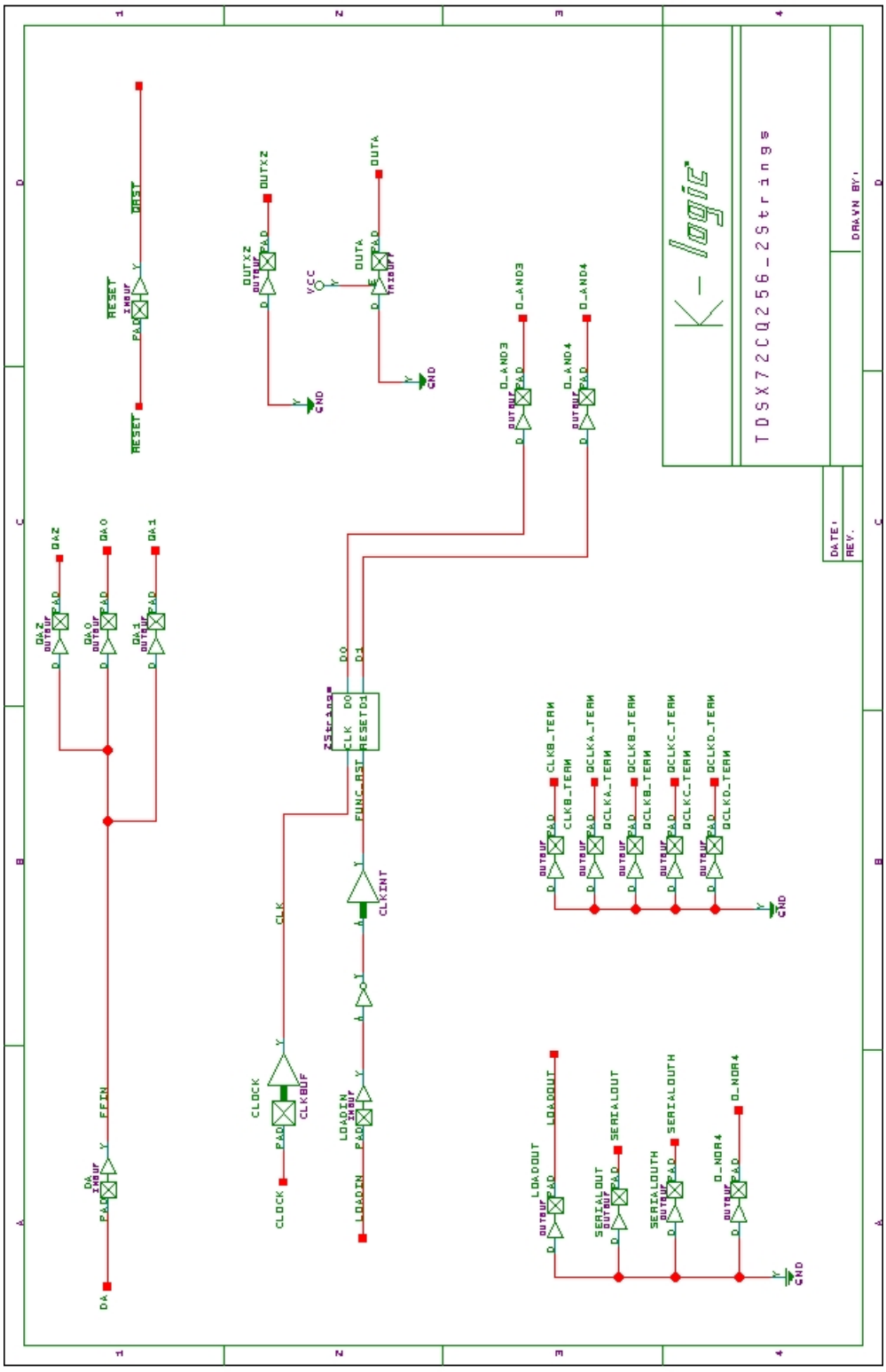
Appendix A DUT Bias

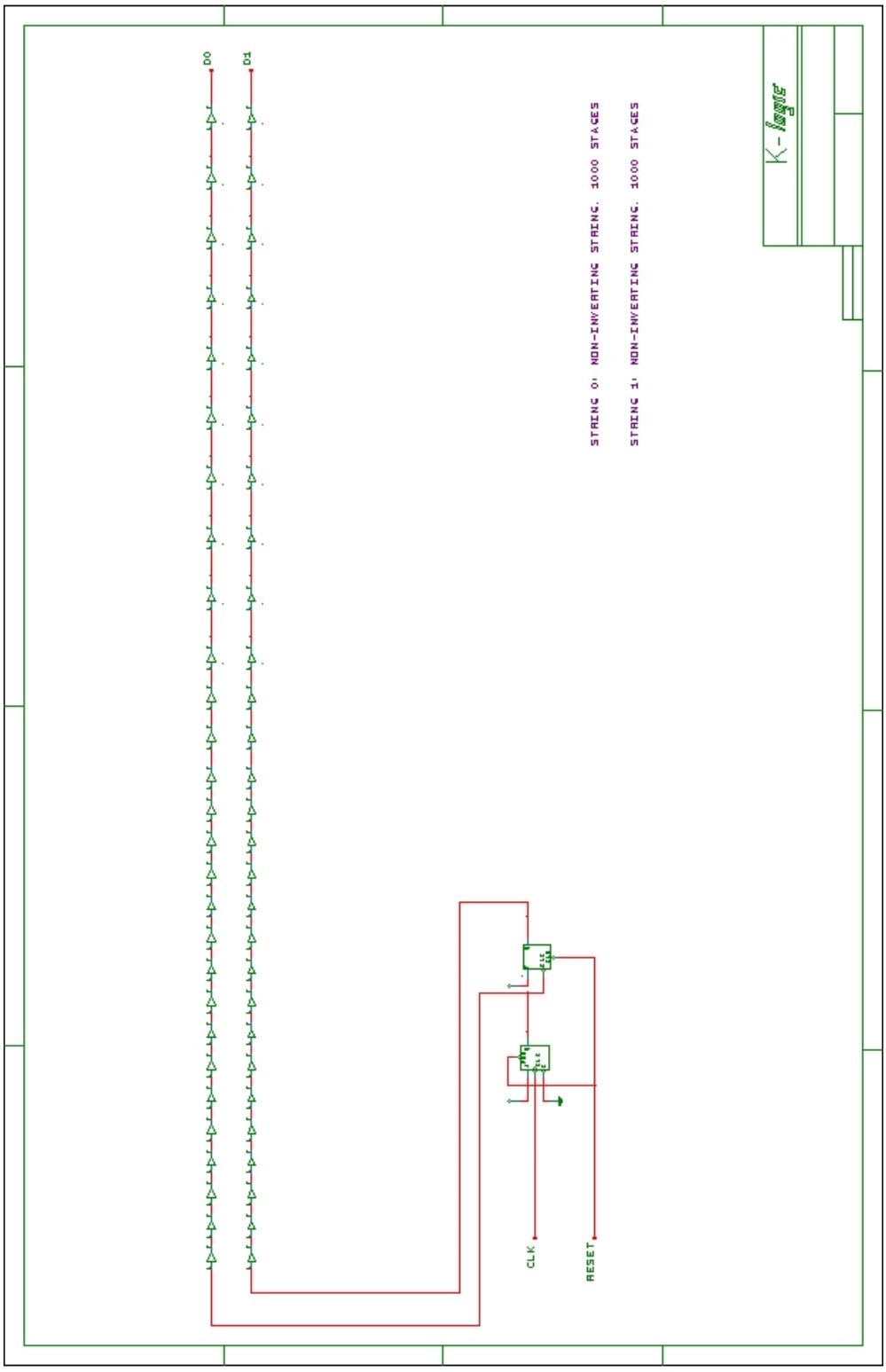


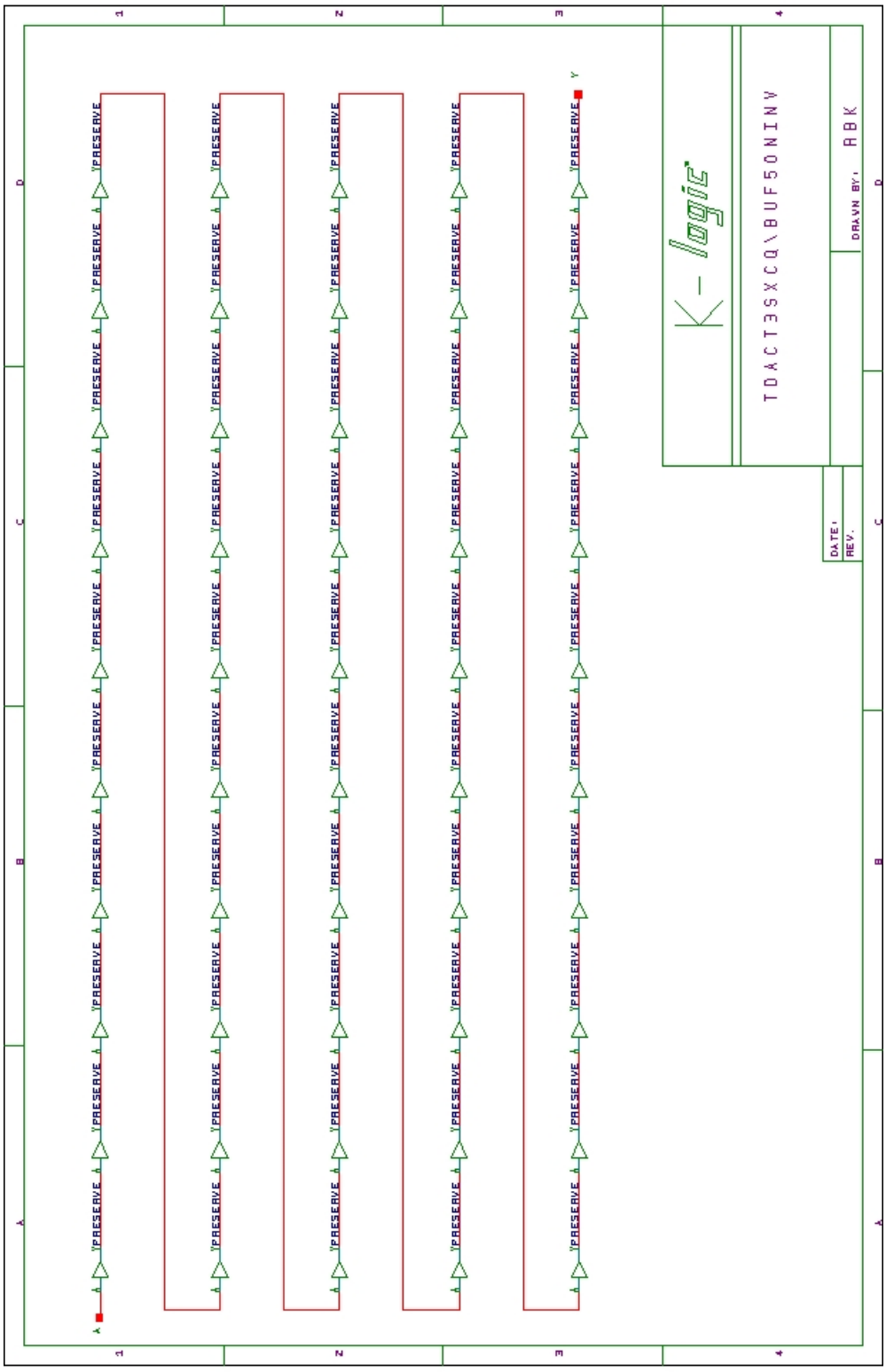

(VCCA)
VCC
(VCCI)
VCC
5X325CQ256
VCCI1
VCCI2
VCCI3
VCCI4
VCCA1
VCCA2
VCCA3
VCCA4
VCCA5
CLKA
TDI
TMS
TRST
TCK
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
10K
10K
10K
10K
10K
GND
GND

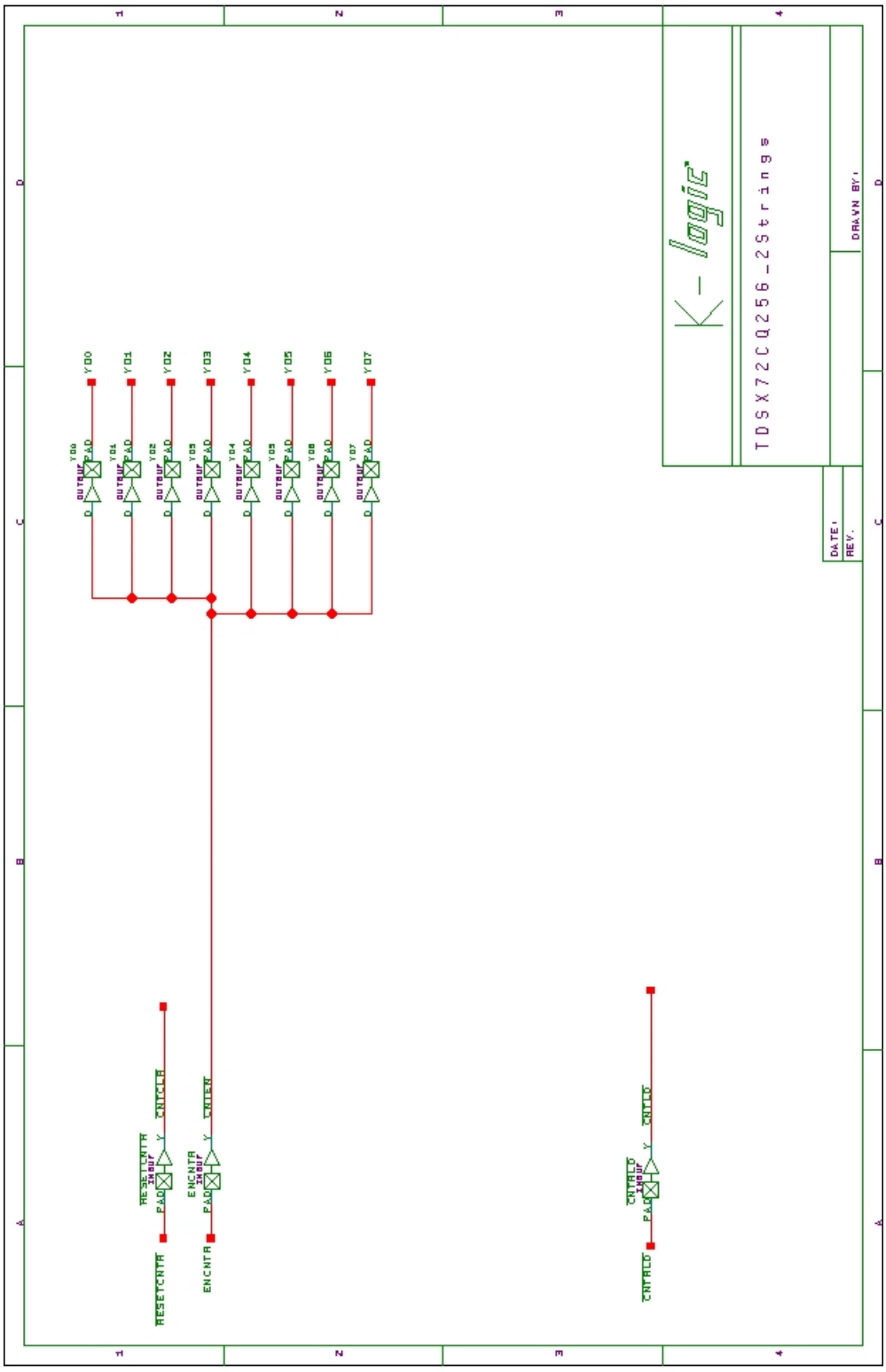
APPENDIX B DUT DESIGN SCHEMATICS (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

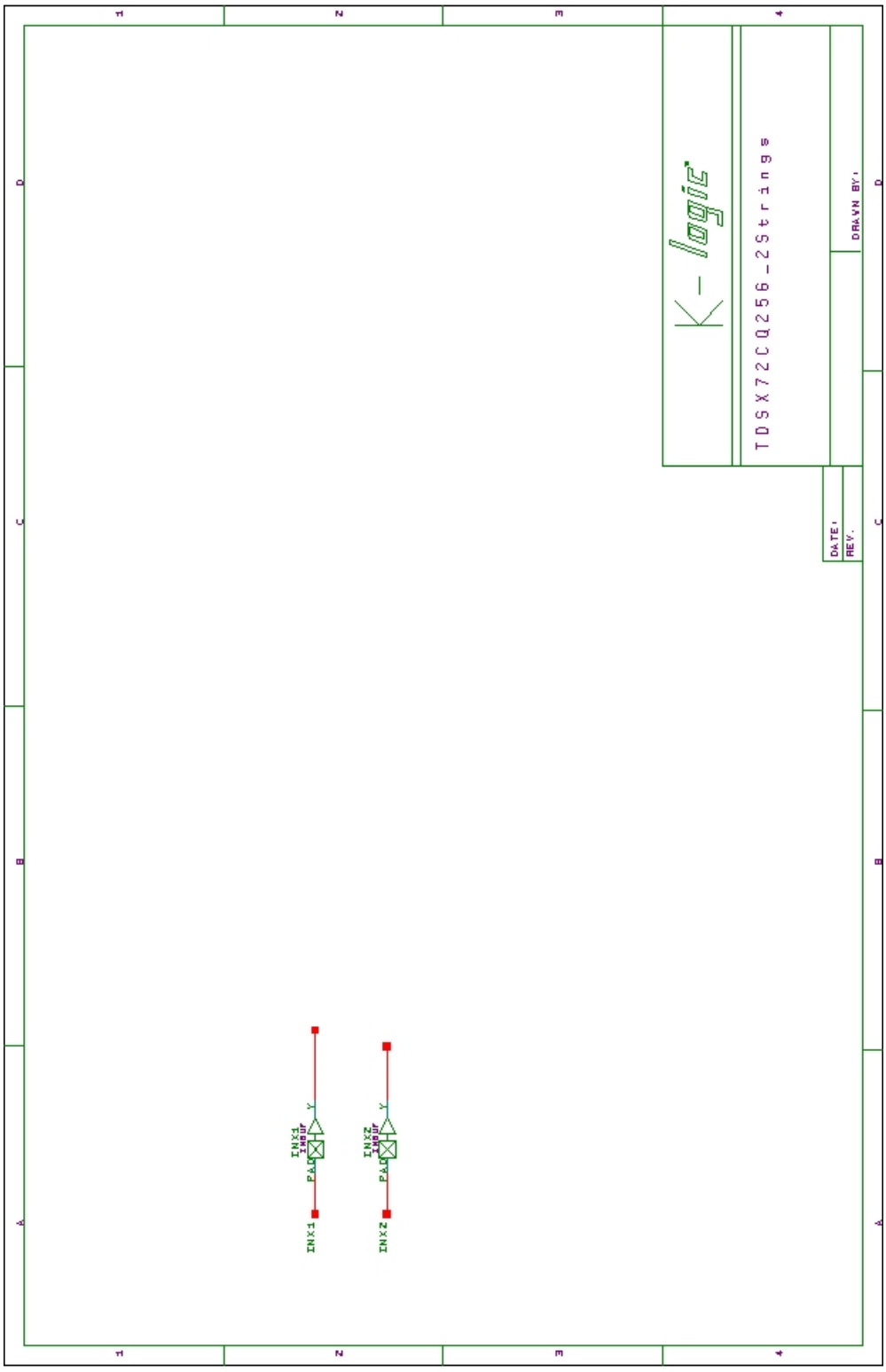


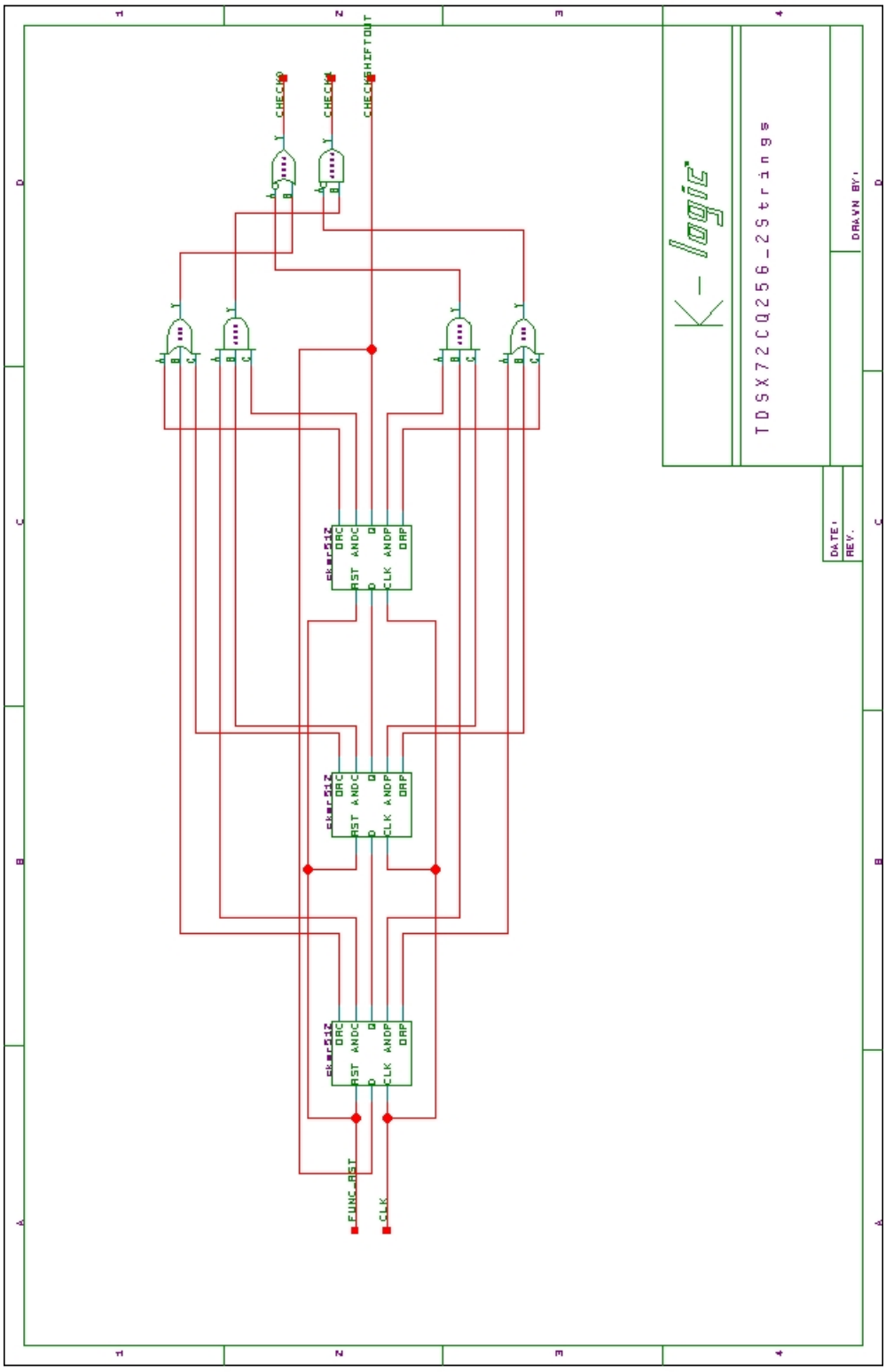

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
ZStrings
CLK
D0
D1
RESET
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
FFIN
CLKB_TERM
CLKA_TERM
CLKC_TERM
CLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

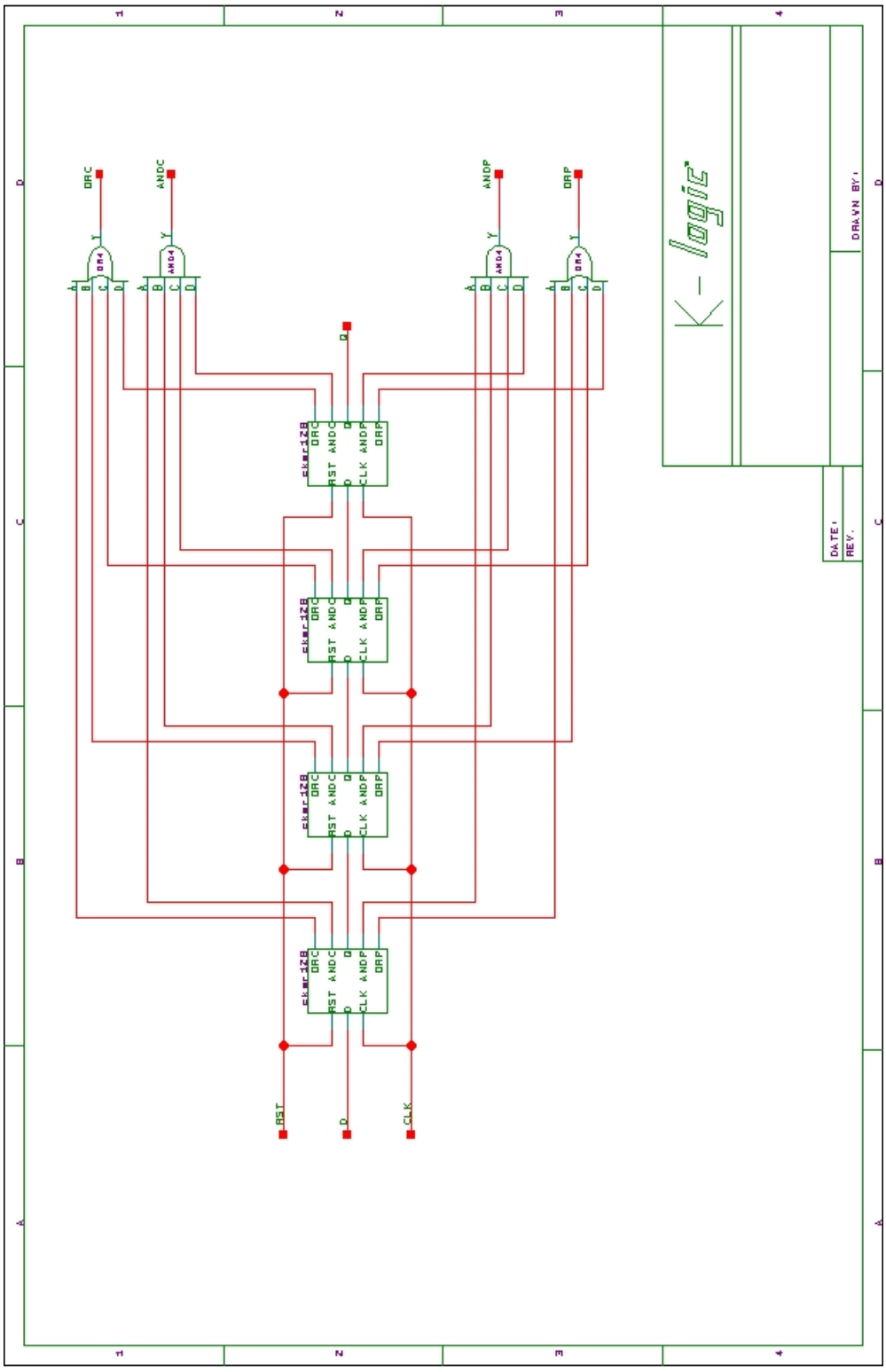

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-Logic
CLK
RESET

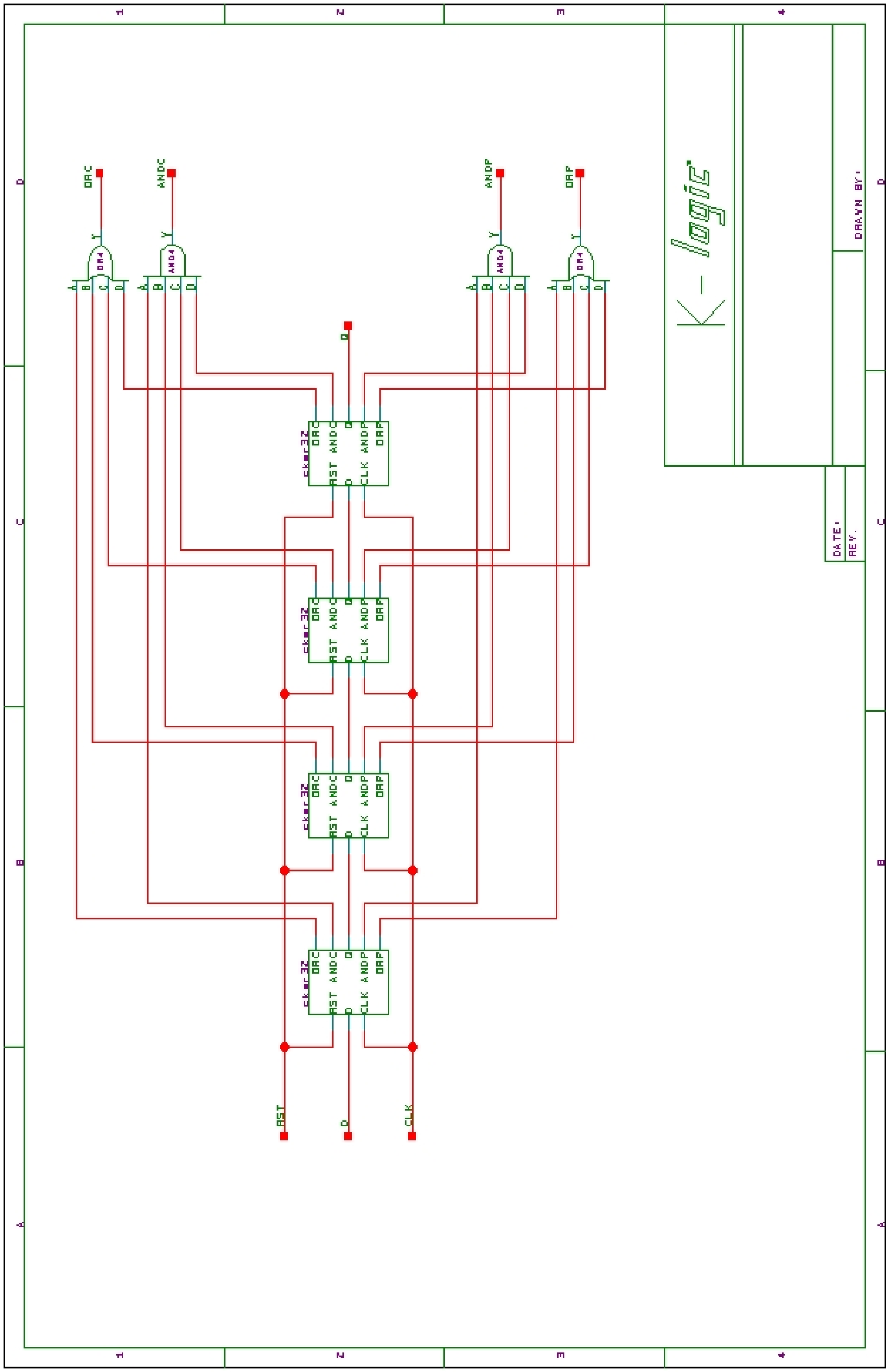

K- logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
PRESERVE

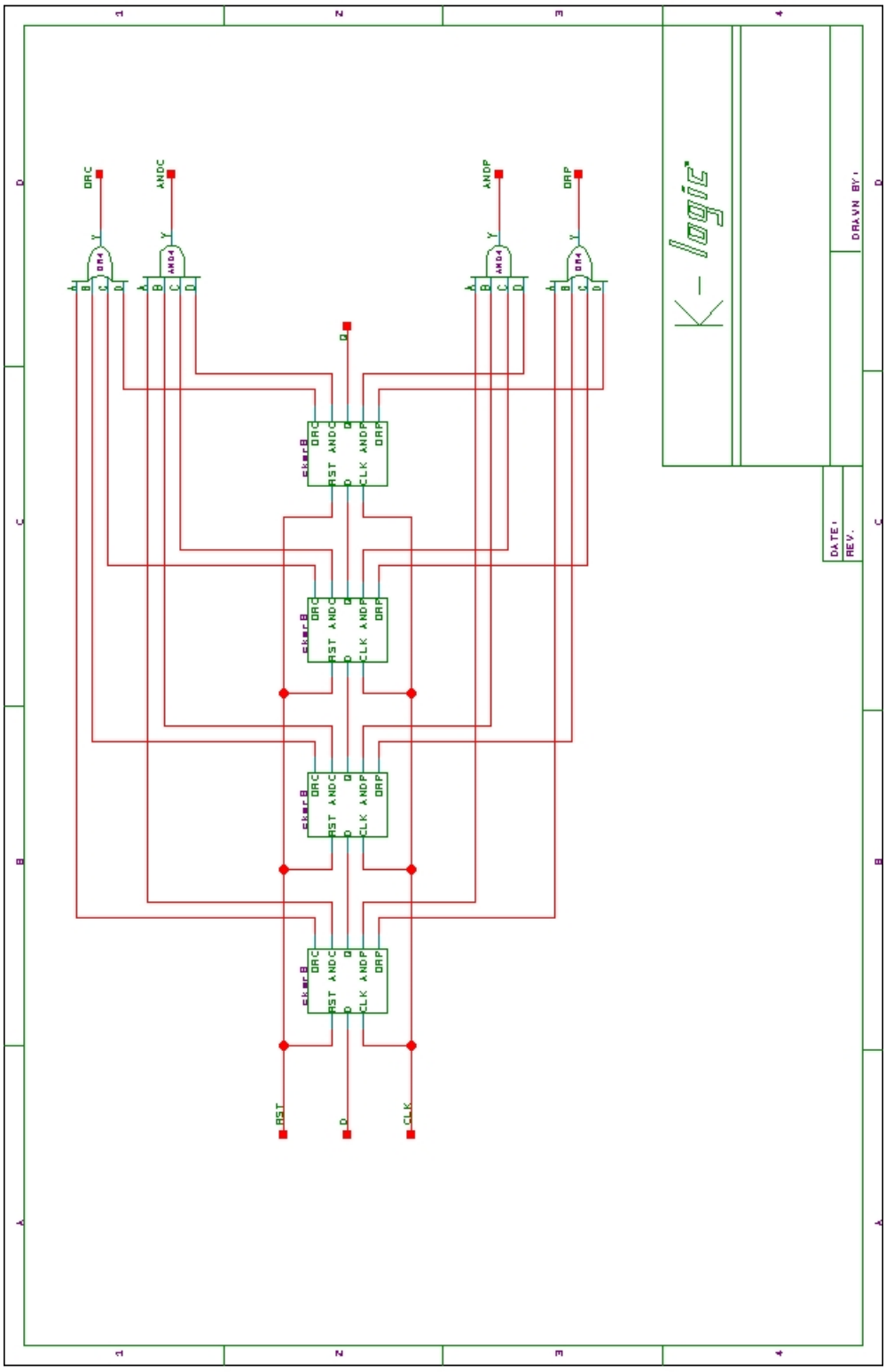

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRLD
CNTCLK
CNTEN

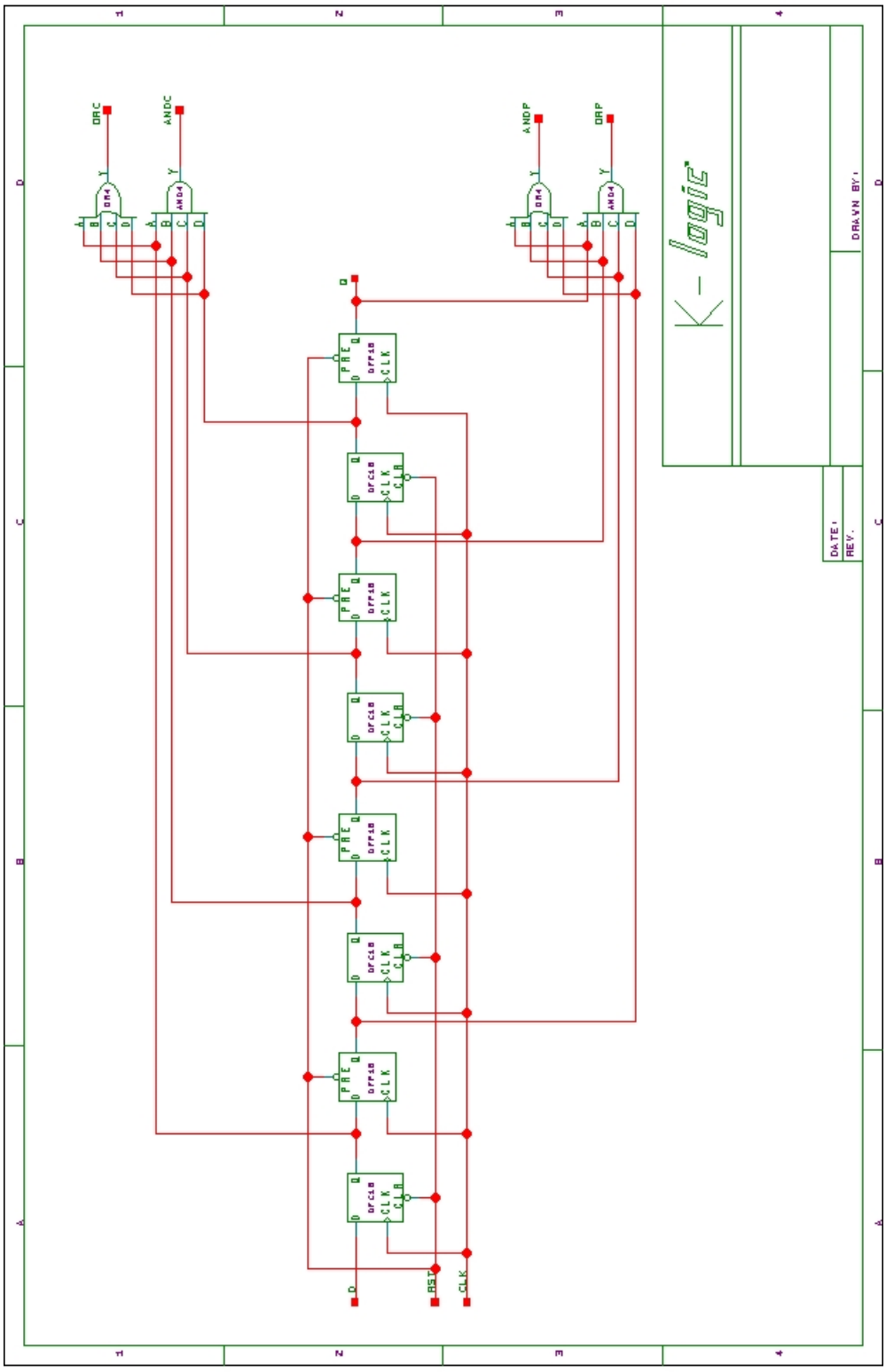

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

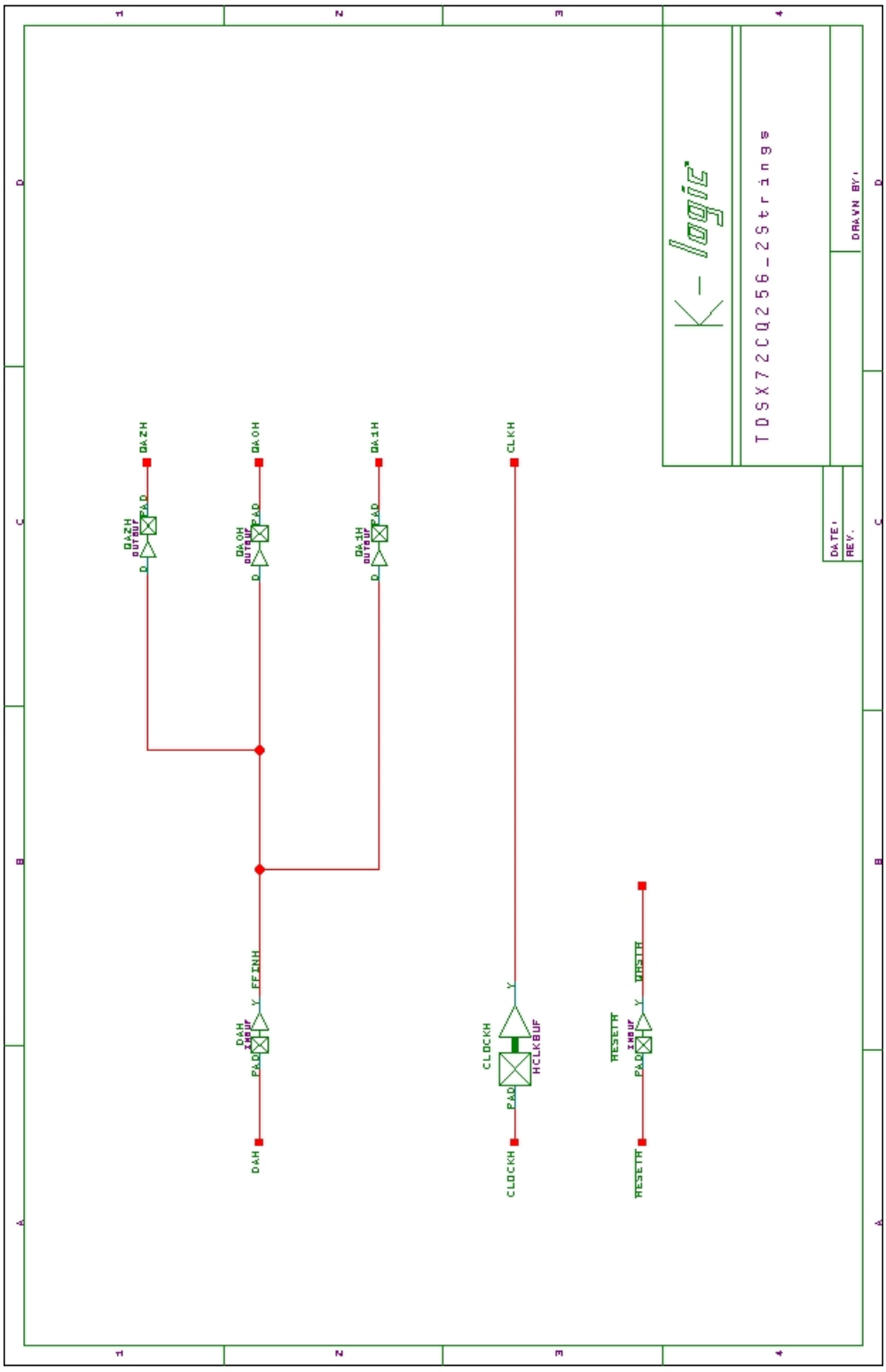

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
CHECKSHIFTOUT
CHECK0
CHECK1
FUNC_RST
CLK

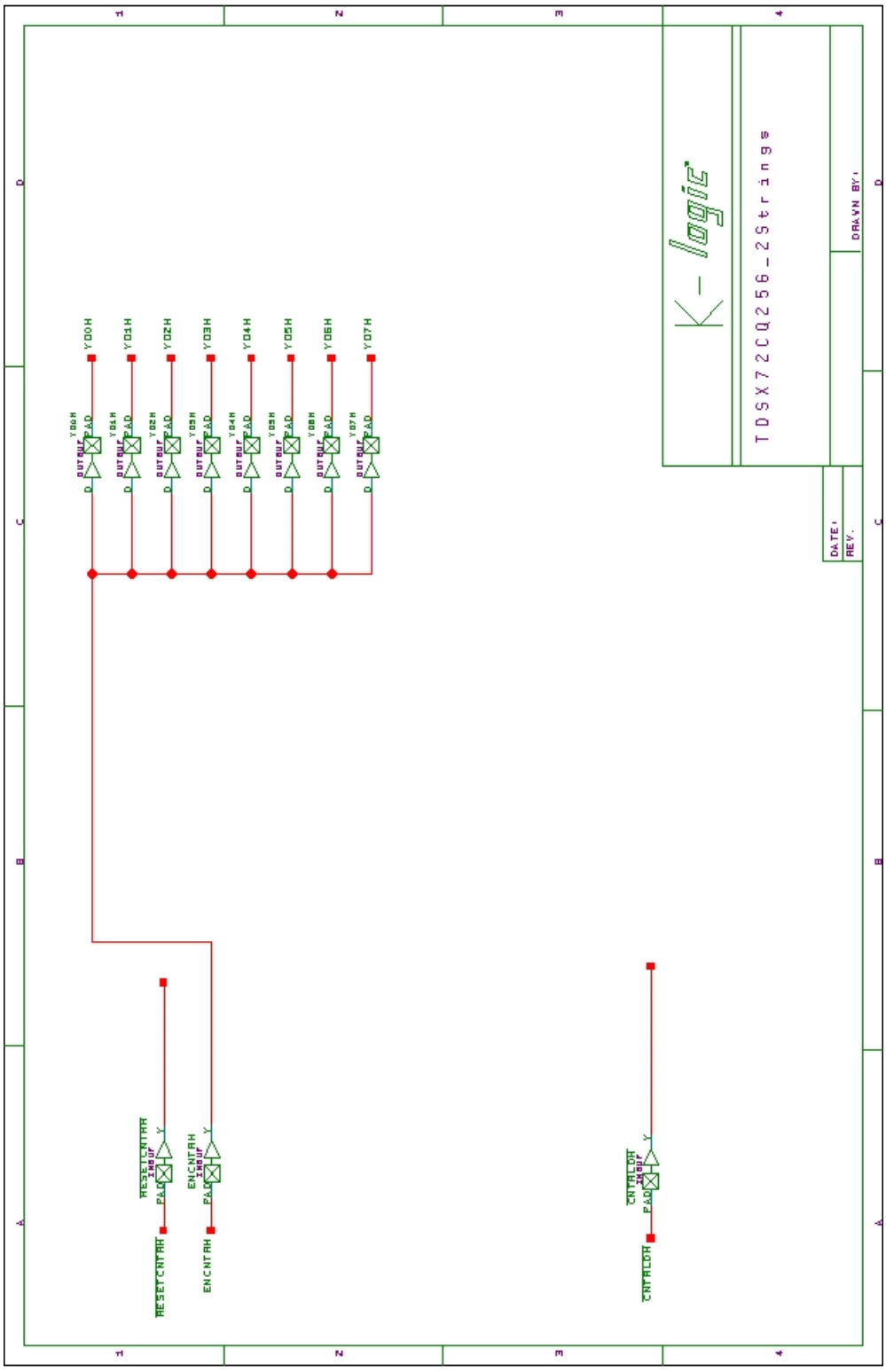

DRC
ANDC
ANDP
DRP
K - logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

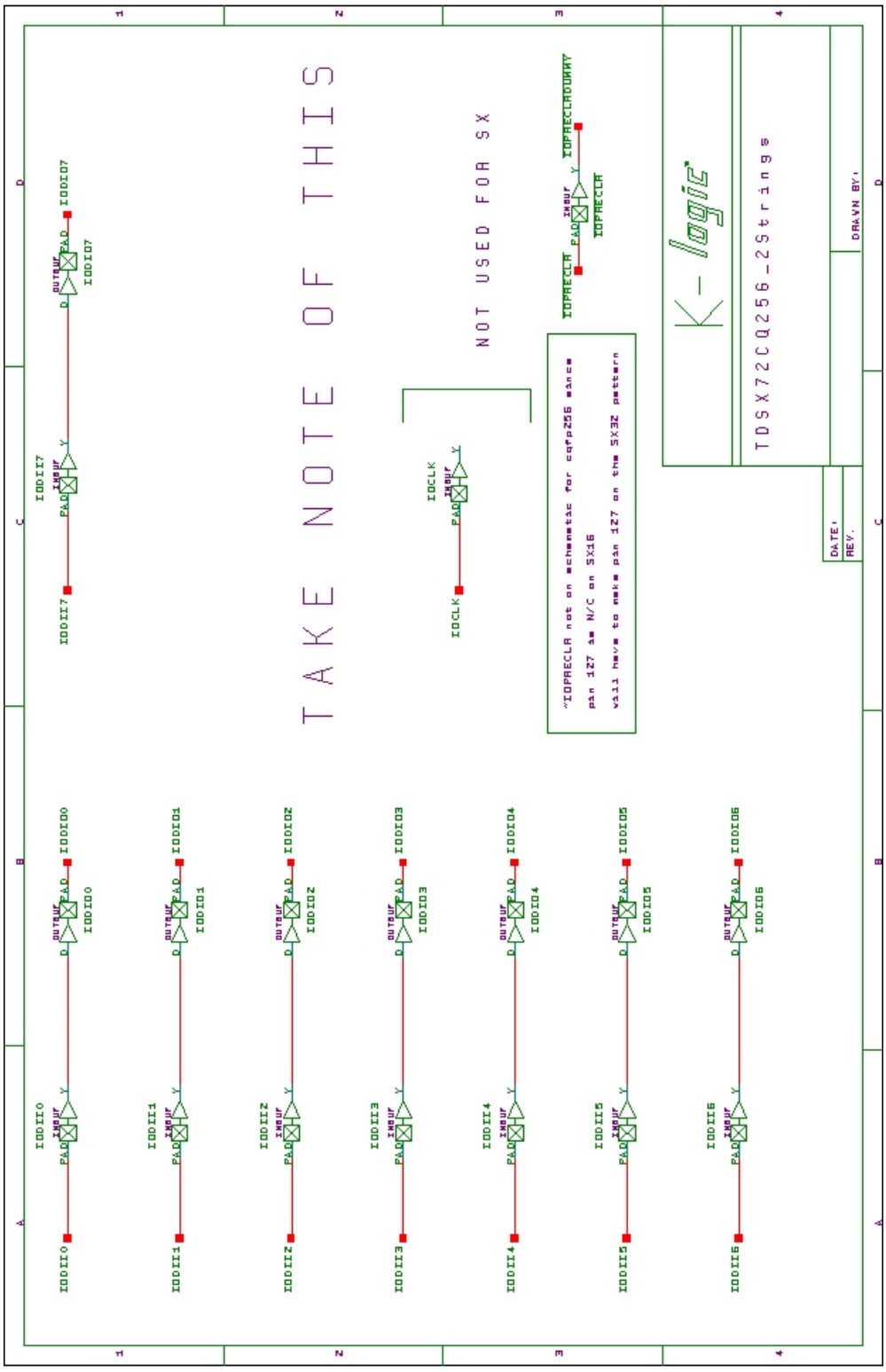

ORC
ANDC
ANDP
ORP
OR4
AND4
ckmr32
RST
D
CLK
Q
K-logic
DRAWN BY:
DATE:
REV.

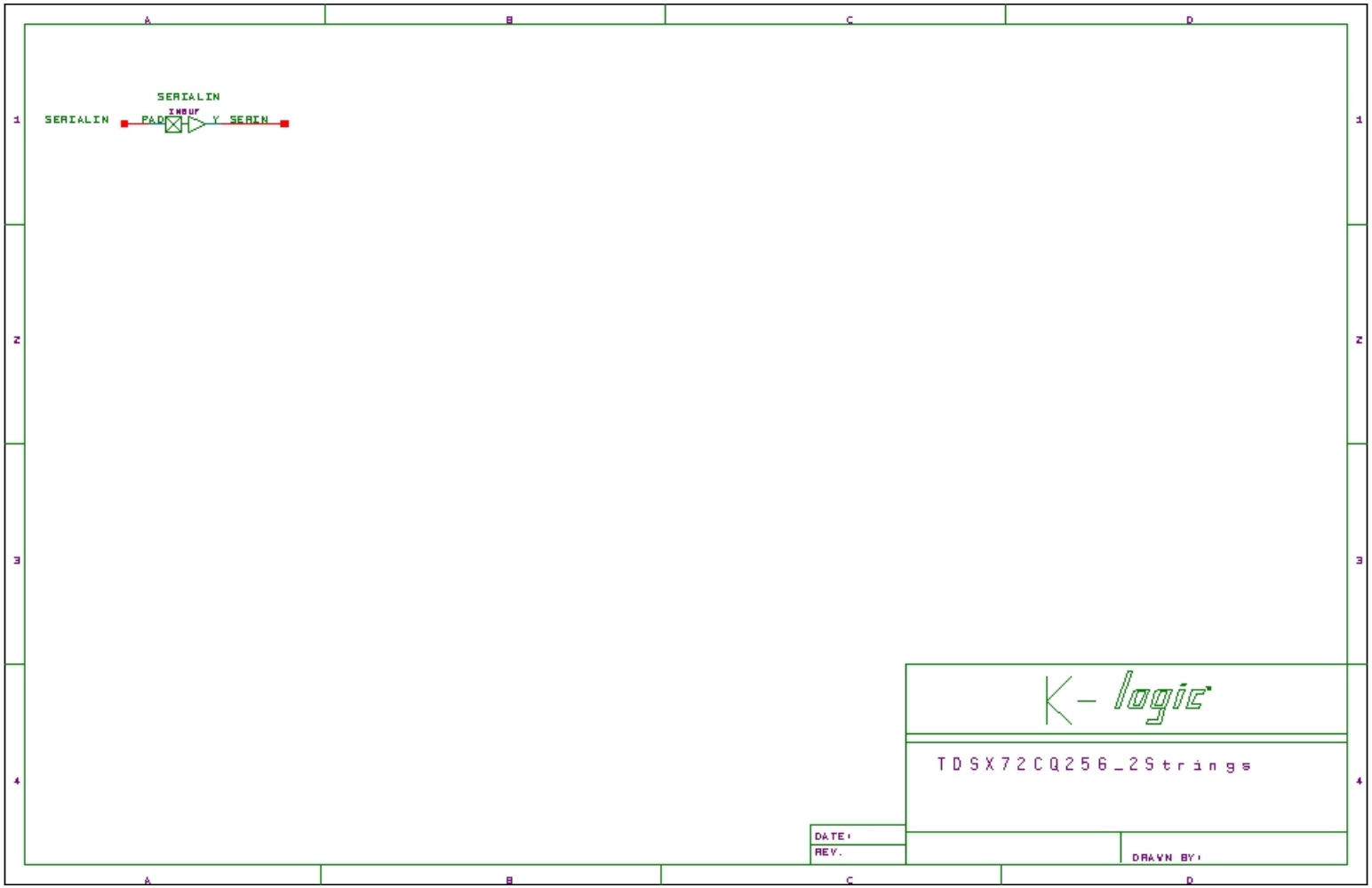

DRC
ANDC
ANDP
DRP
AND4
DR4
Y
A
B
C
D
Q
Ekar8
RST
CLK
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.


K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDF
DRF
D
RST
CLK


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH INBUF
Y FFINH
PAD
DAH
CLOCKH
Y
HCLKBUF
PAD
CLOCKH
RESETH
RESETH INBUF
Y
PAD
RESETH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H
OUTBUF
PAD
RESETCNTAH
ENCNTAH
CNTALOH
IBUF


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IODII7
IODIO7
IODCLK
IODPRECLR
IODPRECLRQUINARY
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6


SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTx1
PAD
GND