TOTAL IONIZING DOSE TEST REPORT

No. 02T-RT54SX72S-T25KS004

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I. SUMMARY TABLE

Parameter	**Tolerance**
1. Gross Functionality	Passed 100 krad(Si)
2. $I_{DDSTDBY}$ (static I_{CC})	~100 mA after 100 krad(Si) irradiation and 2 weeks annealing
3. Input Threshold (V_T)	Passed 100 krad(Si)
4. Output Drives (V_{OL}/V_{OH})	Passed 100 krad(Si)
5. Propagation Delays	Worst case (1000 inverter stages) degradation = 25% after 100 krad(Si) and annealing
6. Transition Time	No abnormality after 100 krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT information and irradiation conditions

Part Number	RT54SX72S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 μm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	T25KS004
Quantity Tested	5
Serial Number	14070, 14098, 14111, 14122, 14178
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad(Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	5.0 V/2.5 V

B. Test Method

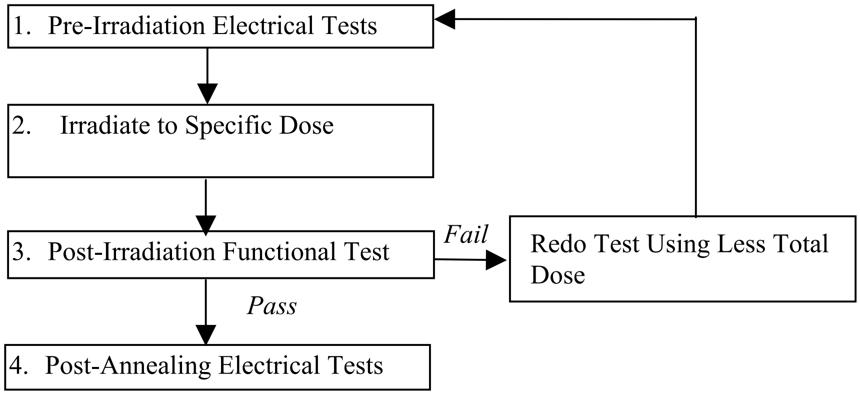

1. Pre-Irradiation Electrical Tests
2. Irradiate to Specific Dose
3. Post-Irradiation Functional Test
Fail
Redo Test Using Less Total Dose
Pass
4. Post-Annealing Electrical Tests

Fig 1 Parametric test flow chart

There are two types of radiation test regularly performed by Actel. For "functional test", the DUT is irradiated to the total dose level at which the gross functional failure occurs. This total dose level is determined as the tolerance for functional failure (the first data row in the summary table). The tests for AC/DC parameters are called "parametric tests." It follows the military standard test method 1019.5. Fig 1 shows the testing flow. In a previous product (RT54SX32S) manufactured by the same 0.25 µm CMOS process, the time dependent effect (TDE) was evaluated by comparing the results of a high dose rate (1 krad(Si)/min) against the results of a low dose rate (1 krad(Si)/hr). No adverse TDE was observed. Thus, the accelerated aging (rebound test) is omitted in this report.

C. Electrical Parameter Measurements

1) Type 1-Functional Test

In-flux measurements are performed to monitor the functionality. The parameters usually include I_{CC}, output voltage of combinatorial circuits and sequential circuits, and the propagation delay of an inverter string. However, in this report, only I_{CC} is monitored in-flux because of the limited space in the gamma cell.

2) Type 2-Parametric Tests

A high utilization design (in this report, TDSX72CQ256_2Strings) to address total dose effects in typical space applications is used. The circuit schematics are shown in appendix A.

Table 2 lists the electrical parameters measured in the parametric tests. The functionality is measured pre-irradiation, post-irradiation, and post-annealing on the output pin (O_AND3 or O_AND4) of the two combinatorial inverter-strings and on the output pin (O_OR4 and O_NAND4) of the shift register. The I_{CC} is measured in-flux on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. During annealing, the I_{CC} of one DUT (S/N number 14178) is monitored independently. The other four DUT are grouped on a burn-in board and their total I_{CC} is monitored.

The input logic thresholds (V_T) and output drives (V_{OH}/V_{OL}) are measured pre-irradiation and post-annealing on a combinatorial net, the input pin DA to the output pin QA0. The propagation delays are measured pre-irradiation and post-annealing on one of the output of the global combinatorial inverter string, which has 1000 inverters. The delay is defined as from the input CLOCK to the output pin O_AND4. The transient time is measured pre-irradiation and post-annealing on the same design. The global combinatorial inverter strings are controlled by clocked flip-flops during the propagation delay and transient measurements.

Unused inputs are grounded with a 1M ohm resistor during irradiation and a 1.2K ohm resistor during annealing.

Table 2. Logic design for parametric tests

Parameter/Characteristics	**Logic Design**
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC}	DUT power supply
3. Input Threshold (V_T)	TTL compatible input buffer (pin DA to QA0)
4. Output Drives (V_{OH}/V_{OL})	TTL compatible output buffer (pin QA0)
5. Propagation Delays	String of 1000 inverters (pin LOADIN to O_AND4)
6. Transition Time	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Type 1-Functional Test

As mentioned above, the in-flux monitoring only includes I_{CC} in this test. Because the high dose rate enhances the radiation-induced leakage, every DUT was only irradiated to 100 krad(Si). Bench tests confirmed that all the DUT were functional right after irradiation. The plots of in-flux I_{CC} are shown in Fig 2-6. They display typical I_{CC} versus total dose characteristic.

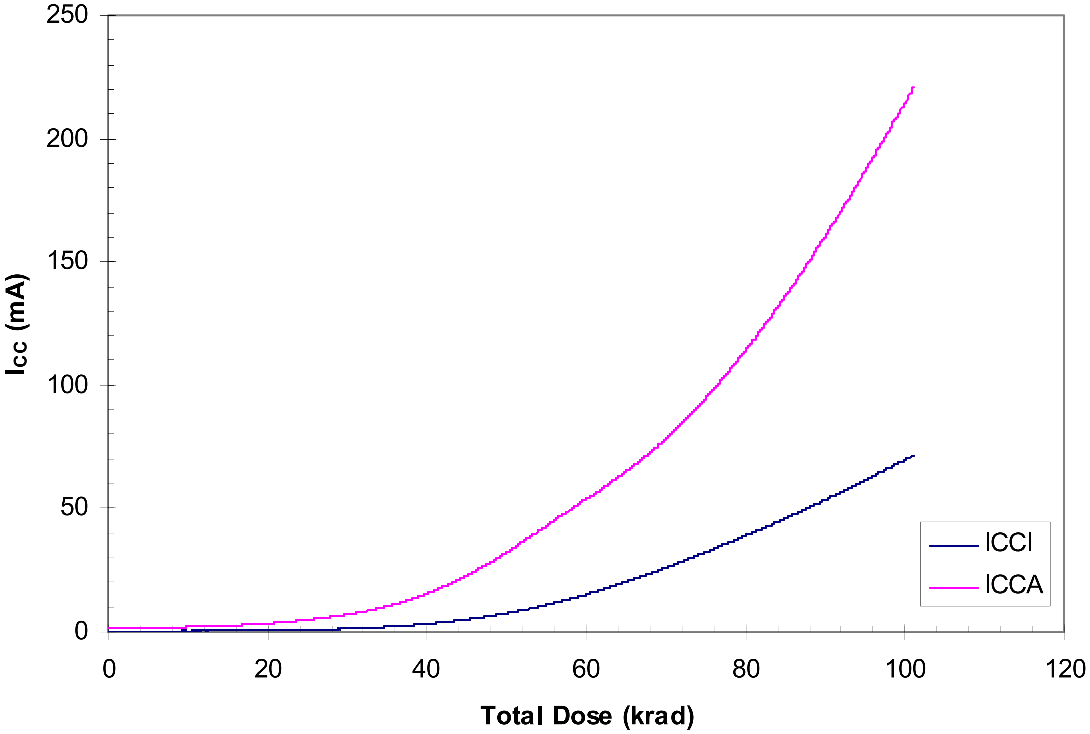


Fig 2 In-flux I_{CC} of DUT 14070

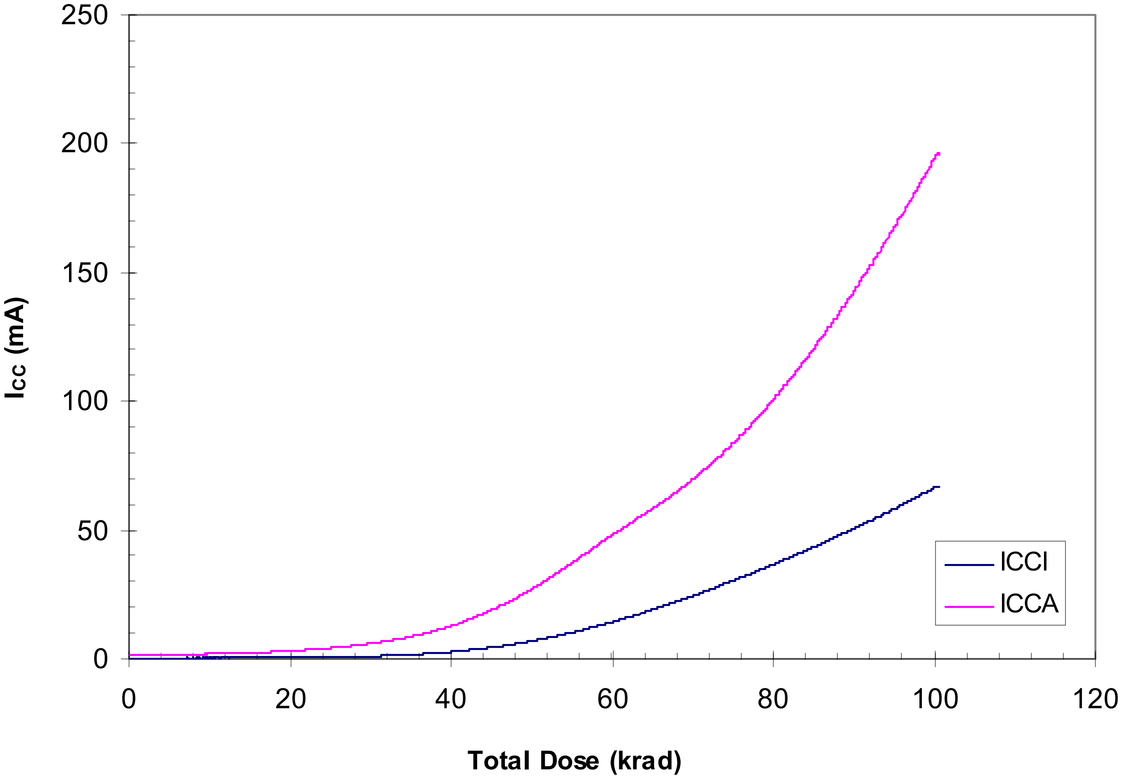


Fig 3 In-flux I_{CC} of DUT 14098

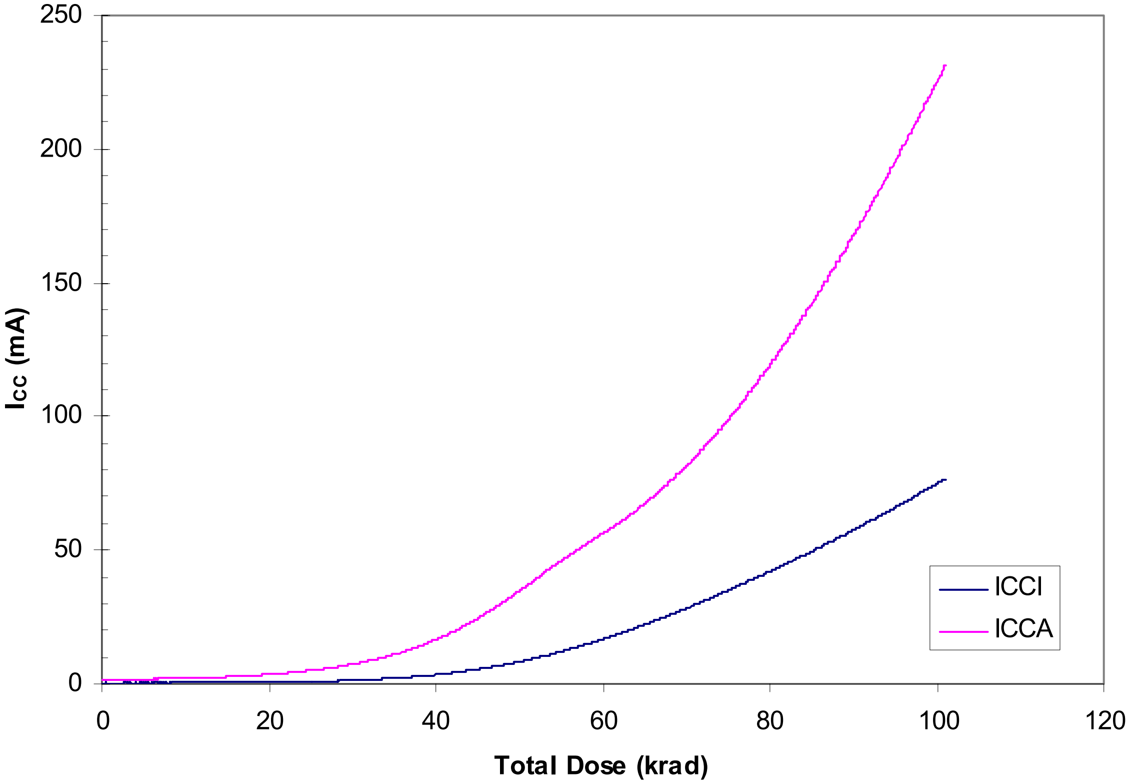


Fig 4 In-flux of DUT 14111

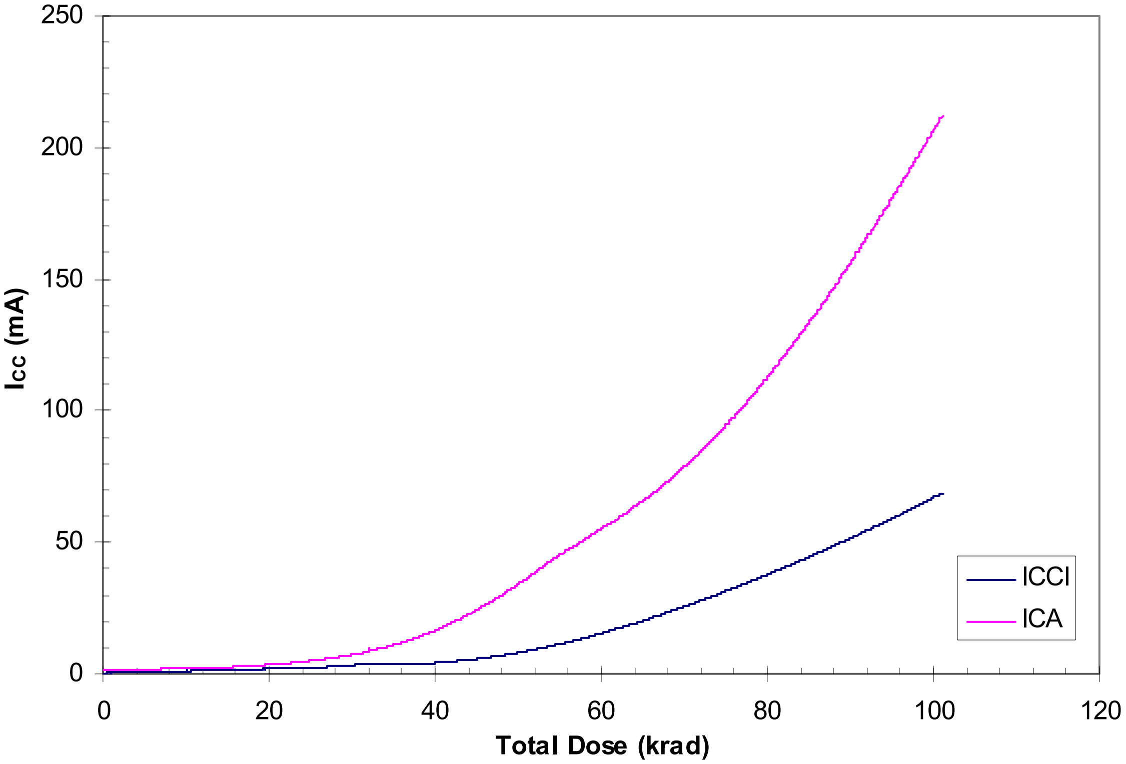


Fig 5 In-flux I_{CC} of DUT 14122

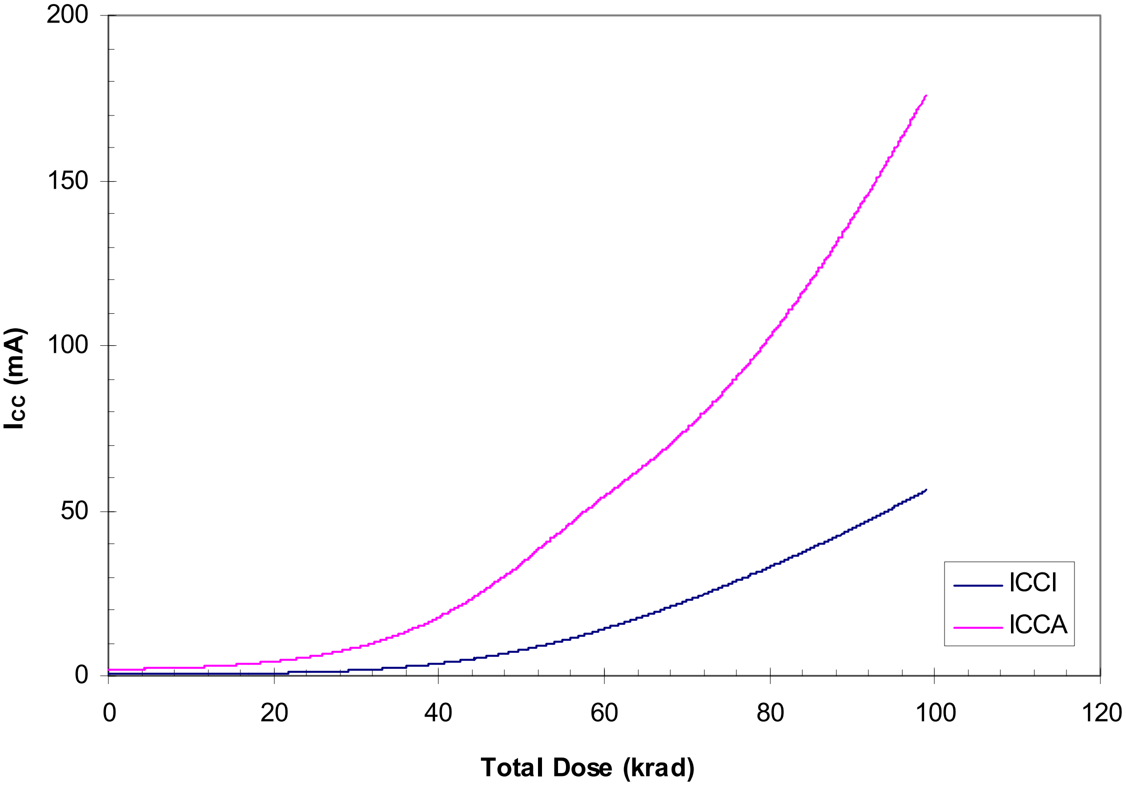


Fig 6 In-flux I_{CC} of DUT 14178

B. Type 2-Parametric Test

1) Functionality

The functionality of each DUT passes at pre-irradiation, post-irradiation, and post-annealing.

2) Standby I_{CC}

Fig 7 shows an annealing curve of DUT 14178. After two weeks of room temperature annealing, I_{CC} dropped approximately one third, from 180 mA to 120 mA. We extrapolate the annealing curve as a straight line on the log scale and assume that the slope for different as-irradiated doses is the same. If after annealing, the I_{CC} reaches the 25 mA spec, the as-irradiated I_{CC} calculated by the annealing rate is 37.5 mA, and the corresponding total dose can be extracted from in-flux data and listed in Table 3.

The extracted tolerance is lower than that in the previous lot, such as T25KS005, because the present dose rate for the gamma cell utilized is 60 times higher than the previously used gamma cell. Room temperature annealing at 2.5 V for this 0.25 µm technology appears to be significantly slower than that of the 5 V biased 0.8 µm technology.

Table 3 Minimum bounded total dose where the projected post-annealing I_{CCA} will reach 25 mA

DUT	Total Dose
14070	49.0 krad(Si)
14098	51.0 krad(Si)
14111	48.0 krad(Si)
14122	48.2 krad(Si)
14178	48.3 krad(Si)

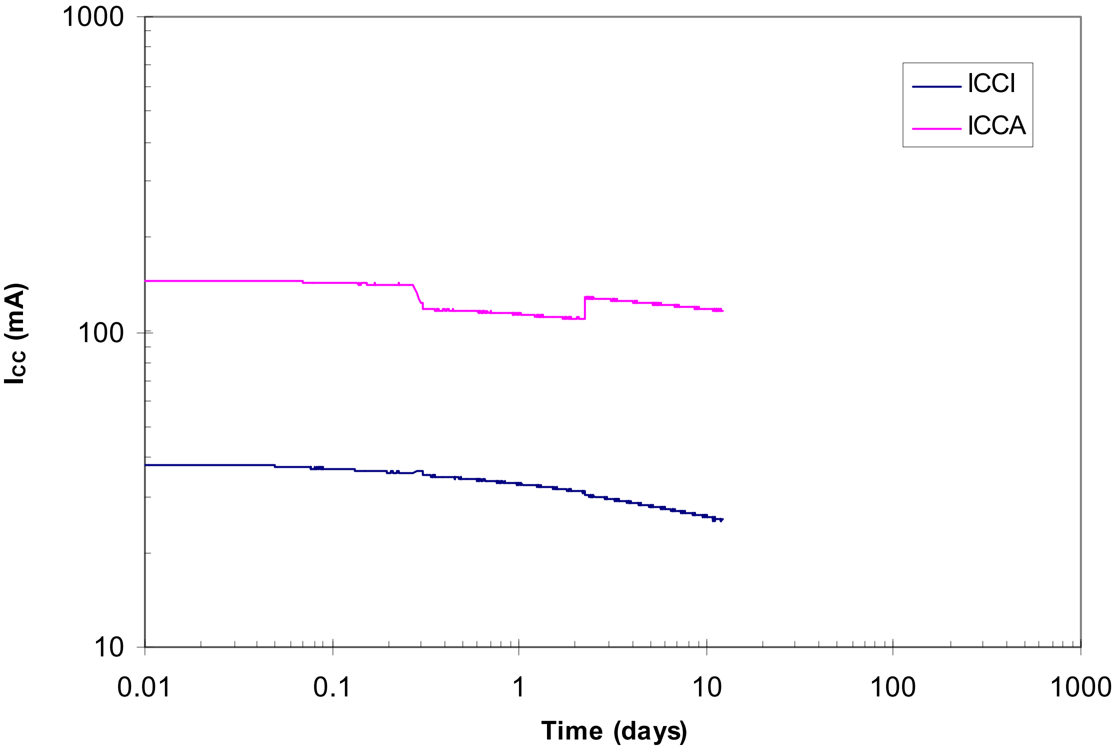


Fig 7 I_{CC} annealing curve of DUT 14178

3) *Input Logic Threshold*

Table 4 lists the pre-irradiation and post-annealing input logic threshold for each DUT. The radiation effect is less than 10%.

Table 4 Pre-irradiation and post-annealing input logic threshold

DUT	Pre-Irradiation		Post-Annealing	
	V_{LH}	V_{HL}	V_{LH}	V_{HL}
14070	1.38V	1.42V	1.38V	1.42V
14098	1.38V	1.42V	1.41V	1.43V
14111	1.38V	1.42V	1.39V	1.44V
14122	1.38V	1.42V	1.38V	1.44V
14178	1.38V	1.42V	1.45V	1.48V

4) *Output Characteristics*

The pre-irradiation and post-annealing V_{OH}/V_{OL} are measured and listed in table 5 and 6. In every case, the DUT passes the spec limit.

Table 5 Pre-irradiation and post-annealing V_{OH} at various sourcing current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
14070	4.99V	4.99V	4.87V	4.87V	4.67V	4.67V	4.15V	4.14V	3.10V	3.07V
14098	4.99V	4.99V	4.87V	4.87V	4.67V	4.66V	4.13V	4.11V	3.05V	3.01V
14111	4.99V	4.98V	4.87V	4.87V	4.67V	4.66V	4.15V	4.12V	3.10V	3.03V
14122	4.99V	4.98V	4.87V	4.87V	4.67V	4.66V	4.15V	4.12V	3.12V	3.05V
14178	4.99V	4.98V	4.87V	4.87V	4.67V	4.67V	4.15V	4.14V	3.11V	3.07V

Table 6 Pre-irradiation and post-annealing V_{OL} at various sinking current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
14070	0.01V	0.01V	0.1V	0.1V	0.17V	0.17V	0.42V	0.44V	0.86V	0.91V
14098	0.01V	0.01V	0.1V	0.1V	0.17V	0.17V	0.42V	0.43V	0.87V	0.88V
14111	0.01V	0.01V	0.1V	0.1V	0.17V	0.17V	0.42V	0.43V	0.86V	0.88V
14122	0.01V	0.01V	0.1V	0.1V	0.17V	0.17V	0.43V	0.43V	0.88V	0.89V
14178	0.01V	0.01V	0.1V	0.1V	0.17V	0.17V	0.42V	0.43V	0.87V	0.88V

5) Propagation Delays

Table 7 lists the pre-irradiation and post-annealing propagation delays and radiation-induced degradations in percentages. The larger than usual degradation is due to the high dose rate employed in this test. To conservatively estimate the propagation delay degradation at various dose levels, a typical low dose rate curve (Fig 8) can be used. Piece-wise linearly fit this curve into two regions. Region 1 has the zero slope from 0 krad to 40 krad. Region 2 has the slope:

$$Slope = \frac{TPD(Max\ Dose) - TPD(Initial)}{Maximum\ Dose - 40krad}$$

Use this equation and apply 10% degradation as the tolerance limit, the worst tolerance point is 63.2 krad(Si). However, user should notice that the design to measure the delay has 1000 inverter stages. An unpublished test shows that even when the high dose rate gamma cell is used, the degradation after 100 krad(Si) was well below 10% for a more typical design of 10 inverter stages. The very large, but impractical, inverter chain used in this test shows the extreme case of a very large radiation-induced propagation-delay degradation.

Table 7 Propagation delays (ns)

DUT	Rising Output			Falling Output		
	Pre-Irrad	Post-Ann	Degradation	Pre-Irrad	Post-Ann	Degradation
14070	1295.83	1560.64	20.4%	1125.71	1356.25	20.5%
14098	1301.62	1558.17	19.7%	1139.40	1375.67	20.7%
14111	1283.64	1594.48	24.2%	1118.50	1407.28	25.8%
14122	1284.40	1535.31	19.5%	1123.54	1338.59	19.1%
14178	1289.81	1523.65	18.1%	1119.47	1344.04	20.1%

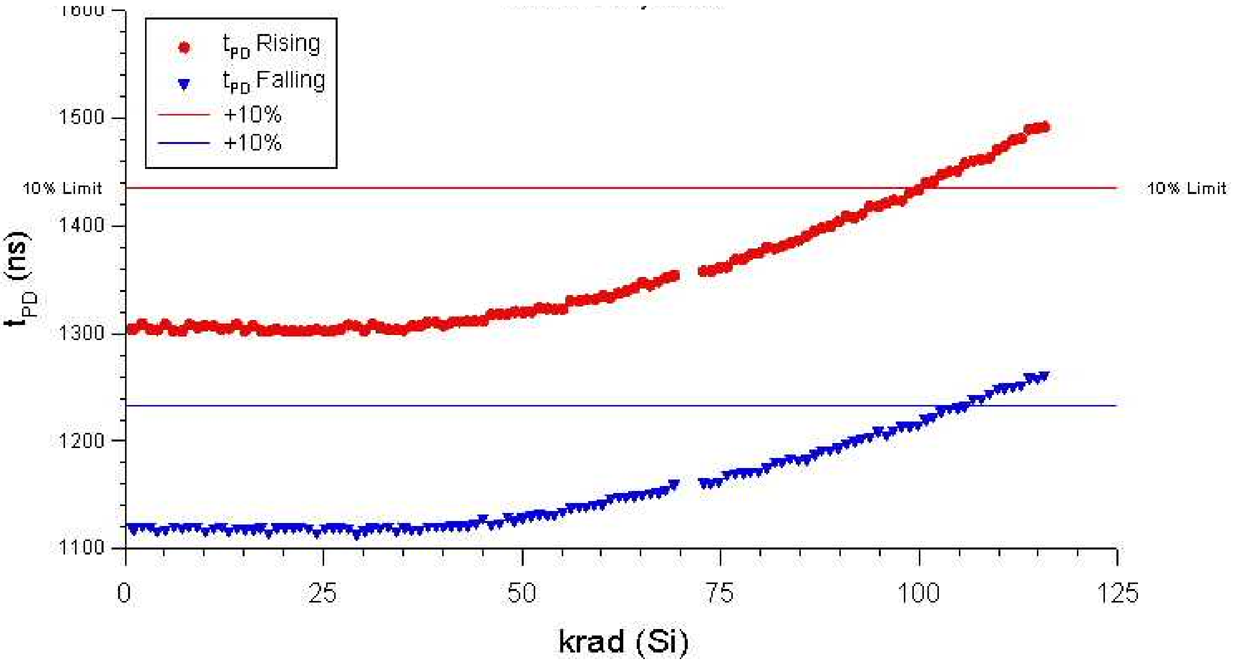


Fig 8 Propagation delay versus total dose for a typical low dose rate (1 krad/hr) test

6) Transition Time

The pre-irradiation and post-annealing rising and falling edges are plotted in Fig 9-18. Unless otherwise stated the voltage scale in these plots is 2 V/div, and the time scale is 1 ns/div. The radiation-induced degradation is apparent in every case and it contributes to the propagation delay measured in the previous section. Rising edge has approximately the same degradation as the falling edge. No other abnormality can be identified.

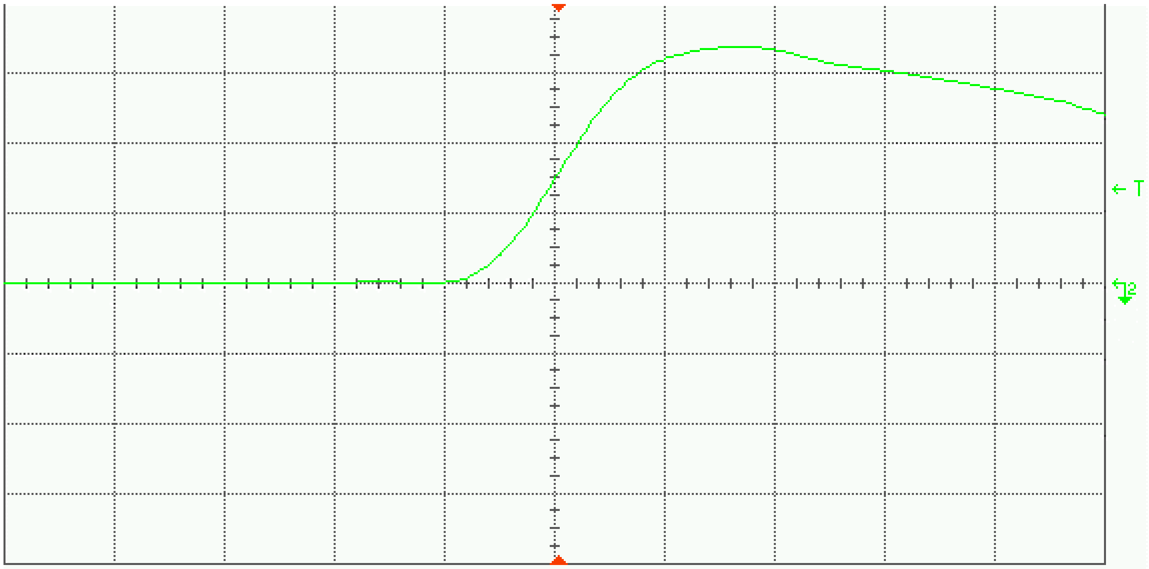


Fig 9(a) Pre-irradiation rising edge of DUT 14070

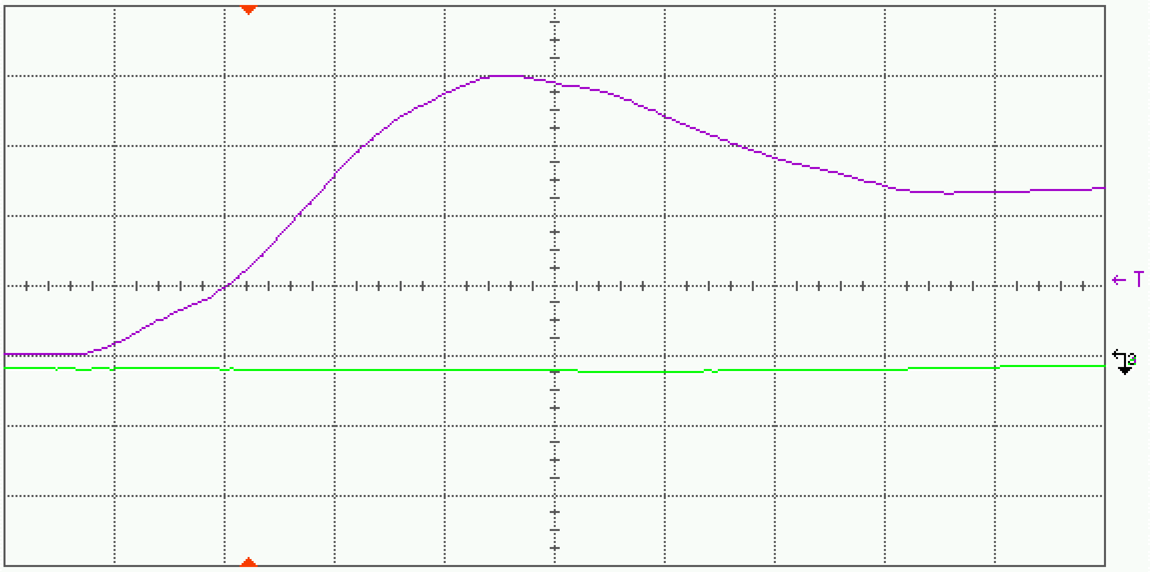


Fig 9(b) Post-annealing rising edge of DUT 14070

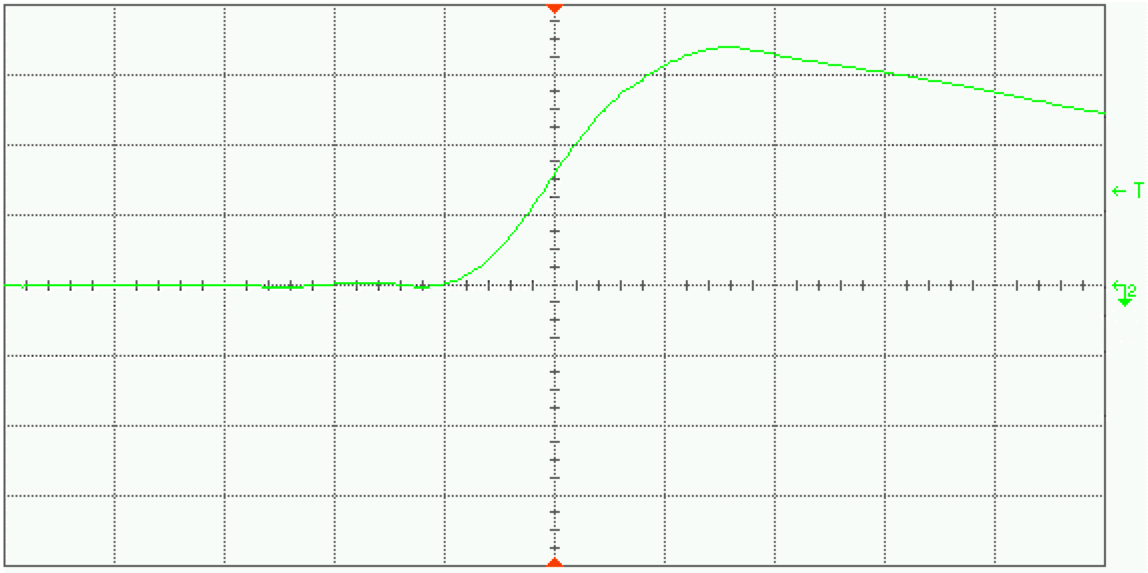


Fig 10(a) Pre-irradiation rising edge of DUT 14098

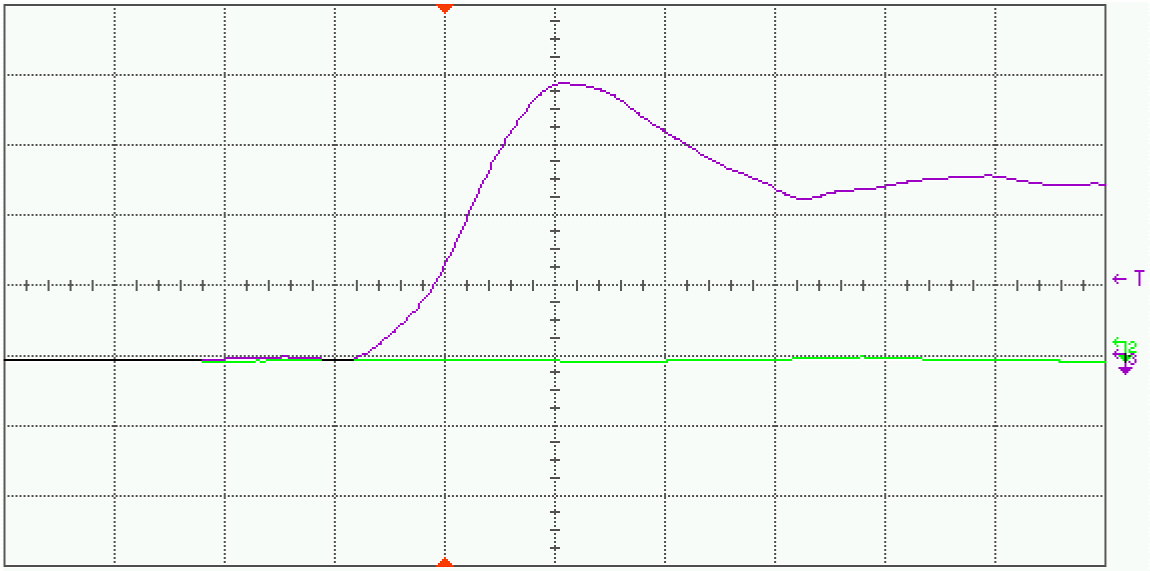


Fig 10(b) Post-annealing rising edge of DUT 14098, notice that the time scale is 2 ns/div.

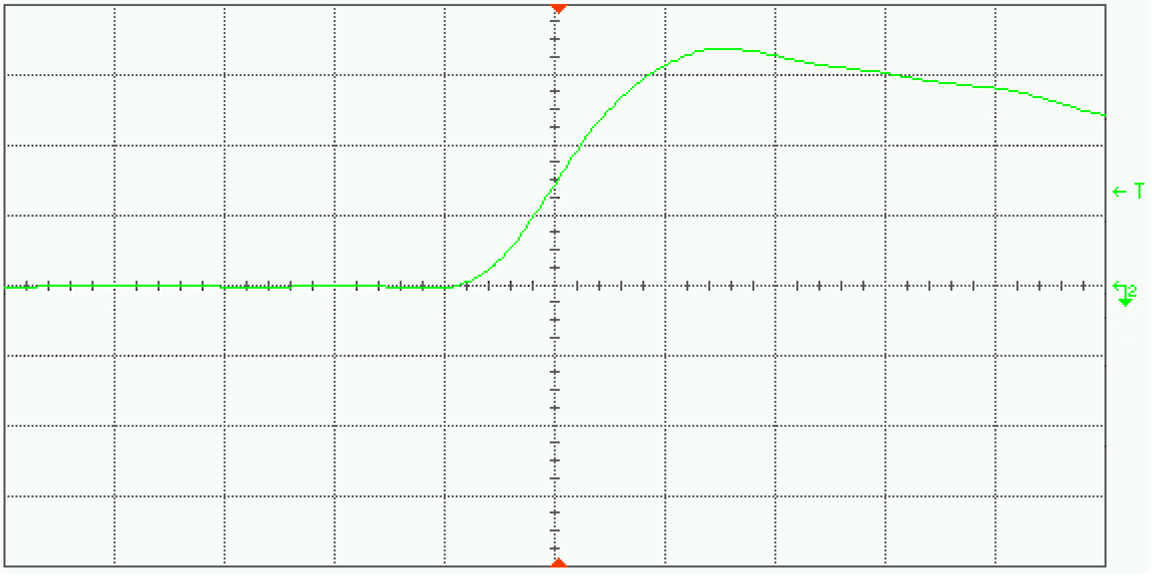


Fig 11(a) Pre-irradiation rising edge of DUT 14111

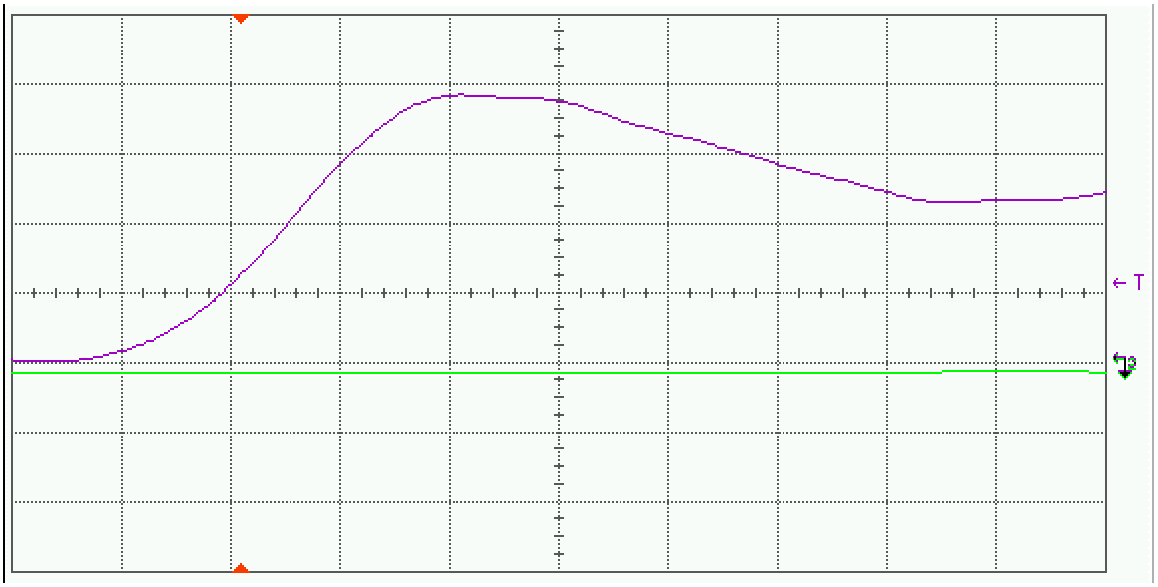


Fig 11(b) Post-annealing rising edge of DUT 14111

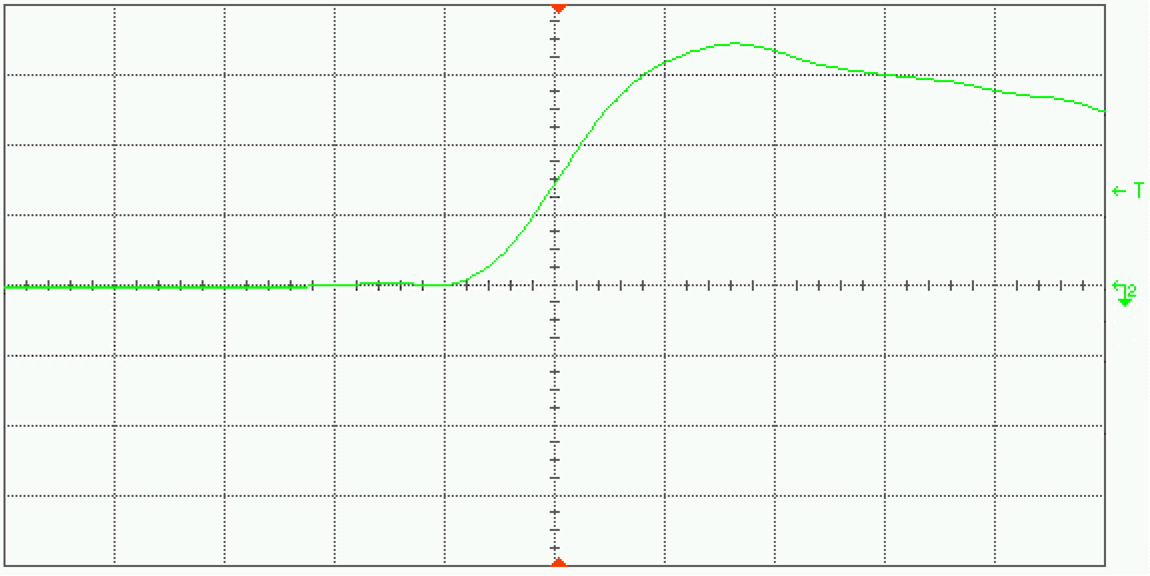


Fig 12(a) Pre-irradiation rising edge of DUT 14122

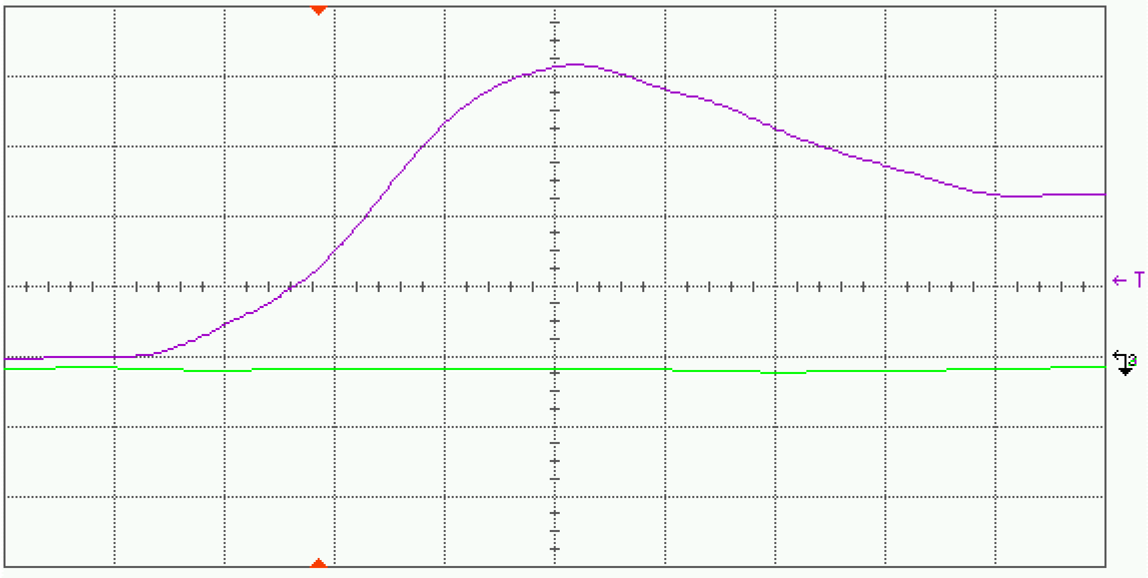


Fig 12(b) Post-annealing rising edge of DUT 14122

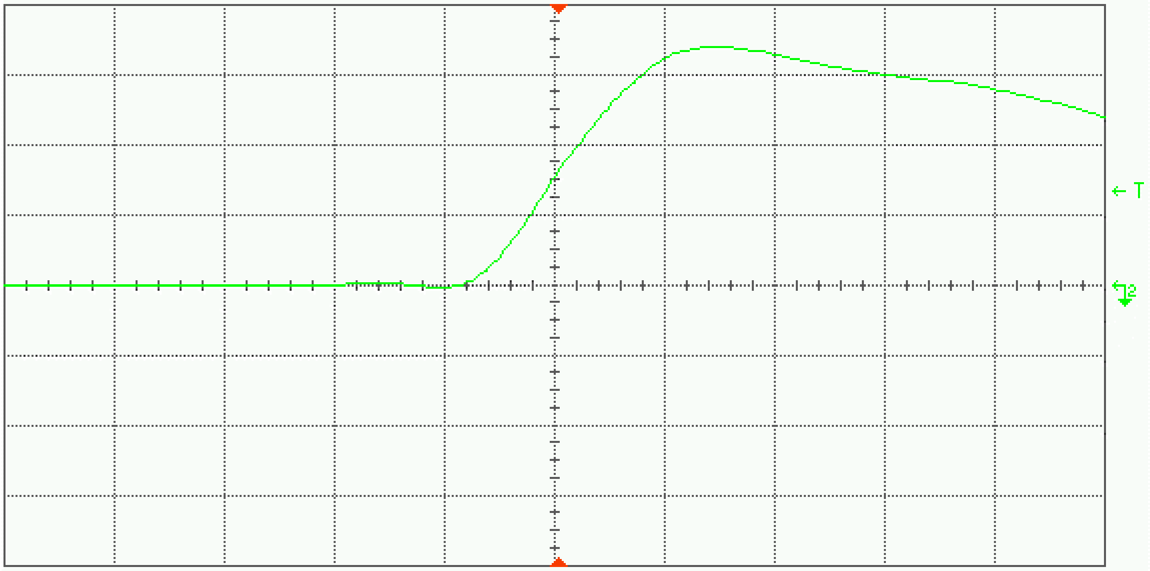


Fig 13(a) Pre-irradiation rising edge of DUT 14178

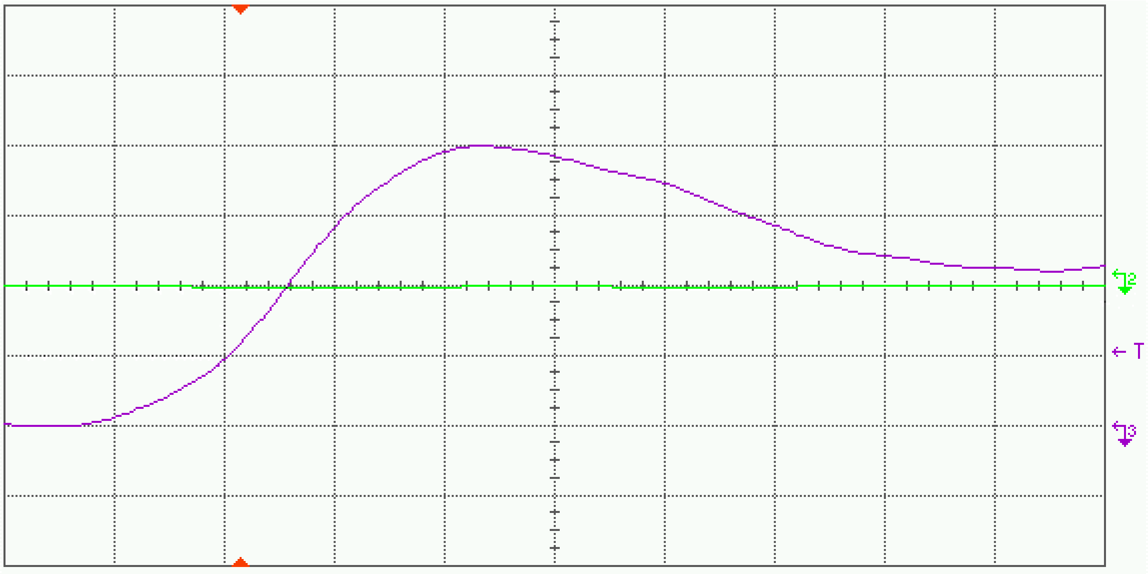


Fig 13(b) Post-annealing rising edge of DUT 14178

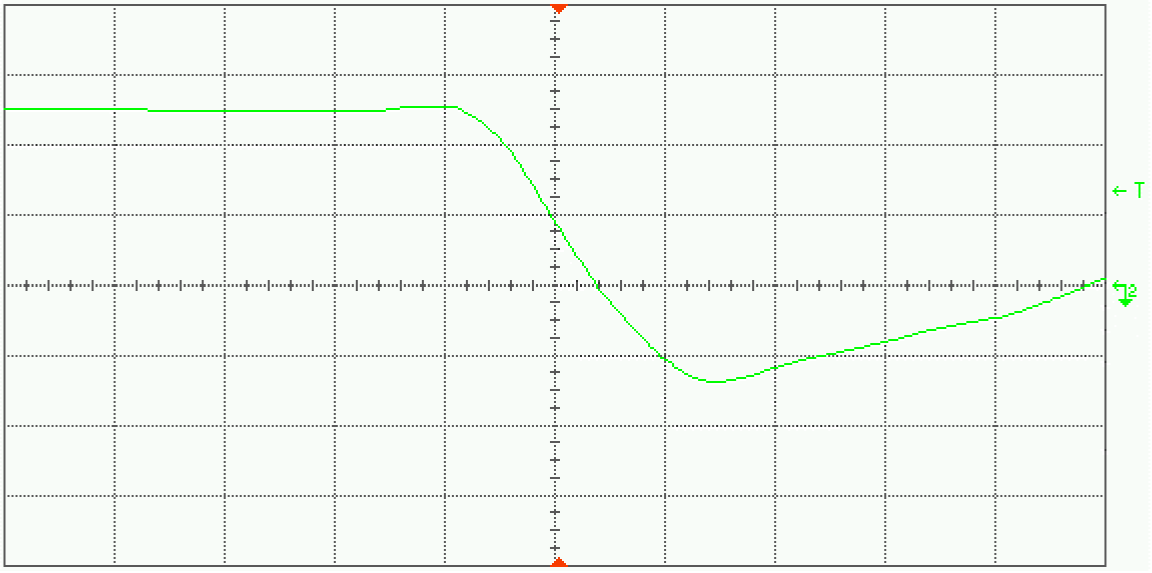


Fig 14(a) Pre-irradiation falling edge of DUT 14070

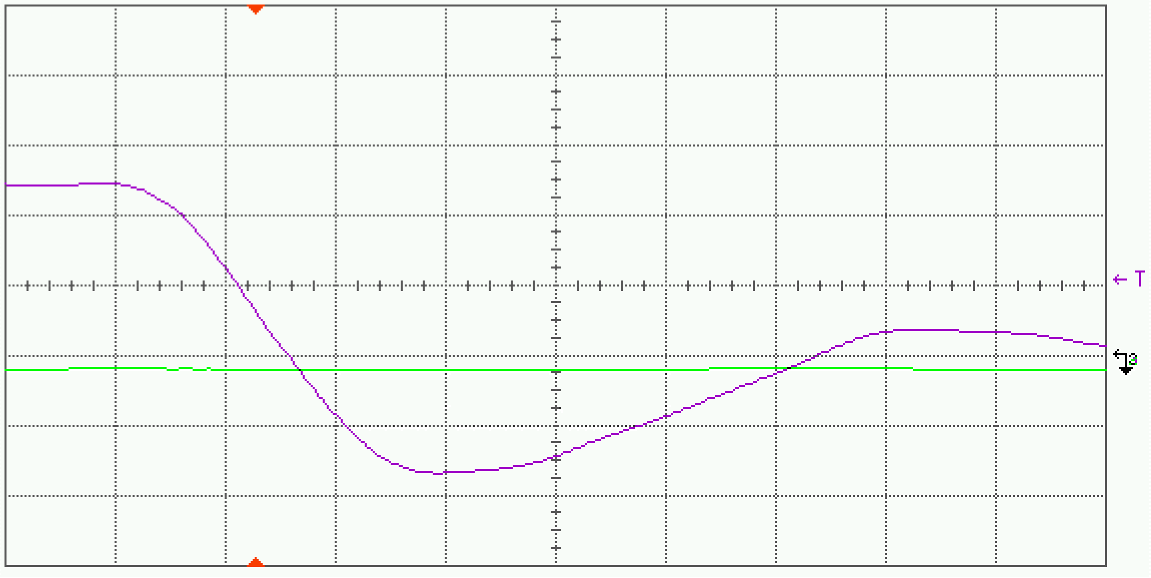


Fig 14(b) Post-annealing falling edge of DUT 14070

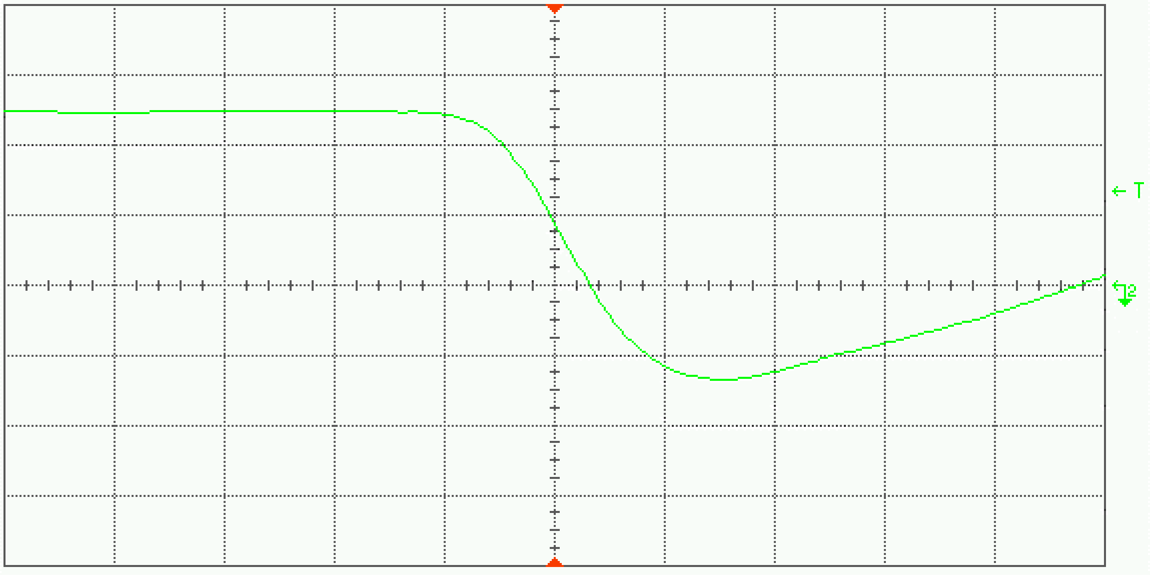


Fig 15(a) Pre-irradiation falling edge of DUT 14098

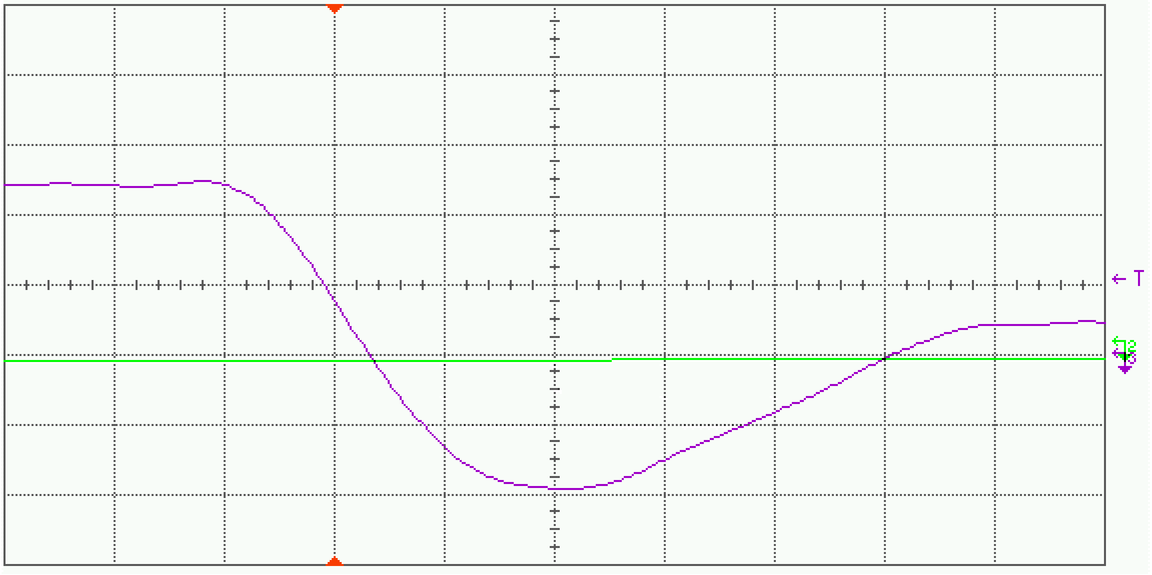


Fig 15(b) Post-annealing falling edge of DUT 14098

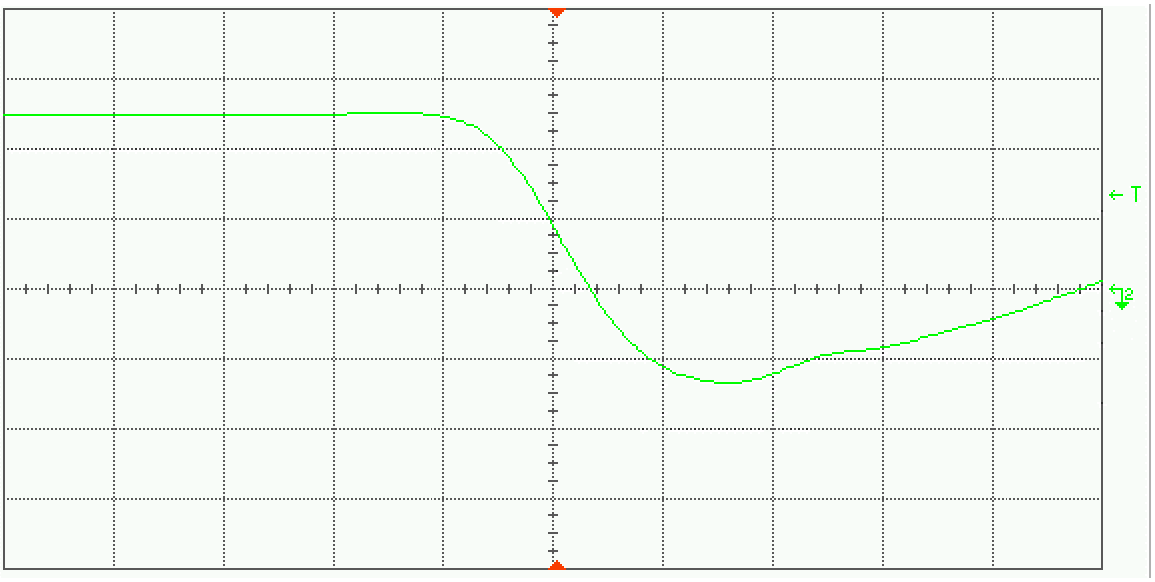


Fig 16(a) Pre-irradiation falling edge of DUT 14111

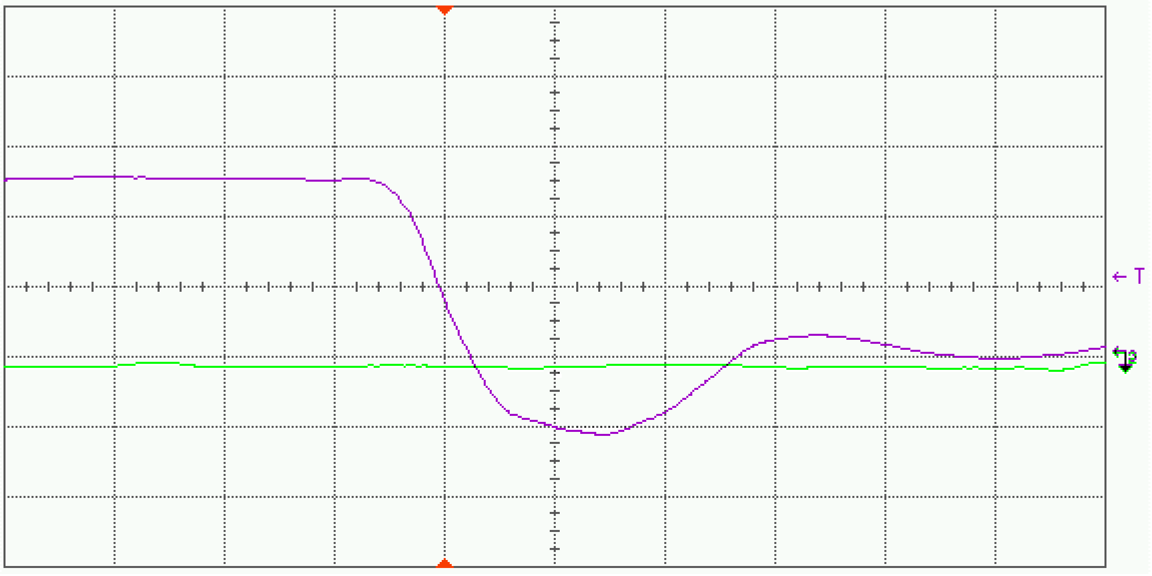


Fig 16(b) Post-annealing falling edge of DUT 14111, notice that the time scale is 2 ns/div.

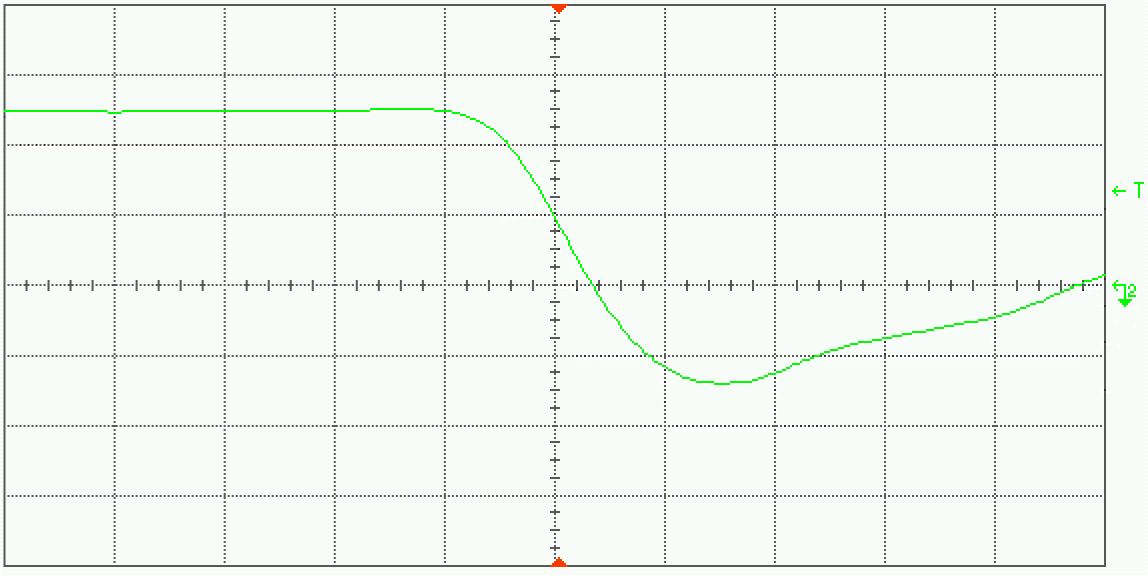


Fig 17(a) Pre-irradiation falling edge of DUT 14122

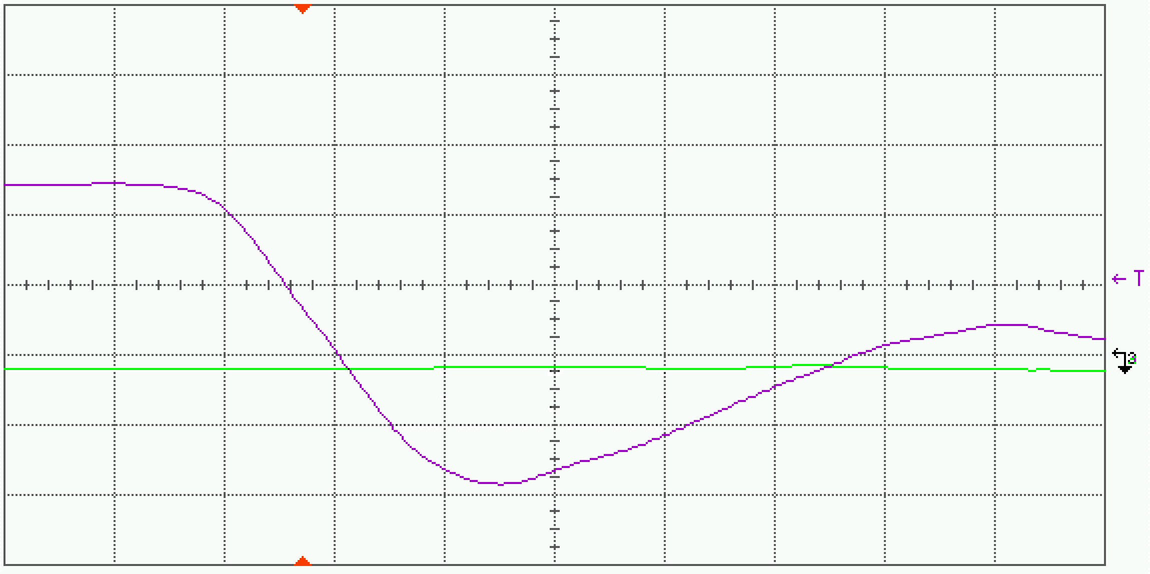


Fig 17(b) Post-annealing falling edge of DUT 14122

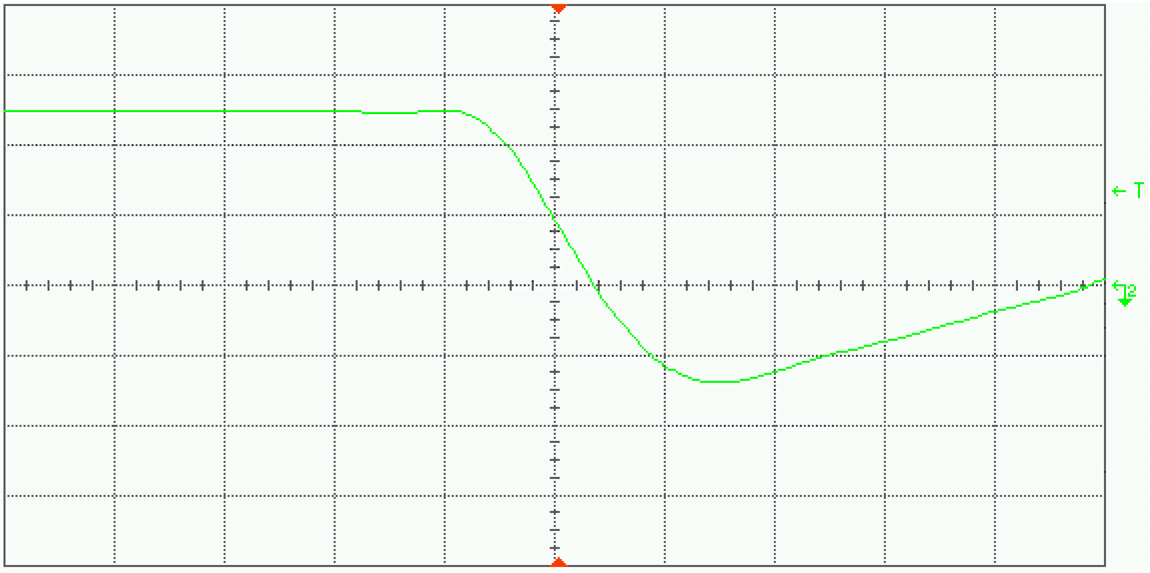


Fig 18(a) Pre-irradiation falling edge of DUT 14178

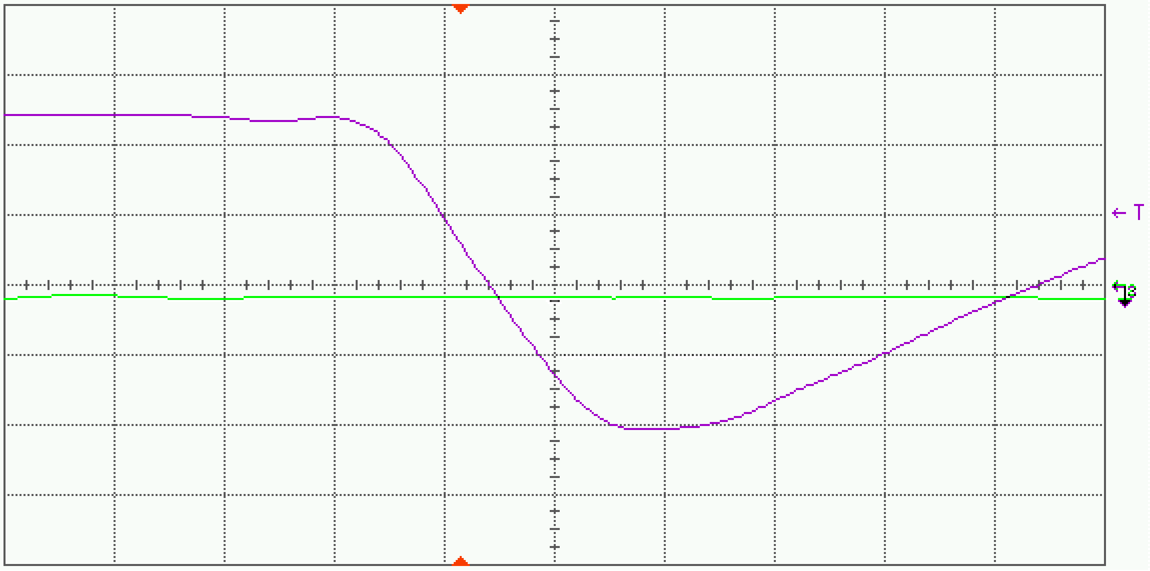
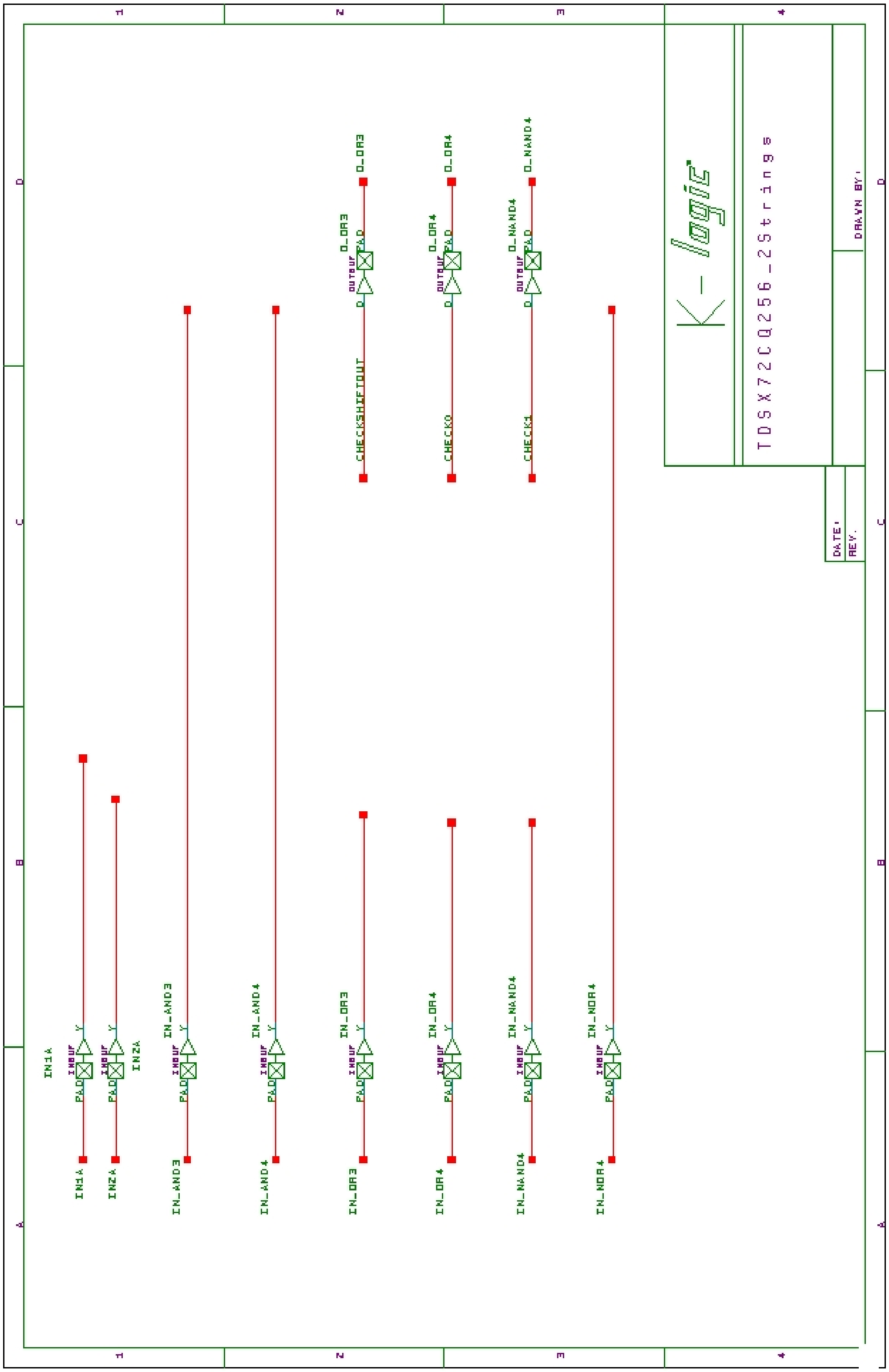


Fig 18(b) Post-annealing falling edge of DUT 14178

APPENDIX A DUT DESIGN SCHEMATICS



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IN_AND4
IN_OR3
IN_OR4
IN_NAND4
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INBUF
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Y
CHECKSHIFTOUT
CHECK0
CHECK1
OUTBUF
D
O_OR3
O_OR4
O_NAND4
K-logic
TDSX72CQ256_2Strings
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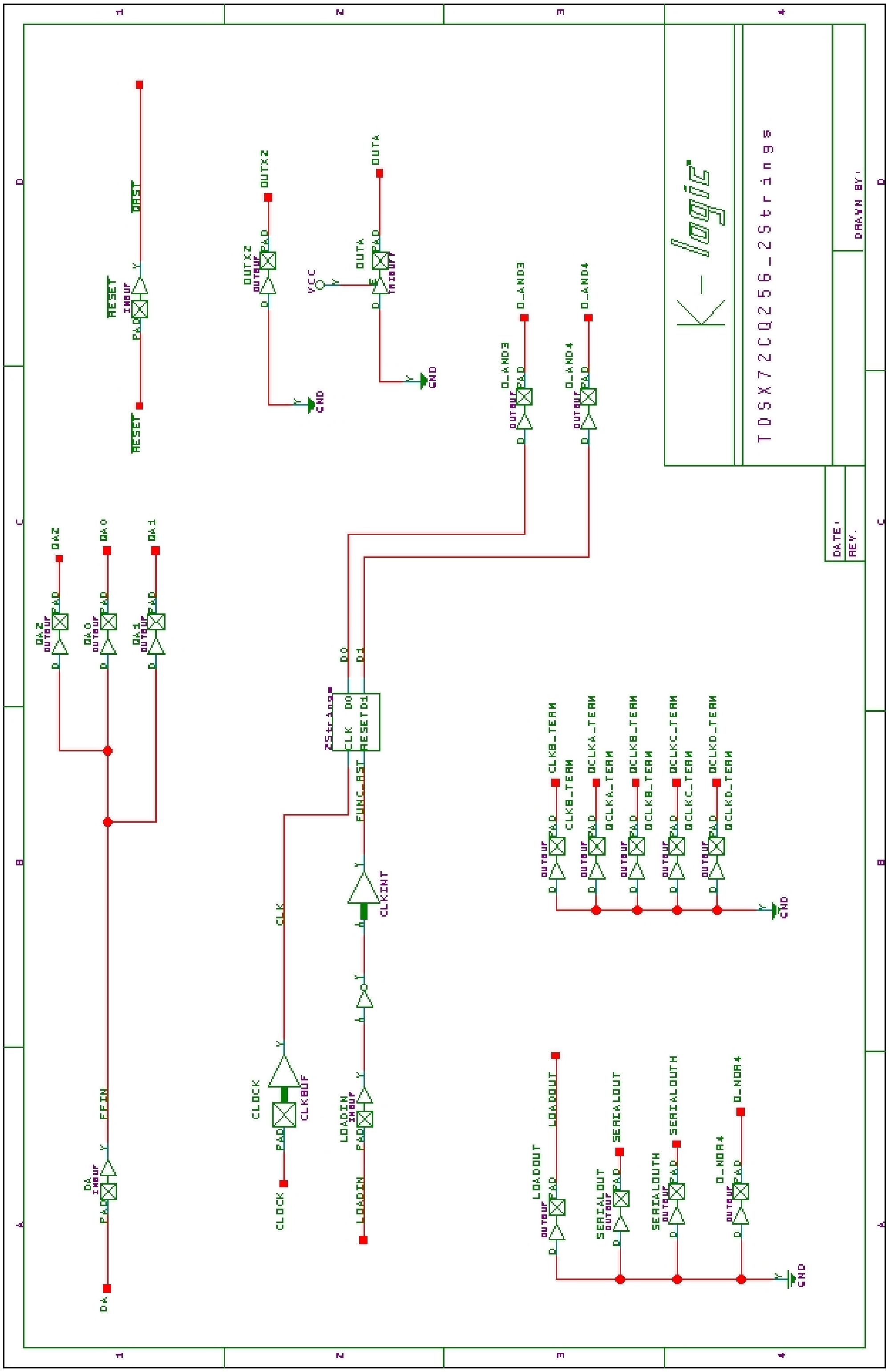
REV:
1
2
3
4
A
B
C
D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QA1
OUTBUF
D
RESET
QRST
CLOCK
CLKBUF
CLK
LOADIN
CLKINT
FUNC_RST
2Strings
CLK
D0
RESETD1
D1
OUTX2
OUTA
TRIBUF
E
VCC
GND
D_AND3
D_AND4
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
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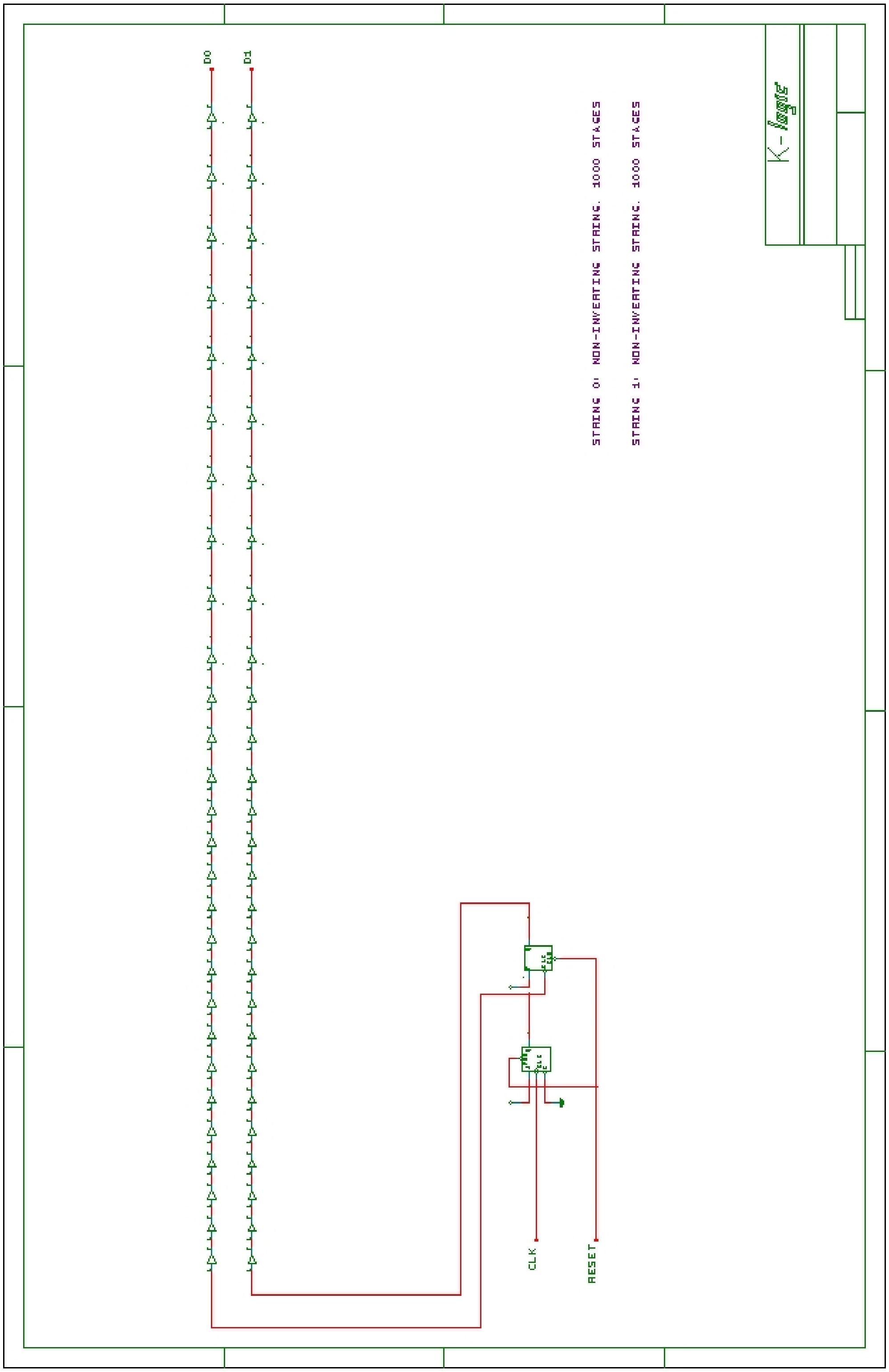
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STRING 1: NON-INVERTING STRING, 1000 STAGES
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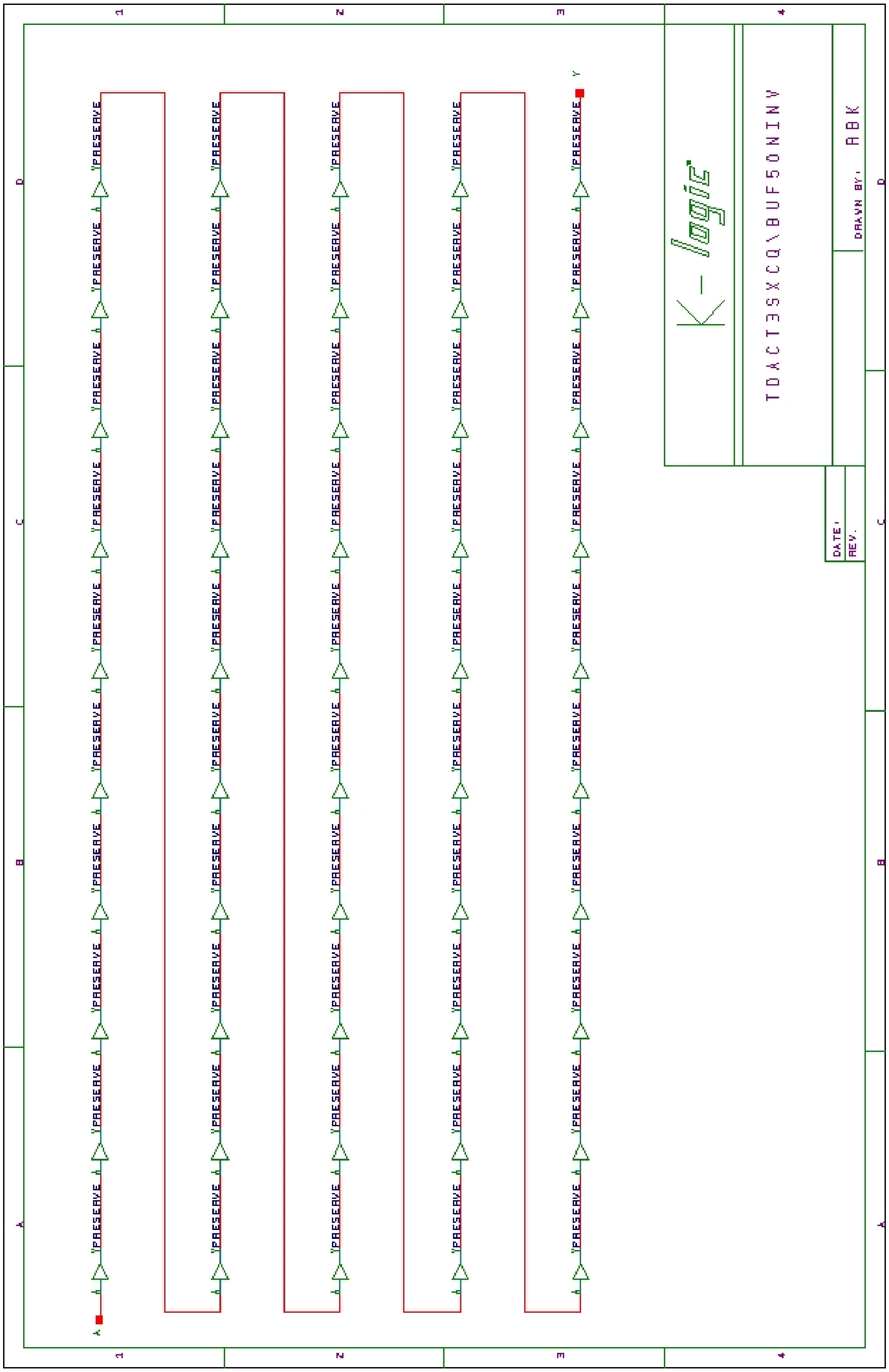
RESET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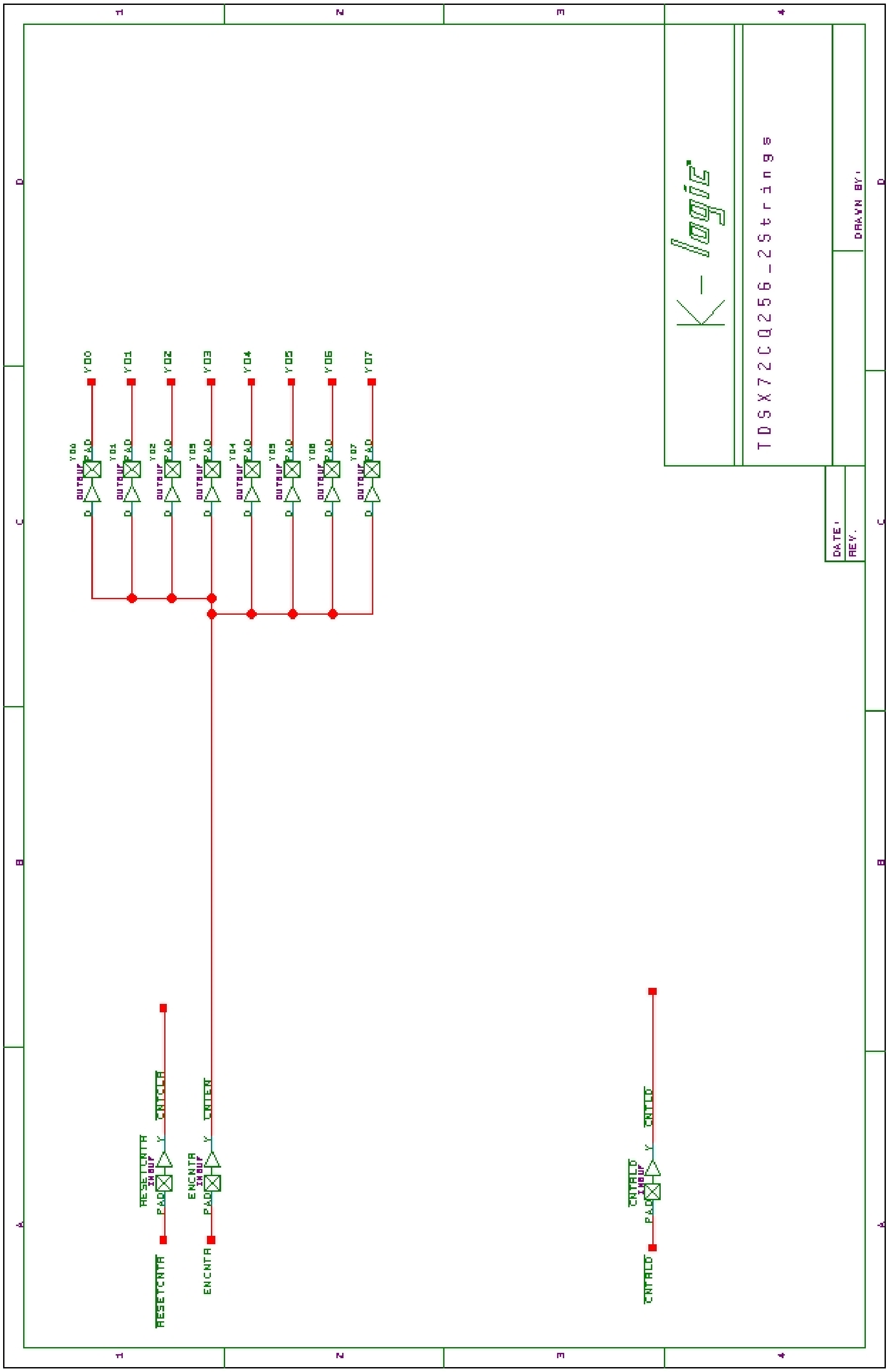
D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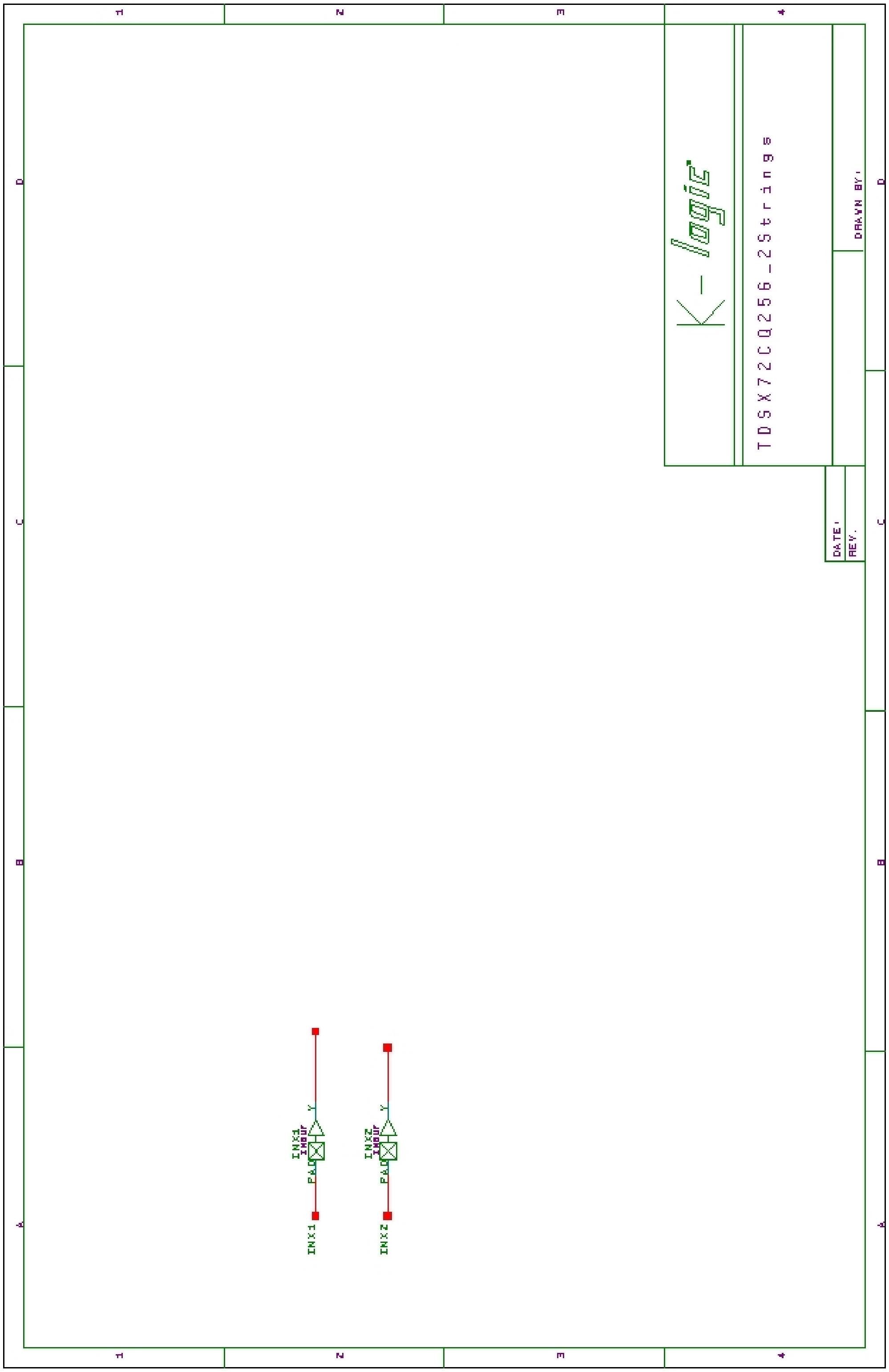
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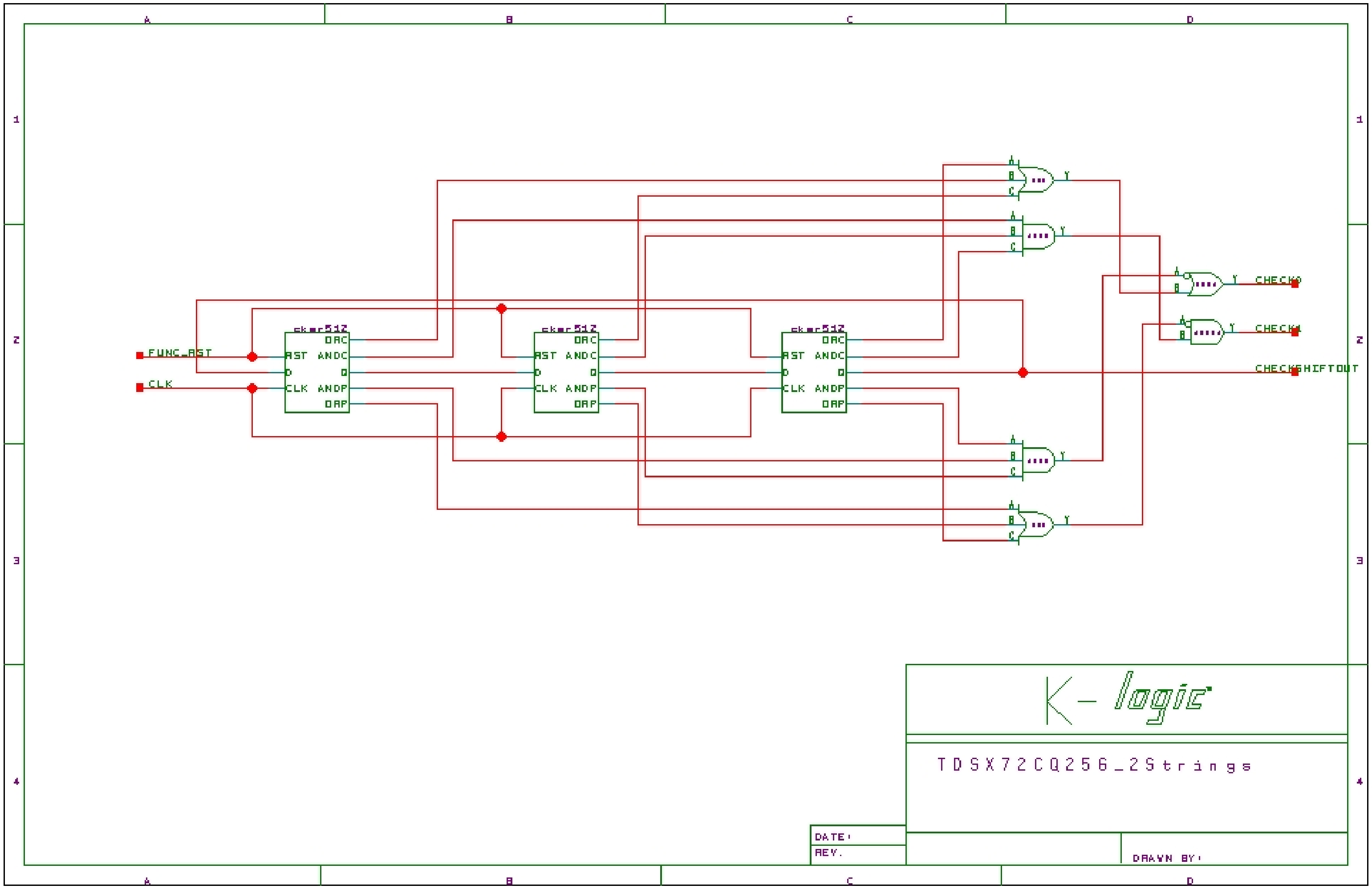
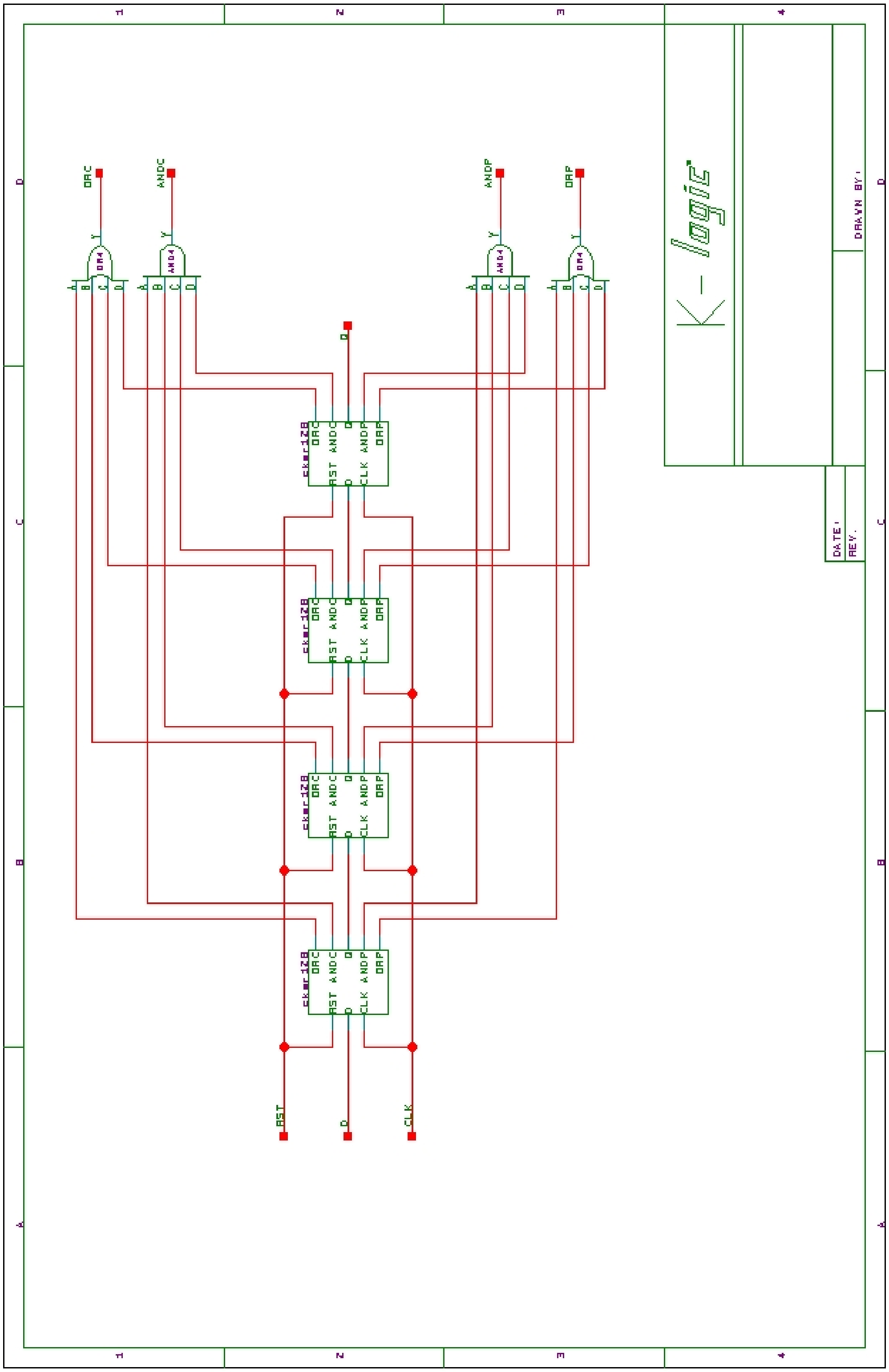
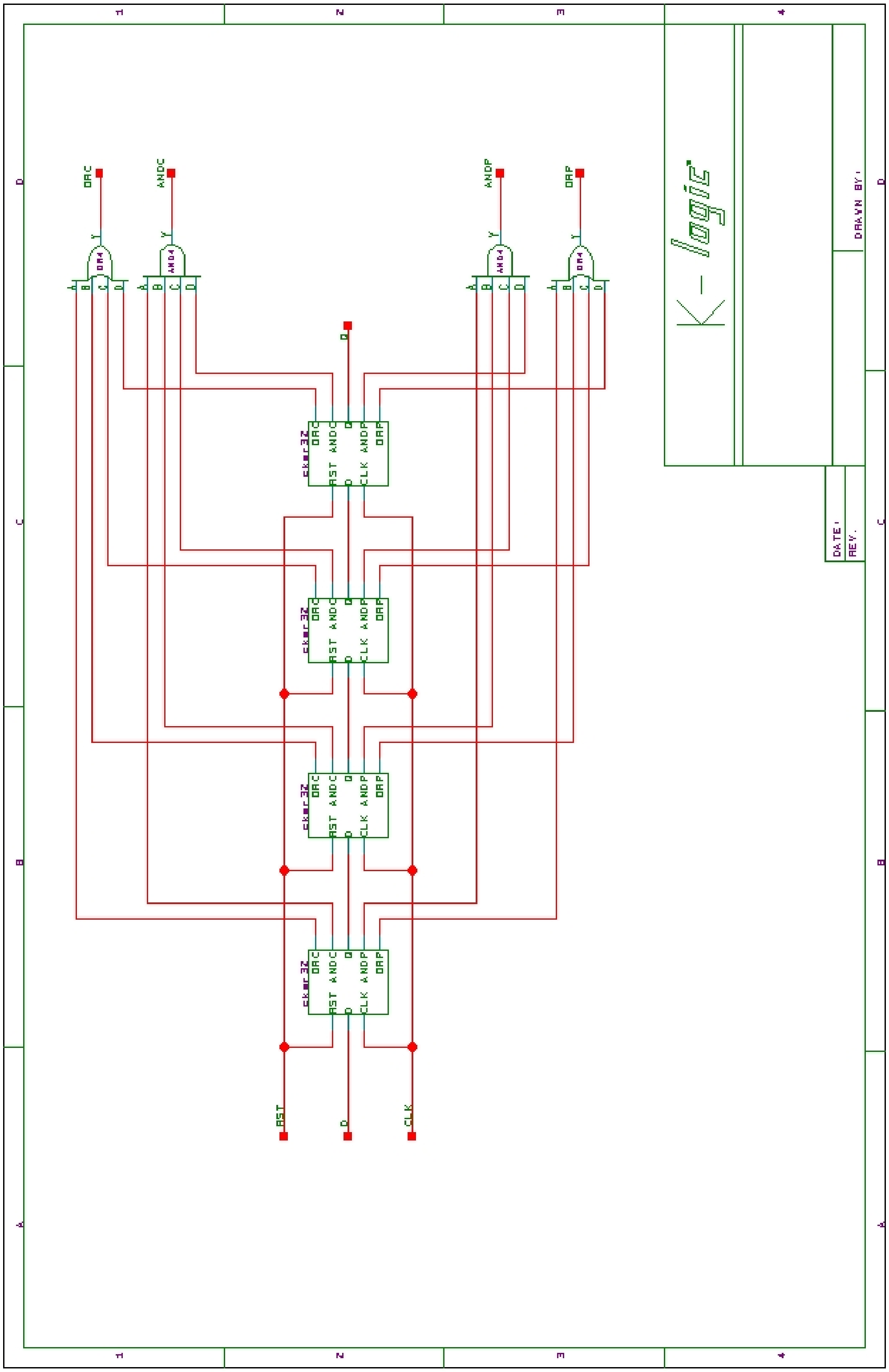
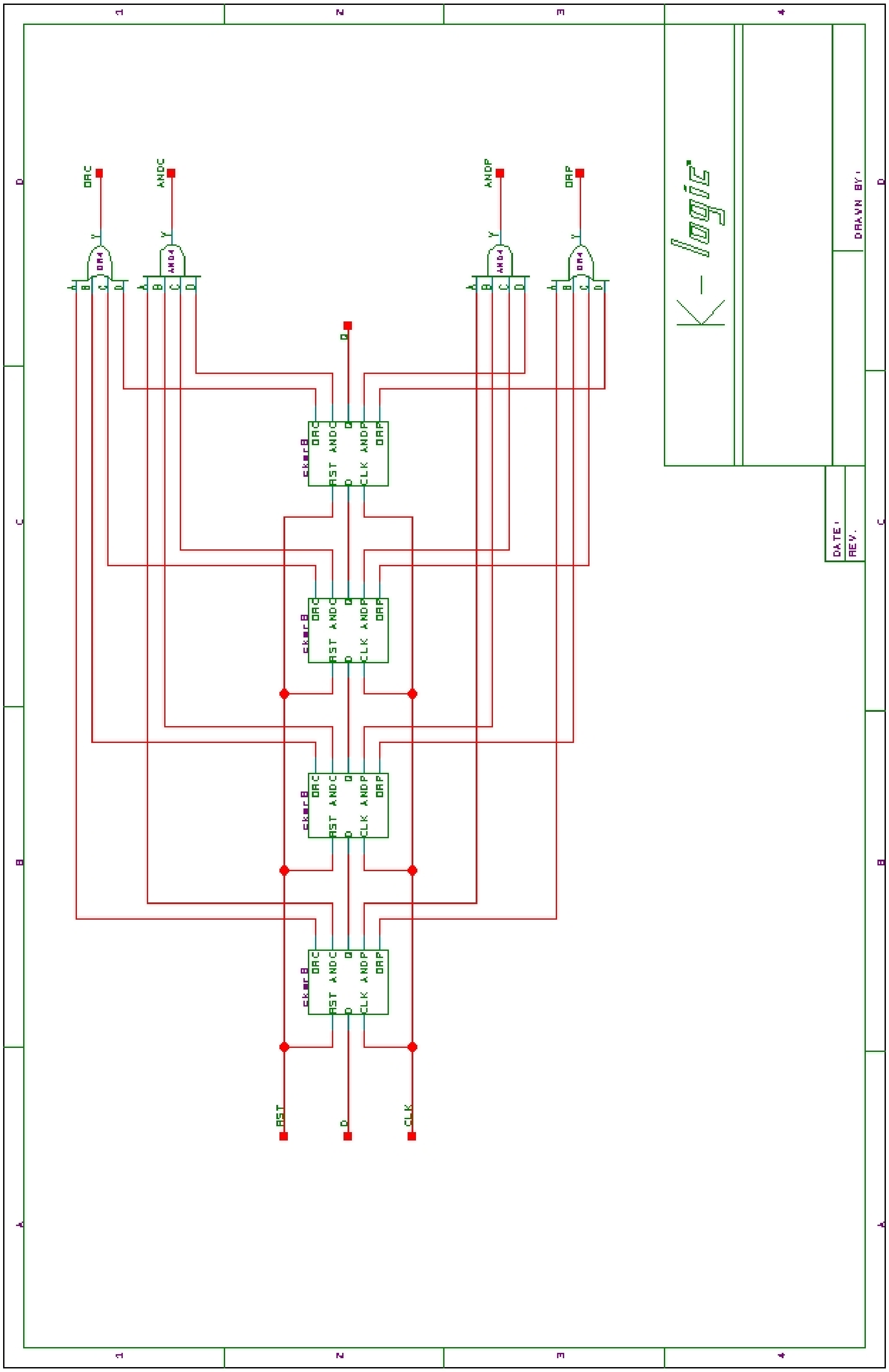
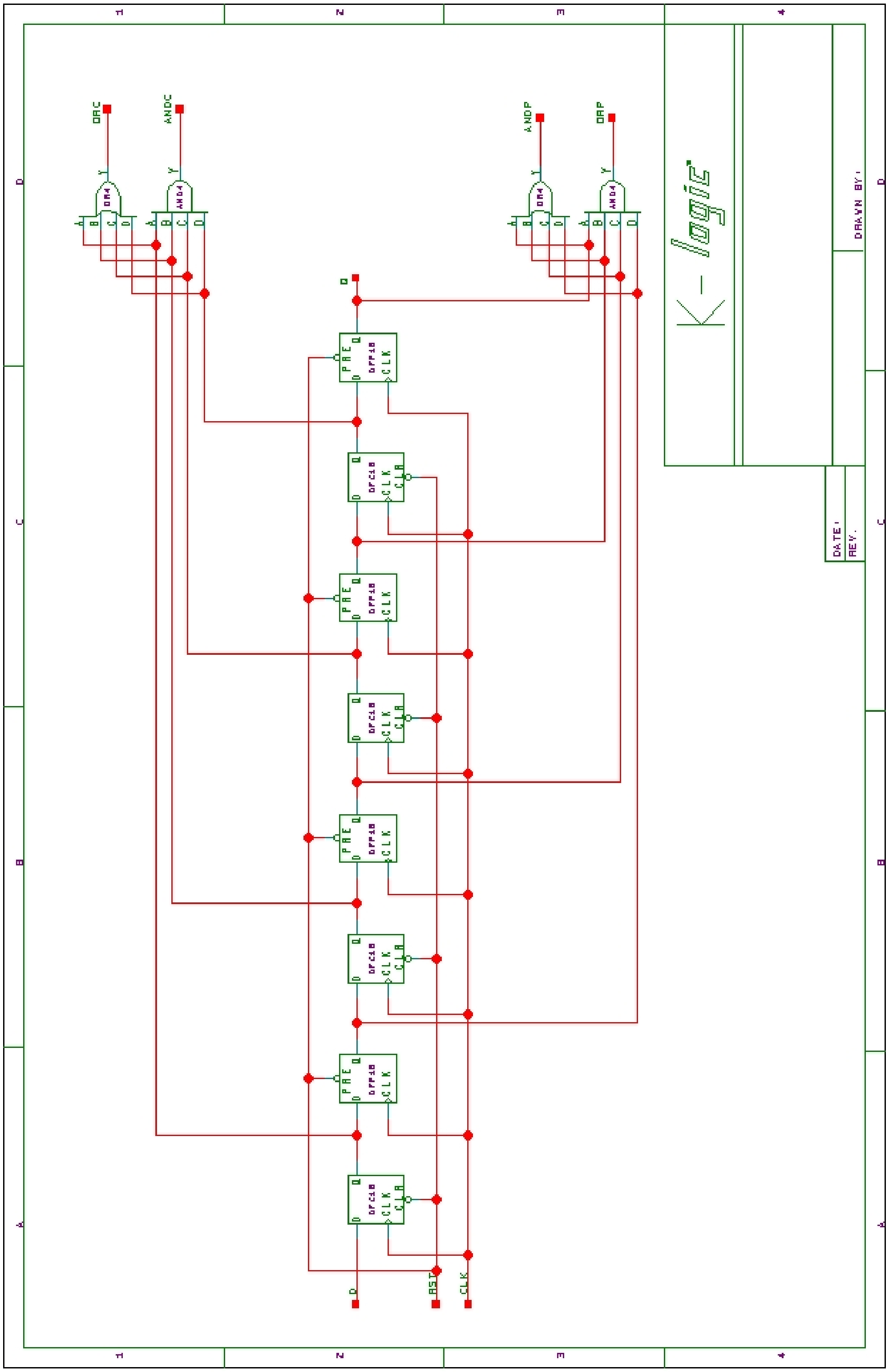
PAD
INX1
INX2
INBUF
Y
PAD
INX2
1
2
3
4
A
B
C
D


A
B
C
D
1
2
3
4
FUNC_RST
CLK
ckmr512
RST
D
CLK
ORC
ANDC
Q
ANDP
ORP
ckmr512
RST
D
CLK
ORC
ANDC
Q
ANDP
ORP
ckmr512
RST
D
CLK
ORC
ANDC
Q
ANDP
ORP
A
B
C
Y
A
B
C
Y
A
B
C
Y
A
B
C
Y
A
B
Y
CHECK0
A
B
Y
CHECK1
CHECKSHIFTOUT
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:

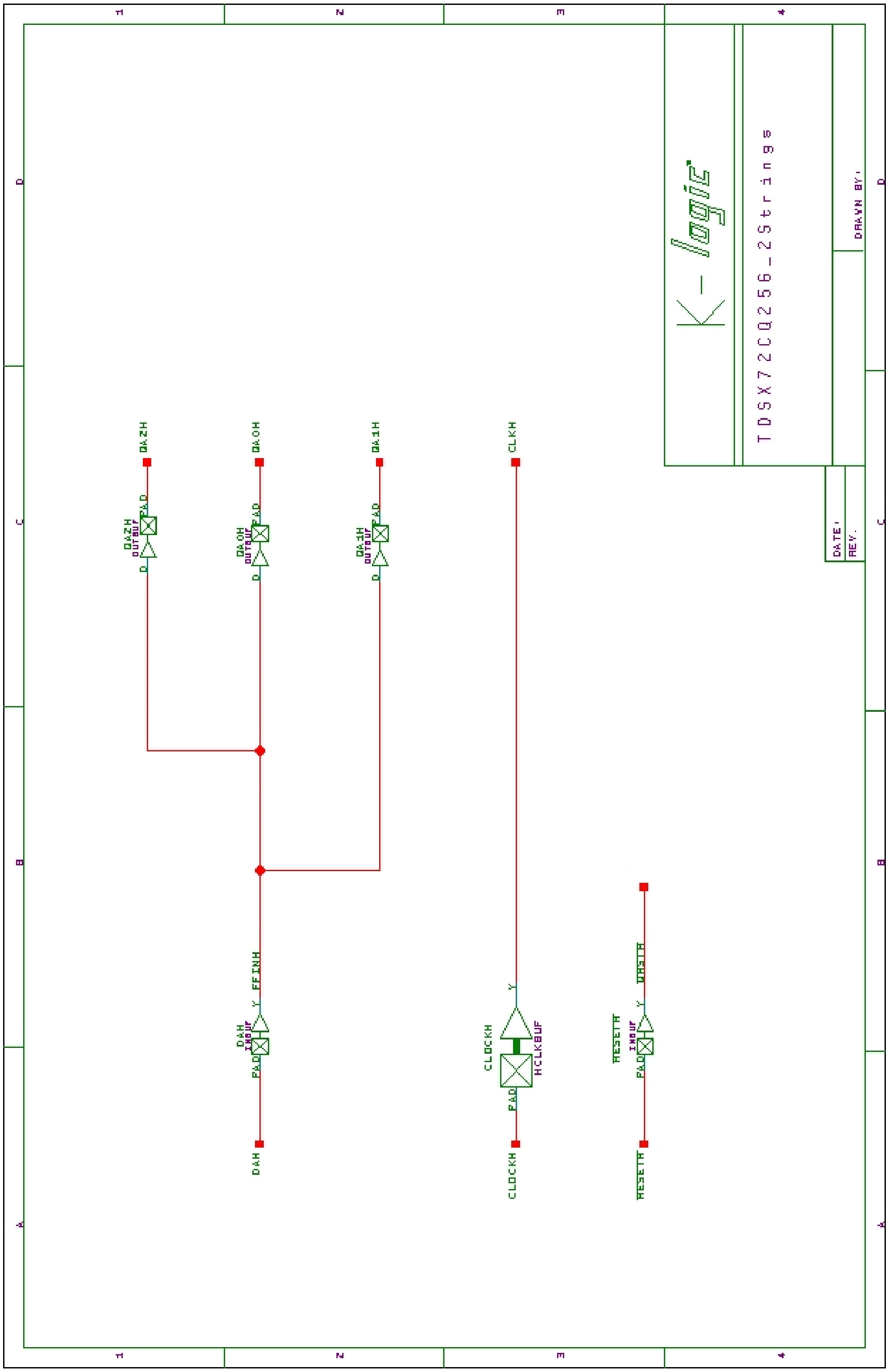

ORC
ANDC
ANDP
ORP
OR4
AND4
A
B
C
D
Y
Q
ckmr128
RST
ANDC
Q
ORC
D
CLK
ANDP
ORP
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

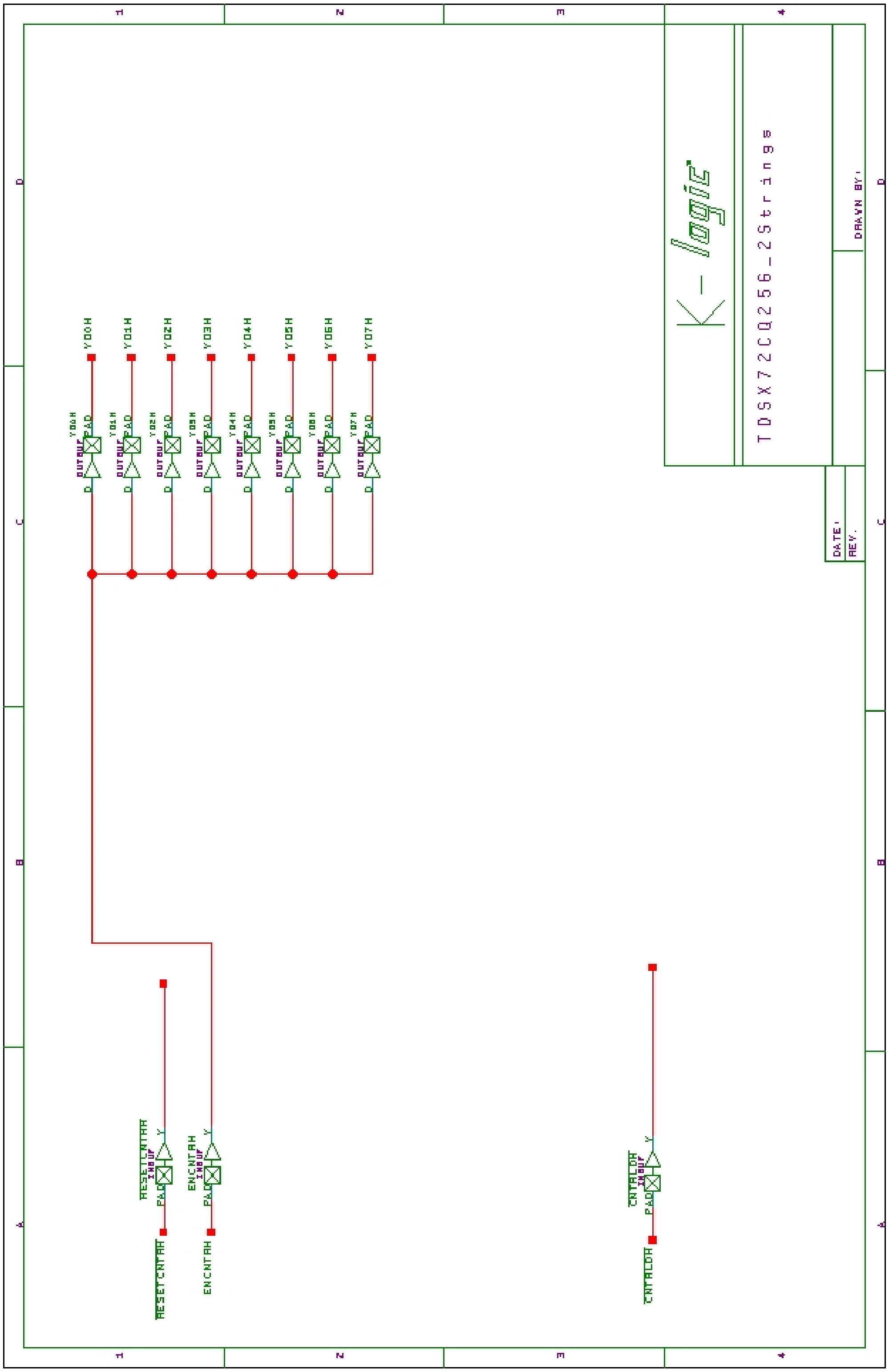

ORC
ANDC
ANDP
ORP
OR4
AND4
Y
A
B
C
D
ckmr32
RST
D
CLK
Q
ANDC
ANDP
ORC
ORP
RST
D
CLK
Q
K-logic
DRAWN BY:
DATE:
REV.
1
2
3
4
A
B
C
D


ORC
ANDC
ANDP
ORP
OR4
AND4
A
B
C
D
Y
Q
ckmr8
RST
D
CLK
Q
K-logic
DRAWN BY:
DATE:
REV.

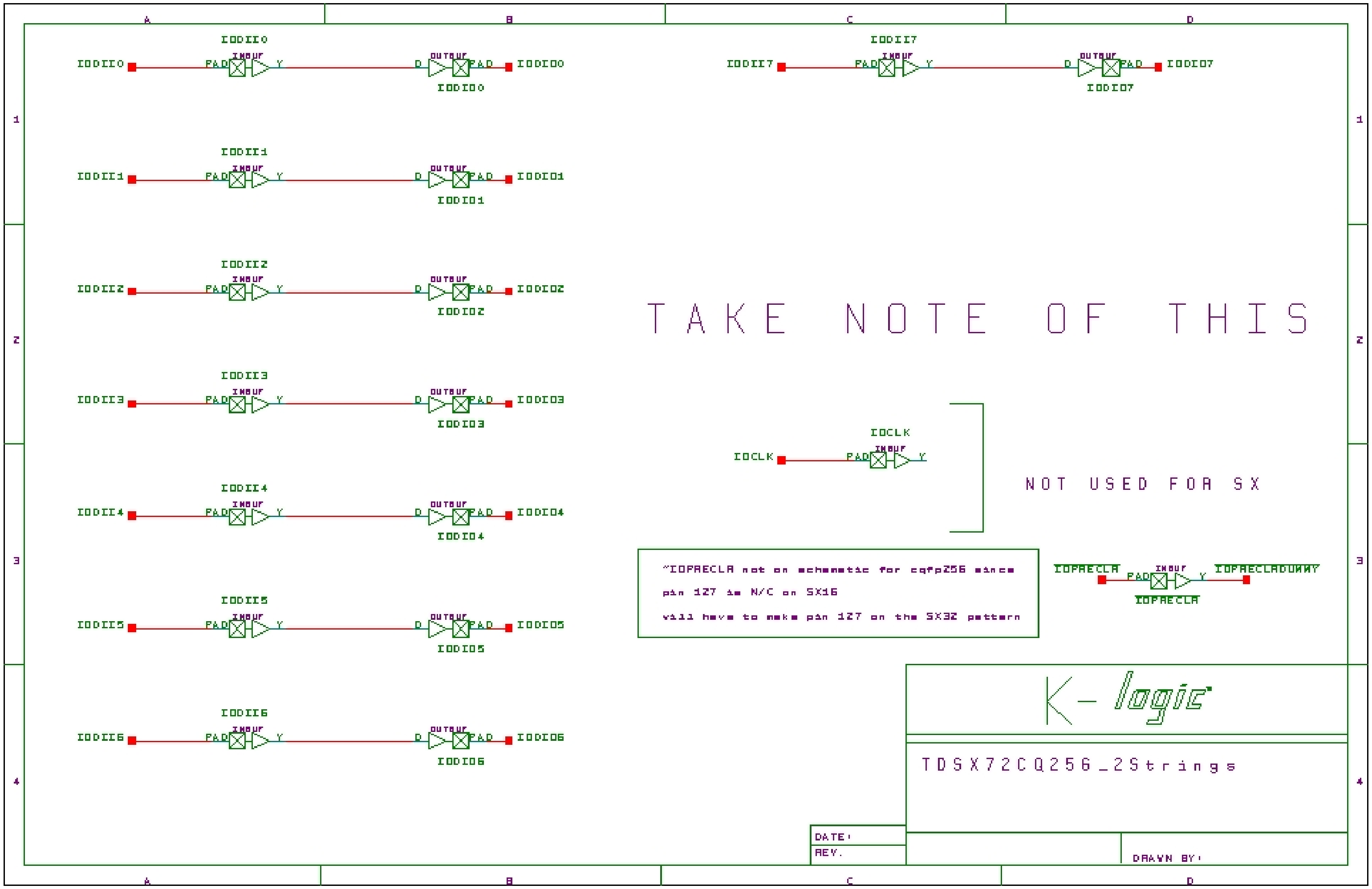


ORC
ANDC
ANDP
ORP
OR4
AND4
Y
A
B
C
D
DFF1B
DFC1B
PRE
CLR
CLK
Q
RST
K-logic
DRAWN BY:
DATE:
REV.


QA2H
OUTBUF
PAD
D
QA0H
QA1H
CLKH
DAH
INBUF
Y
FFINH
CLOCKH
HCLKBUF
RESETH
URSTH
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
1
2
3
4
A
B
C
D



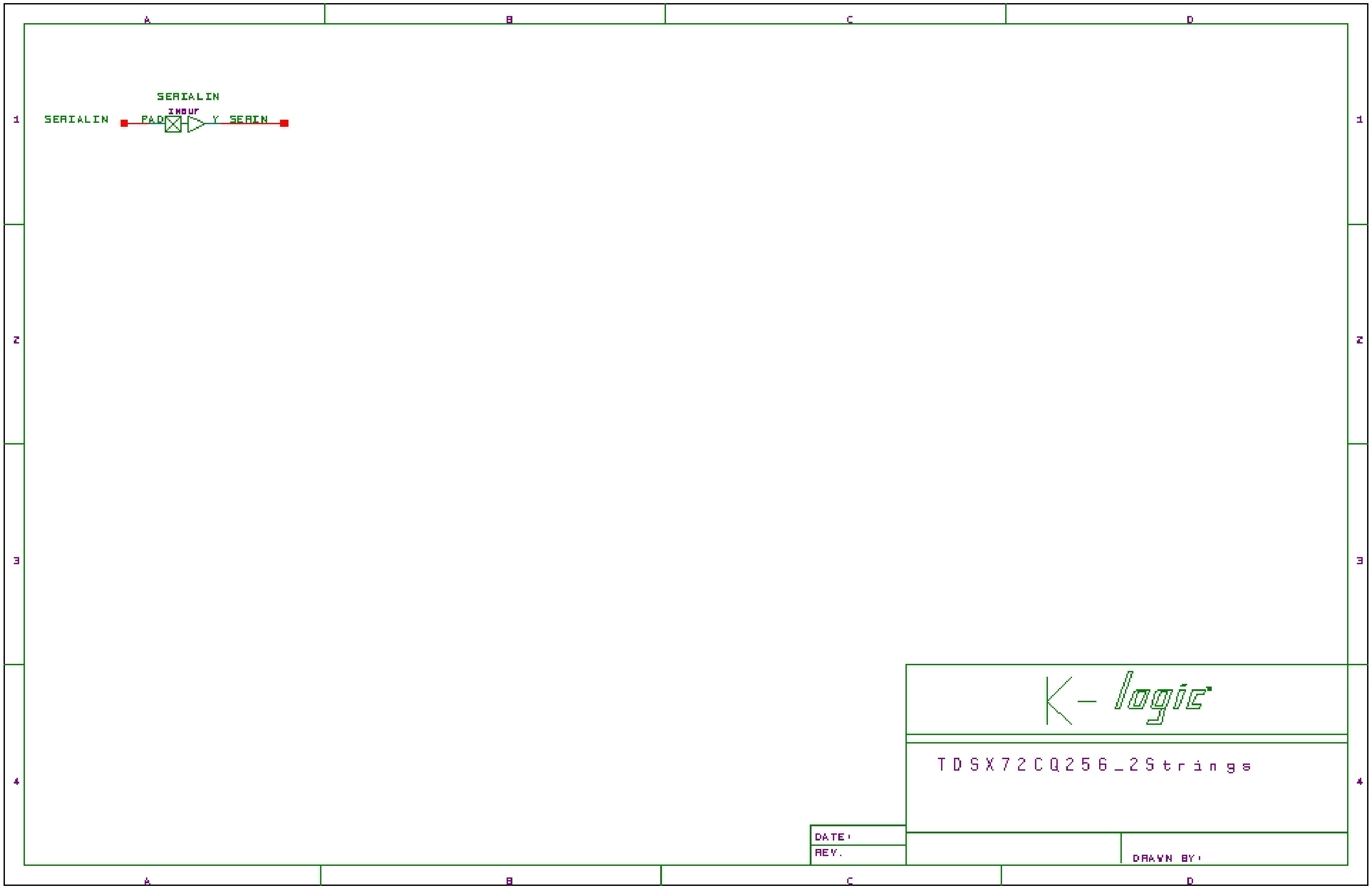
TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV:
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
D
PAD
RESETCNTAH
ENCNTAH
CNTALDH
INBUF
Y

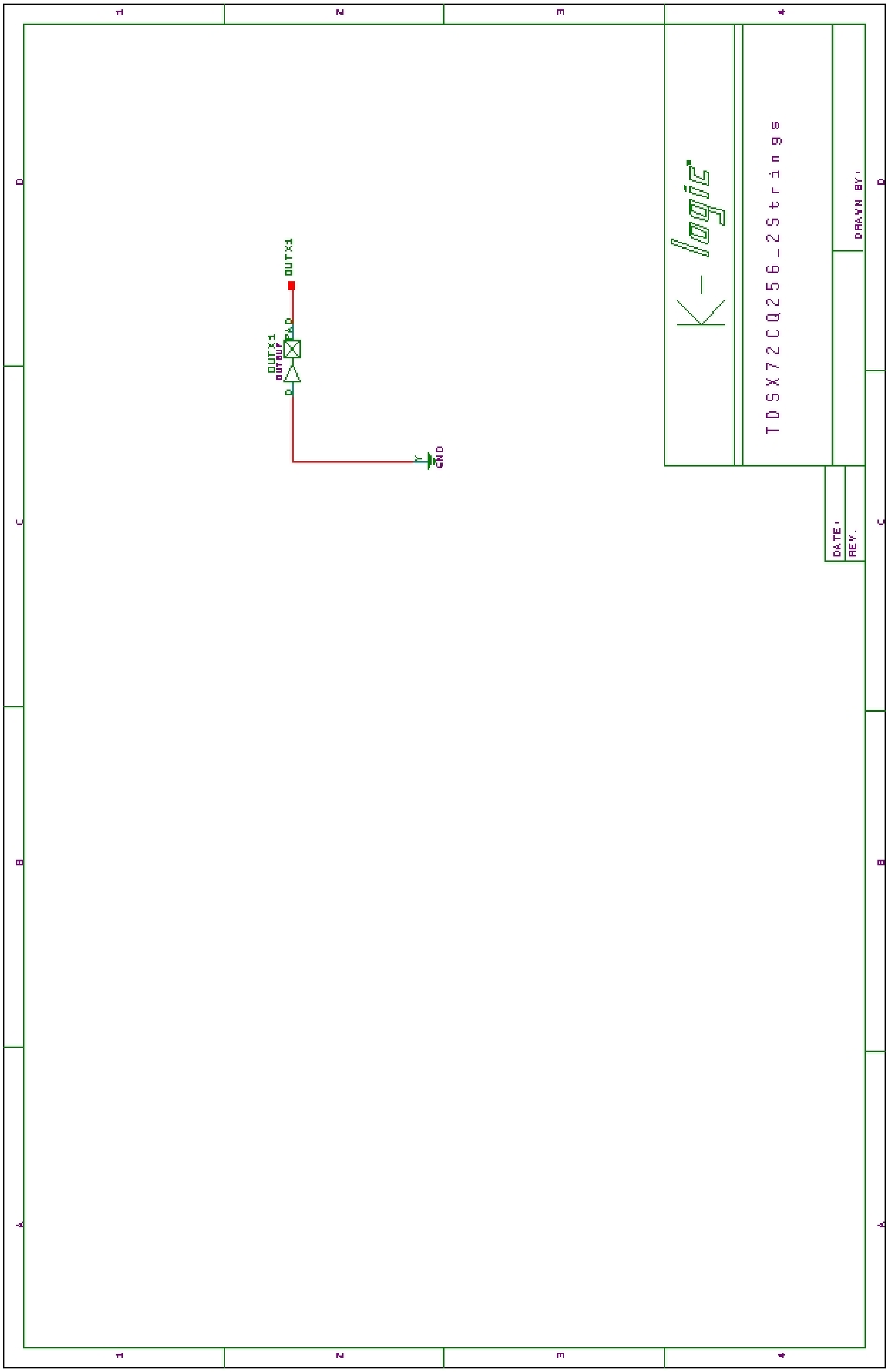

A
B
C
D
1
2
3
4
IODII0
INBUF
PAD
Y
IODII0
D
OUTBUF
PAD
IODIO0
IODIO0
IODII1
IODII1
IODIO1
IODIO1
IODII2
IODII2
IODIO2
IODIO2
IODII3
IODII3
IODIO3
IODIO3
IODII4
IODII4
IODIO4
IODIO4
IODII5
IODII5
IODIO5
IODIO5
IODII6
IODII6
IODIO6
IODIO6
IODII7
IODII7
IODIO7
IODIO7
IOCLK
IOCLK
IOPRECLA
IOPRECLA
IOPRECLADUMMY
K-logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:

TAKE NOTE OF THIS

NOT USED FOR SX

*IOPRECLA not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


A
B
C
D
1
2
3
4
SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


OUTX1
PAD
OUTX1
OUTBUF
D
Y
GND
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
1
2
3
4
A
B
C
D