TOTAL IONIZING DOSE TEST REPORT

No. 01T-RT54SX32-T6JP04
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I. SUMMARY TABLE

Parameters	Tolerance
1. Gross Functional	130krad(Si) static case
2. $I_{DDSTDBY}$	Passed 90krad(Si)
3. V_{IL}/V_{IH}	Passed 90krad(Si)
4. V_{OL}/V_{OH}	Passed 90krad(Si)
5. Propagation Delays	Passed 90krad(Si)
6. Rising/Falling Edge Transient	Passed 90krad(Si)
7. Power-up Transient Current	Passed 90krad(Si)

Note: This test was performed in NASA/Goddard radiation facility following their radiation guidelines.

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. Device Under Test (DUT)

Table 1 lists the DUT information.

Table 1. DUT Information

Part Number	RT54SX32
Package	CQFP208
Foundry	MEC
Technology	0.6µm CMOS
Die Lot Number	T6JP04
Quantity Tested	6
Serial Numbers	LAN4901, LAN4902, LAN4903, LAN4904, LAN4905, LAN4906

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2. Irradiation Parameters

Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	1krad(Si)/hr (+/-10%)
Data Mode	Static
Temperature	Room
Bias	3.3V/5.0V

C. Test Method

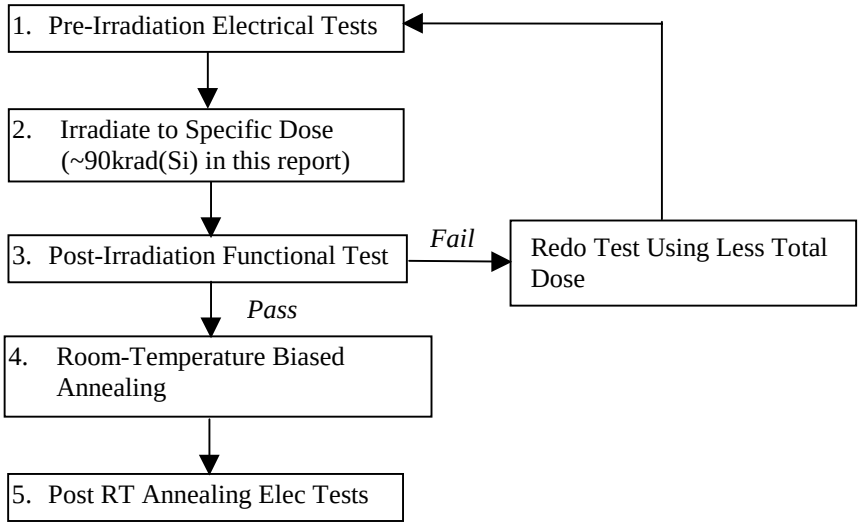

Figure 1. Parametric test flow chart.

In Actel TID testing, two methods are used. Method one performs irradiation and gross functional test. The DUT is irradiated to gross functional failure. The tolerance is determined as the total accumulative dose at which gross functional failure occurs.

Method two performs irradiation and parametric test. Gross functional test is included in the process of this method. The method is in compliance with TM1019.5. If necessary, biased room-temperature-annealing is used to simulate the low-dose-rate space environment. Figure 1 shows the process flow. Rebound annealing at 100°C is omitted because the previous results show that antifuse FPGA fabricated in MEC foundry have no rebound effects.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, this bench setup has much less noise but only sample few pins (due to logistics, not inability). However, since the $I_{DDSTDBY}$ usually determines the tolerance, sampling few pins is sufficient. Moreover, the bench setup enables the in-situ monitoring of $I_{DDSTDBY}$ and functionality (of selected pins) during irradiation. Also, an important but non-standard parameter, power-up transient current, can only be measured accurately on the bench. Table 3 lists the corresponding logic design for each test parameter.

Table 3. Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions
2. $I_{DDSTDBY}$	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	D flip-flop output
7. Power-up Transient Current	DUT power supply

III. Test Results

A. Method One: Irradiate to Gross Functional Failure

Figure 2 shows the radiation induced I_{CC} versus total dose for DUT LAN4901 and LAN4902. During irradiation, the DUT is statically biased. Failure was detected by clocking out the data and comparing them with the truth table. The earliest failure occurred at ~130krad(Si) (LAN4901). The sudden surge of I_{CC} at functional failure only occurs in static case. If the DUT ran dynamically during irradiation, this I_{CC} curve would be smooth over functional failure.

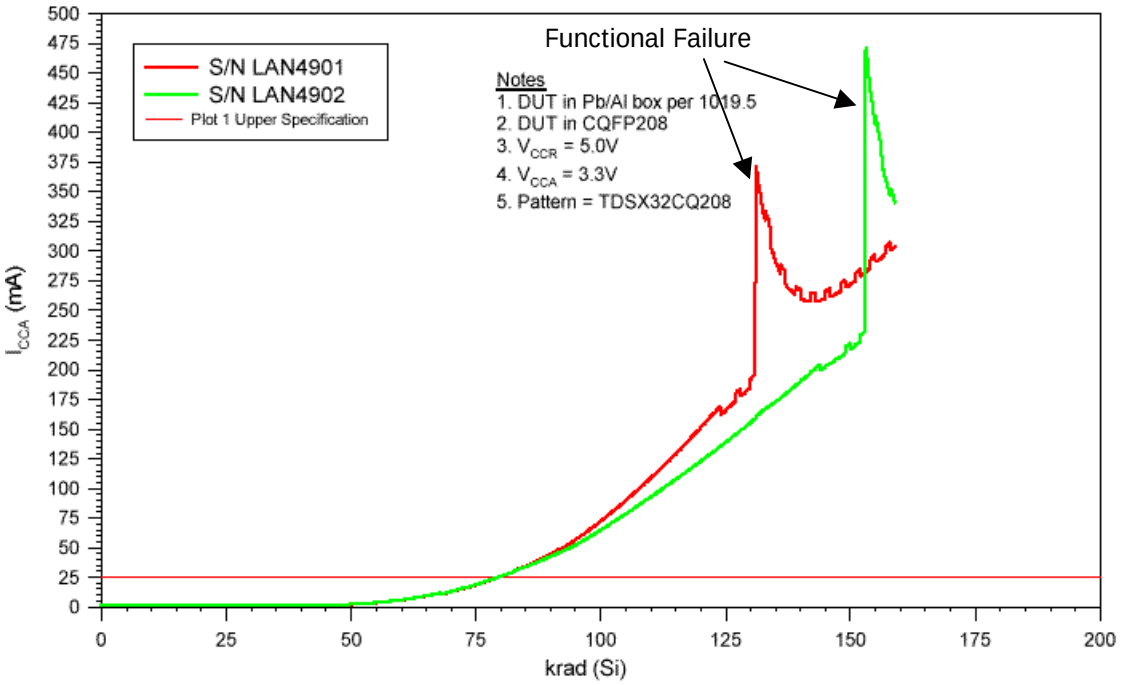

Figure 2. Radiation-induced I_{CC} (Delta I_{CC}) versus total dose for two DUT (LAN4901 and LAN4902).

B. Method Two: Irradiation and Parametric Test

This section presents the parametric test results to show the impact of total dose effects. The room temperature annealing was performed to reduce the static leakage current and power-up transient current. The DUT used for this test are LAN4903, LAN4904, LAN4905 and LAN4906.

1) Functional Test

Table 4 lists the results of the post-irradiation functional test (step 3).

Table 4. Functional Test Results

	Pre-Irradiation	Post-Irradiation
LAN4903	passed	passed
LAN4904	passed	passed
LAN4905	passed	passed
LAN4906	passed	passed

2) $I_{DDSTANDBY}$ (Static I_{CC} or I_{DD})

$I_{DDstandby}$ was monitored during the irradiation. The delta $I_{DDstandby}$ is the increment $I_{DDstandby}$ due to irradiation effect. Compared to the spec of 25mA, the small (< 1mA) pre-irradiation $I_{DDstandby}$ is negligible. The delta $I_{DDstandby}$ spec is approximately 25mA and used to determine tolerance.

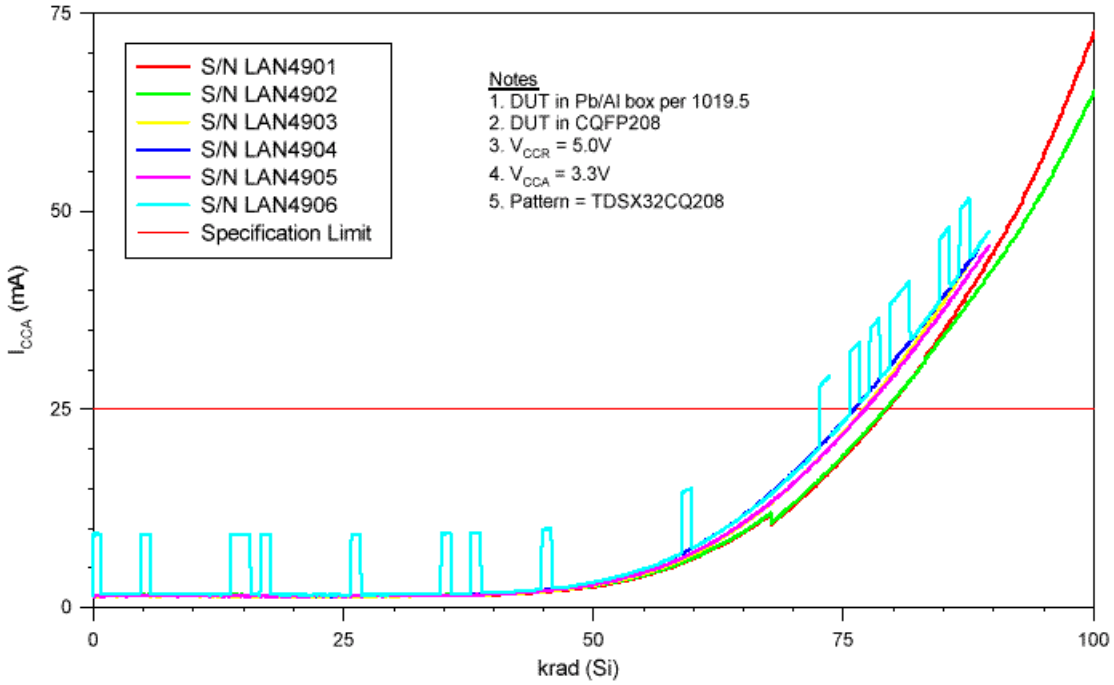

Figure 3. Radiation-induced Delta $I_{DDstandby}$ (I_{CC}) versus total dose for four DUT (LAN4903, LAN4904, LAN4905 and LAN4906).

Figure 3 shows the in-situ $I_{DDSTDBY}$ of LAN4903, LAN4904, LAN4905 and LAN4906 during irradiation. The data have a tight distribution. The device-to-device variation is small. The on-and-off glitches on the data-curve of LAN4906 are believed to be testing noises, which may be caused by grounding issues. The radiation effects applied to this particular DUT should be valid and the same as all the other DUT. The in-situ functional monitoring indicated no signs of trouble for any DUT through the irradiation process.

Figure 4a and b show the annealing curve of $I_{DDSTDBY}$. DUT were biased VCCA=3.3V, VCCI=5.0V at room temperature. These curves show that room temperature annealing can effectively reduce $I_{DDSTDBY}$ to within the spec limit in relatively short time. Only LAN4906 was not annealed to the spec. However, from the trend, it only takes months to reach the spec. Compared to tens of years of radiation to reach this total dose level in space, these data indicate that there are significant safety margins.

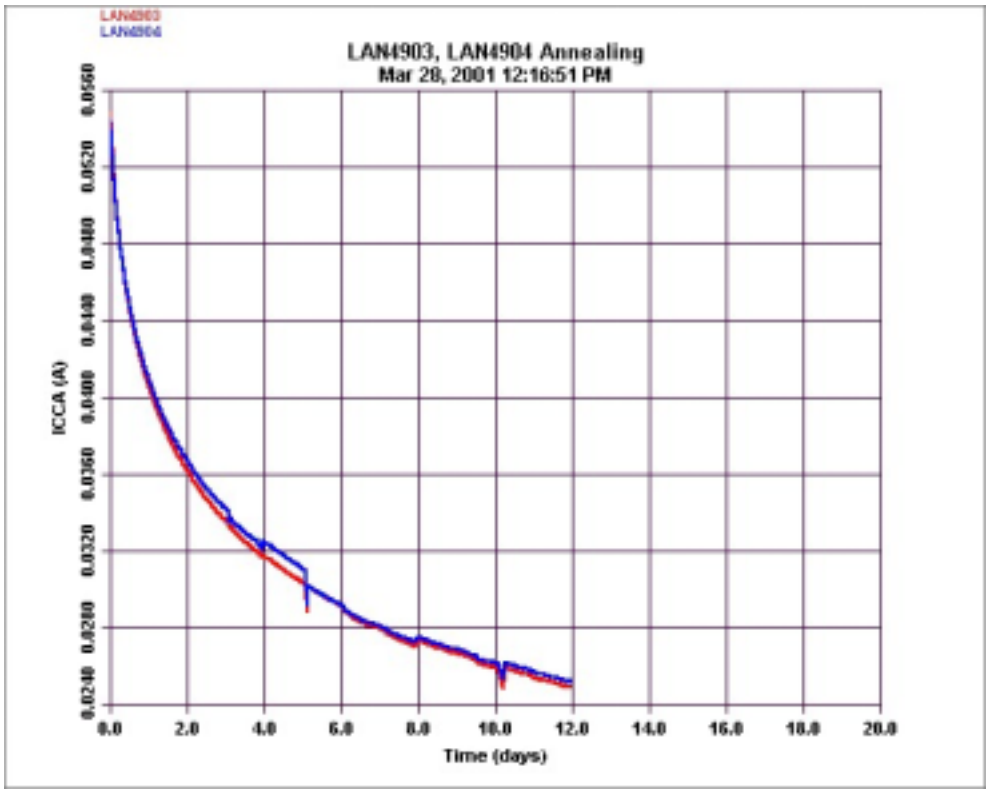

Figure 4 a. Post-irradiation annealing curve of $I_{DDSTDBY}$ for LAN4903 and LAN4904.

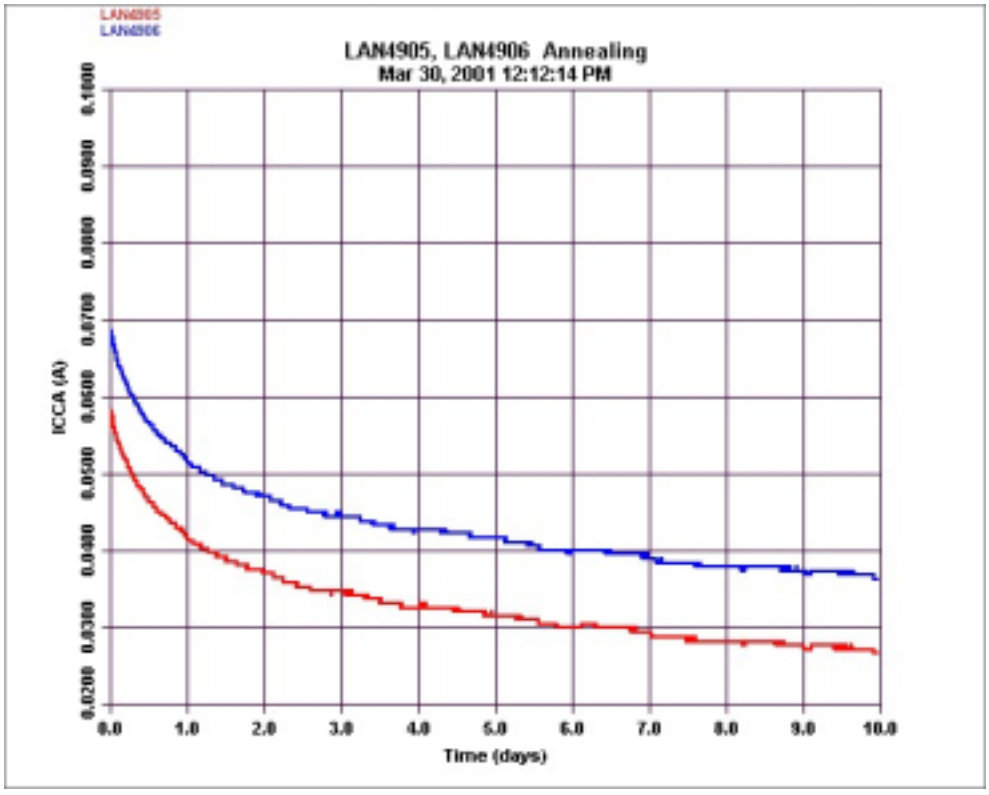

Figure 4b. Post-irradiation annealing curve of $I_{DDSTDBY}$ for LAN4905 and LAN4906.

3) Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-annealing. The post-annealed DUT are within the spec and the change of this parameter for each DUT is rather negligible.

Table 5. Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

	Pre-Irradiation	Post-Annealing
LAN4903	1.49	1.50
LAN4904	1.48	1.52
LAN4905	1.49	1.50
LAN4906	1.49	1.50

4) Output Characteristic

Figure 5a and 5b show the V_{OL} characteristic curves for the pre-irradiated and post-annealed DUT. All irradiated DUT are within the spec, and no significant radiation effect can be identified. The spec is, at I_{OL} = 12mA, V_{OL} cannot exceed 0.5V.

Figure 6a and 6b show the V_{OH} characteristic curves for the pre-irradiated and post-annealed DUT. All DUT pass the spec, and the radiation effect is negligible. The spec is, at I_{OH} = 8mA, V_{OH} cannot be lower than 2.4V.

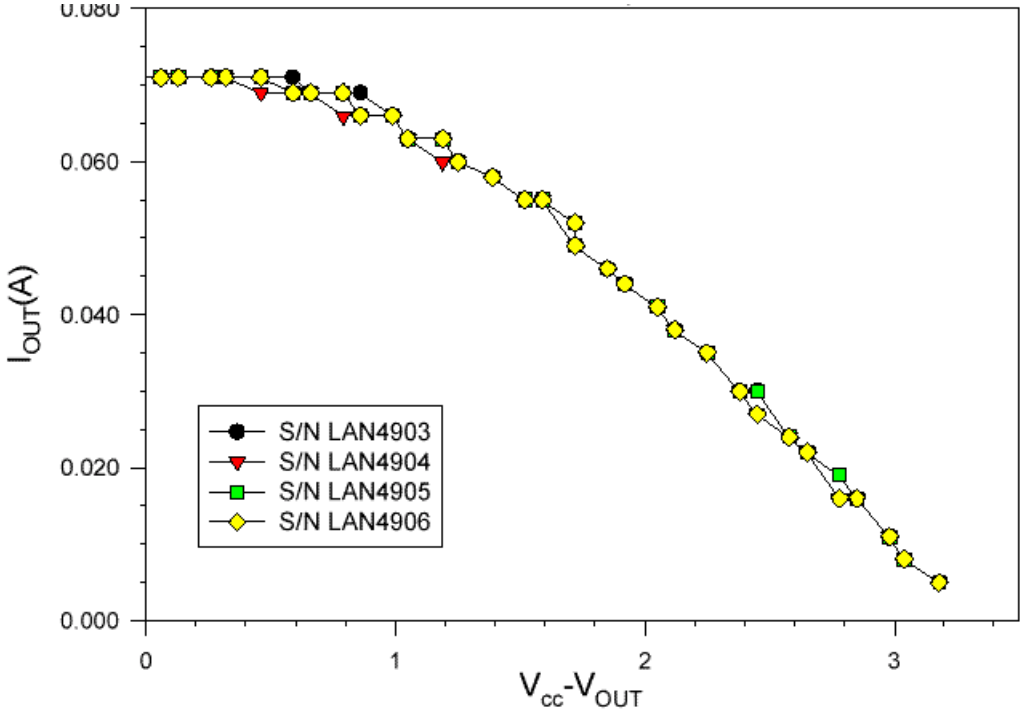

Figure 5a. Pre-irradiation V_{OL} characteristic curves.

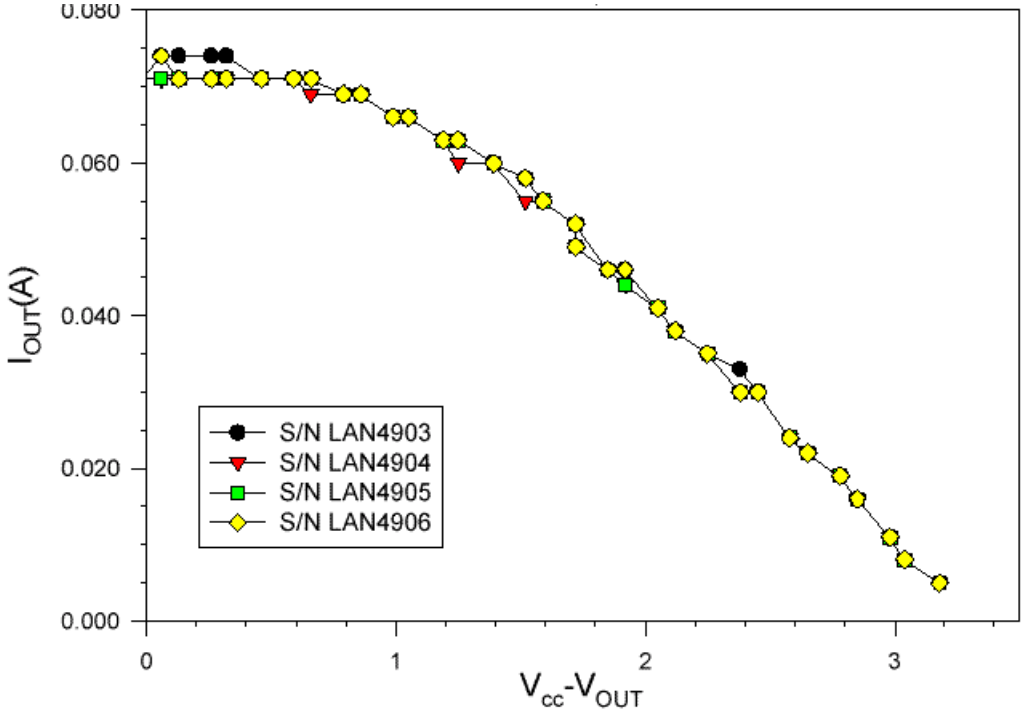

Figure 5b. Post-annealing V_{OL} characteristic curves.

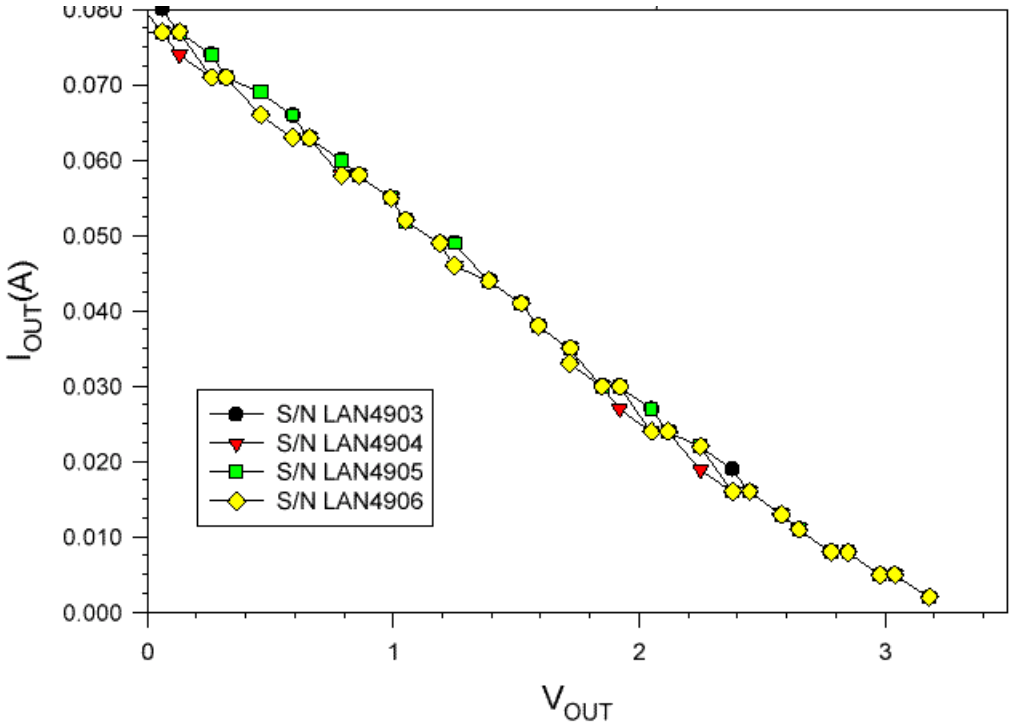

Figure 6a. Pre-irradiation V_{OH} characteristic curves.

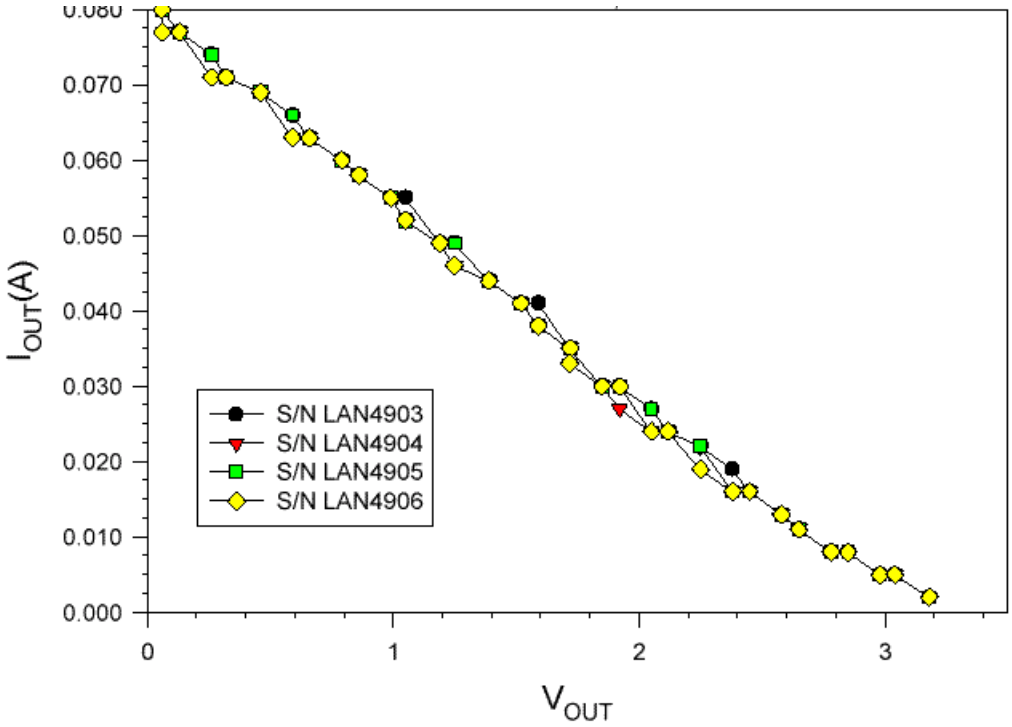

Figure 6b. Post-annealing V_{OH} characteristic curves.

5) Propagation Delays

The propagation delays were measured on three paths, including a combinatorial path, a serial-in path, and a serial-out path. Both the rising edge and falling edge were measured. Table 6, 7 and 8 list the results. The variation due to radiation effect is basically negligible.

Table 6. Propagation Delays of Combinatorial Path (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4903	1434	1448	1439	1433
LAN4904	1448	1458	1448	1439
LAN4905	1479	1486	1476	1466
LAN4906	1444	1451	1439	1430

Table 7. Serial-In Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4903	56.1	55.9	57.2	57.7
LAN4904	56.5	56.9	56.8	56.9
LAN4905	57.1	56.6	58.0	58.1
LAN4906	56.2	56.3	56.4	57.6

Table 8. Serial-Out Delays (ns)

	Rising Output		Falling Output	
	Pre-Irradiation	Post-Annealing	Pre-Irradiation	Post-Annealing
LAN4903	54.9	54.8	55.8	56.4
LAN4904	54.9	55.3	55.5	55.5
LAN4905	55.5	55.3	58.1	56.5
LAN4906	55.3	55.1	55.5	56.0

6) Rising/Falling Edge Transient

The rising and falling edge transient of a D-flip-flop output was measured pre-irradiation and post-annealing. Figures 7-10 show the rising edge transient. Figures 11-14 show the falling edge transient. The radiation effect is basically negligible.

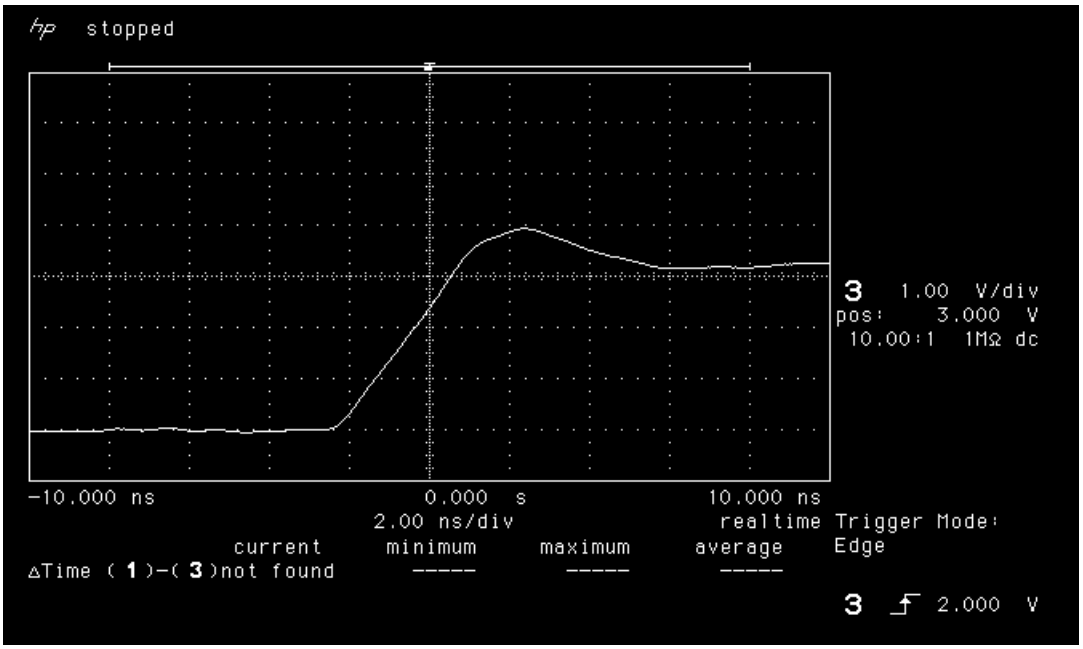

Figure 7a. Rising edge of LAN4903 pre-irradiation.

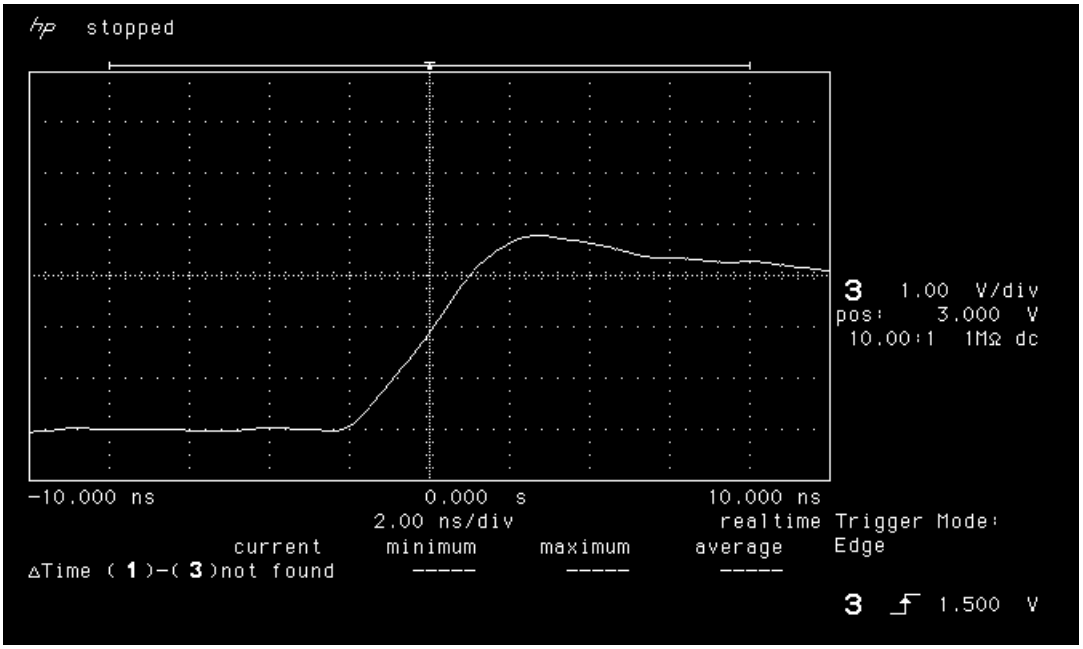

Figure 7b. Rising edge of LAN4903 post-annealing.

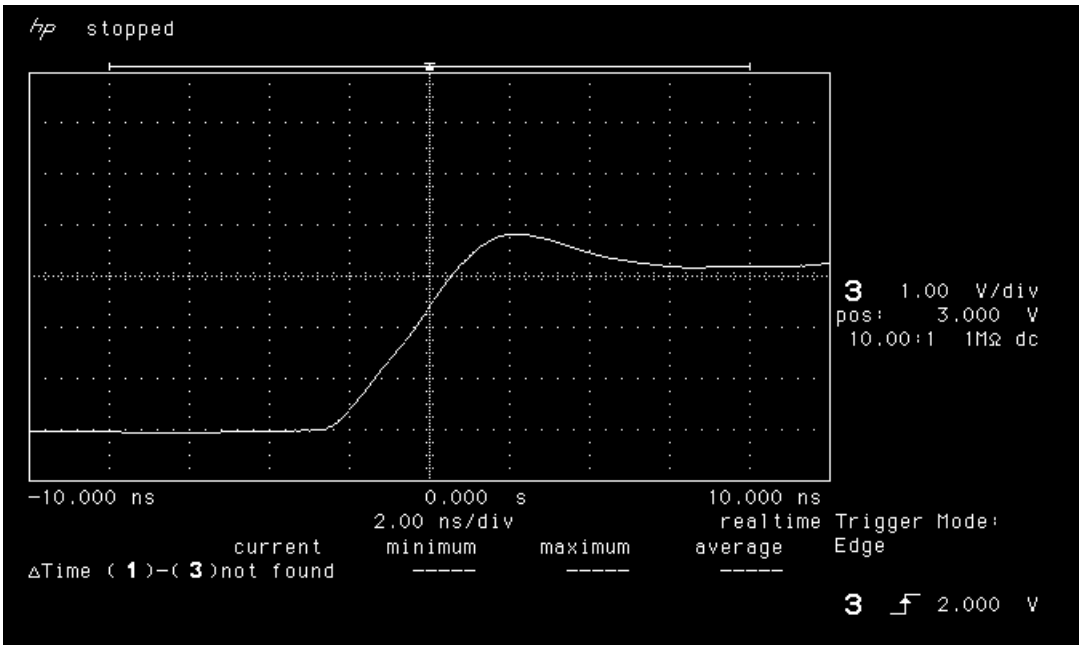

Figure 8a. Rising edge of LAN4904 pre-irradiation.

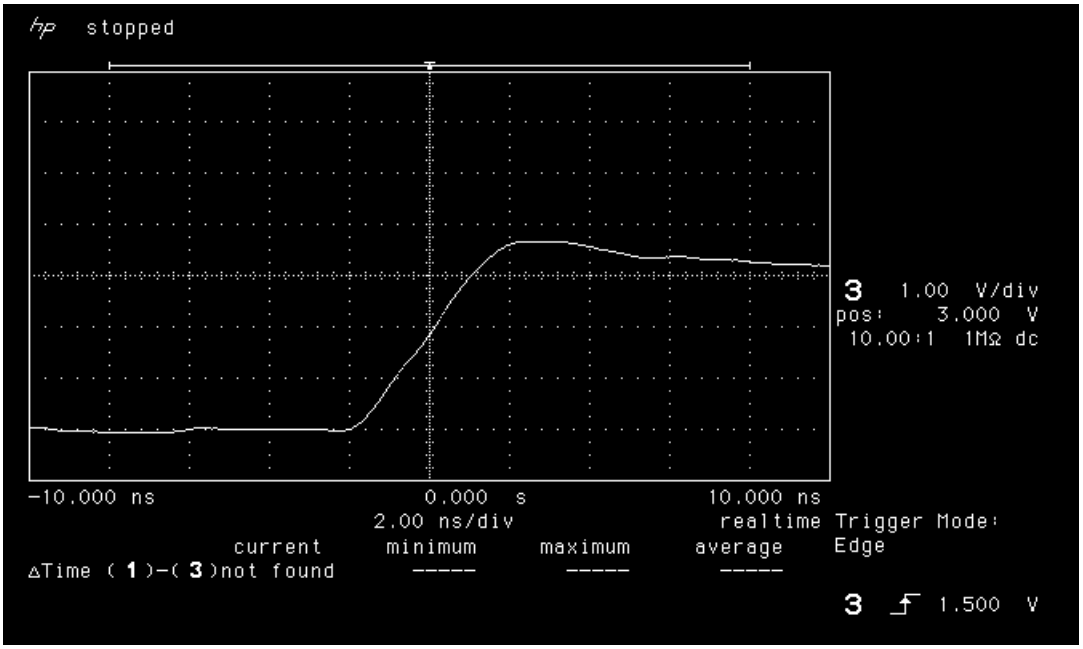

Figure 8b. Rising edge of LAN4904 post-annealing.

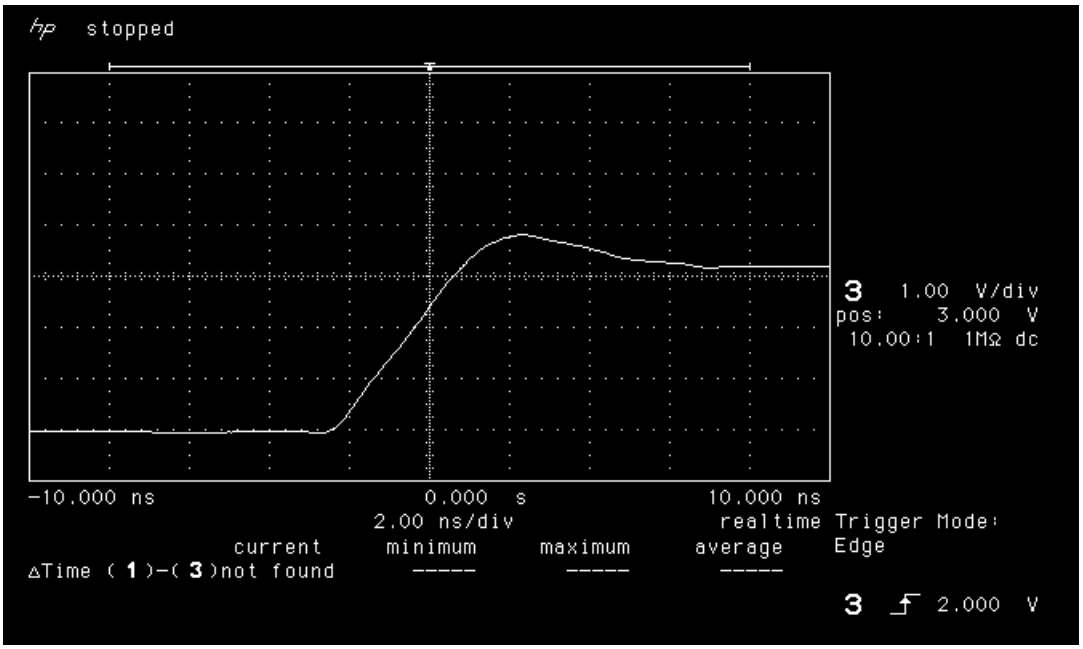

Figure 9a. Rising edge of LAN4905 pre-irradiation.

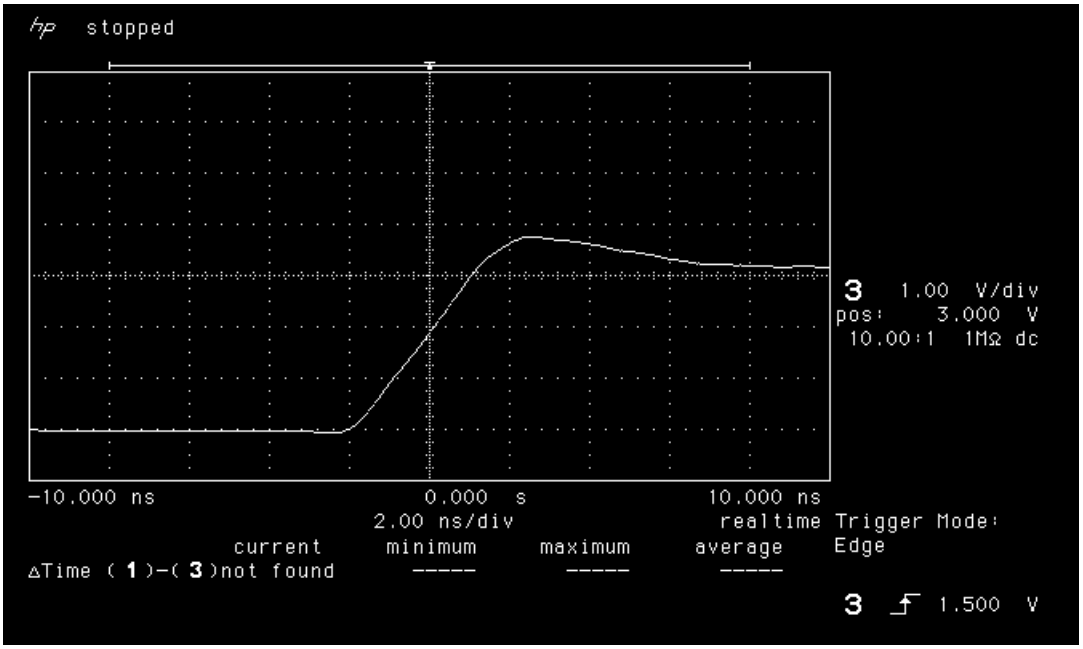

Figure 9b. Rising edge of LAN4905 post-annealing.

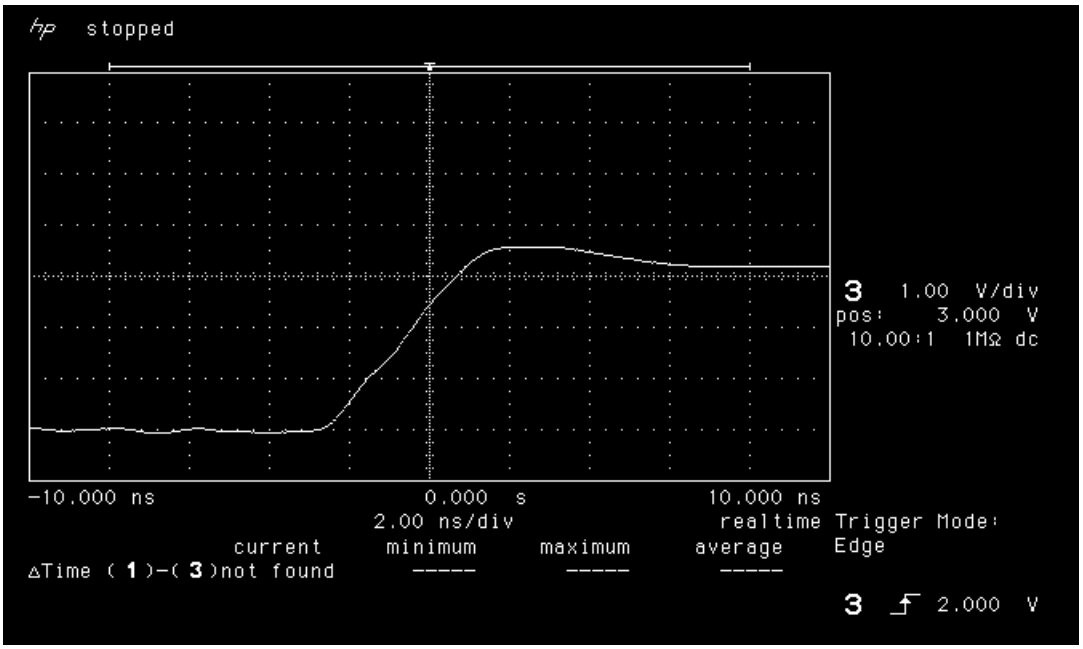

Figure 10a. Rising edge of LAN4906 pre-irradiation.

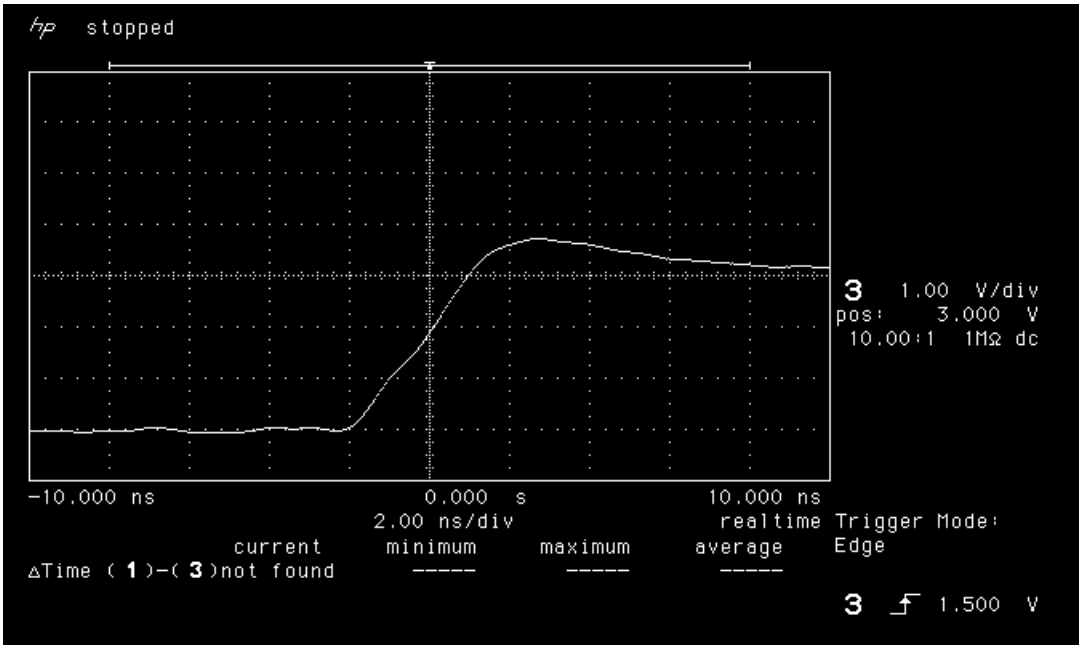

Figure 10b. Rising edge of LAN4906 post-annealing

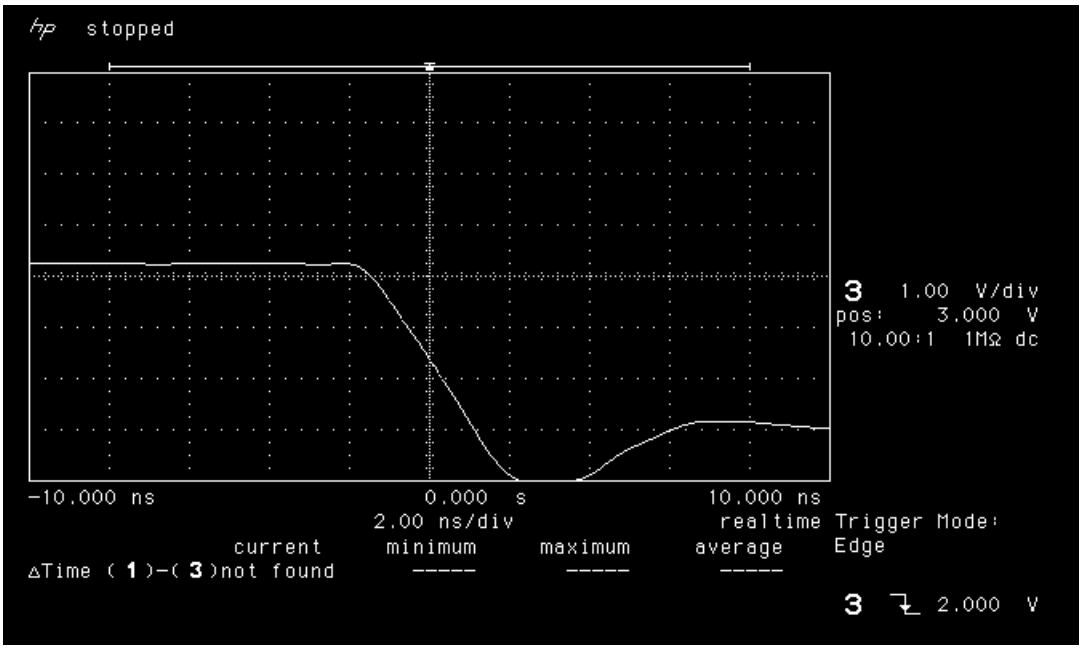

Figure 11a. Falling edge of LAN4903 pre-irradiation

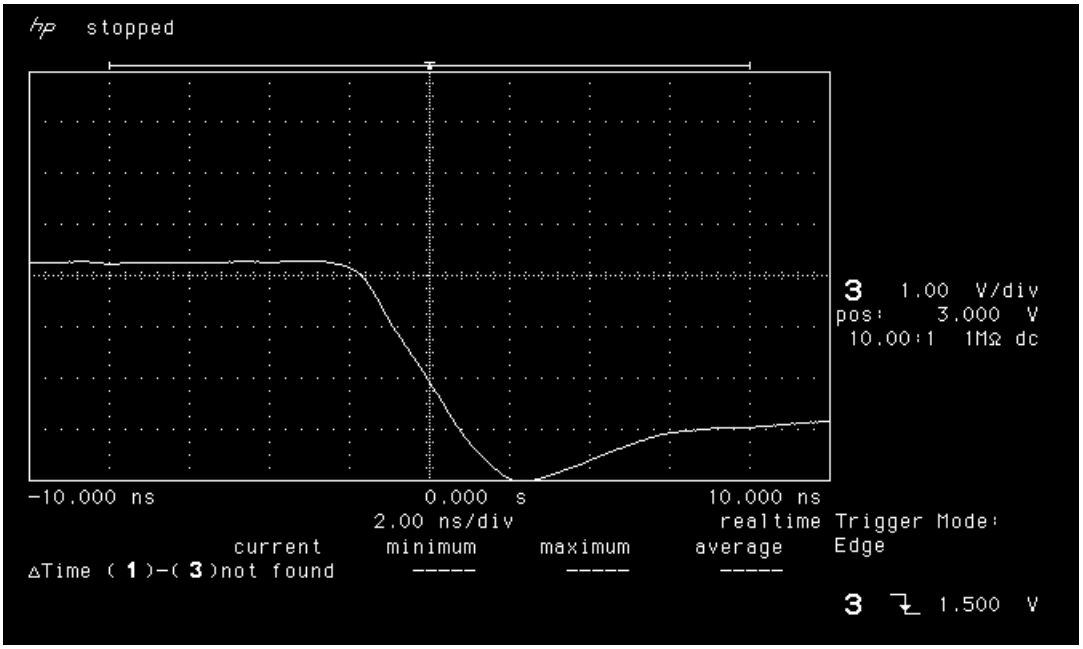

Figure 11b. Falling edge of LAN4903 post-annealing.

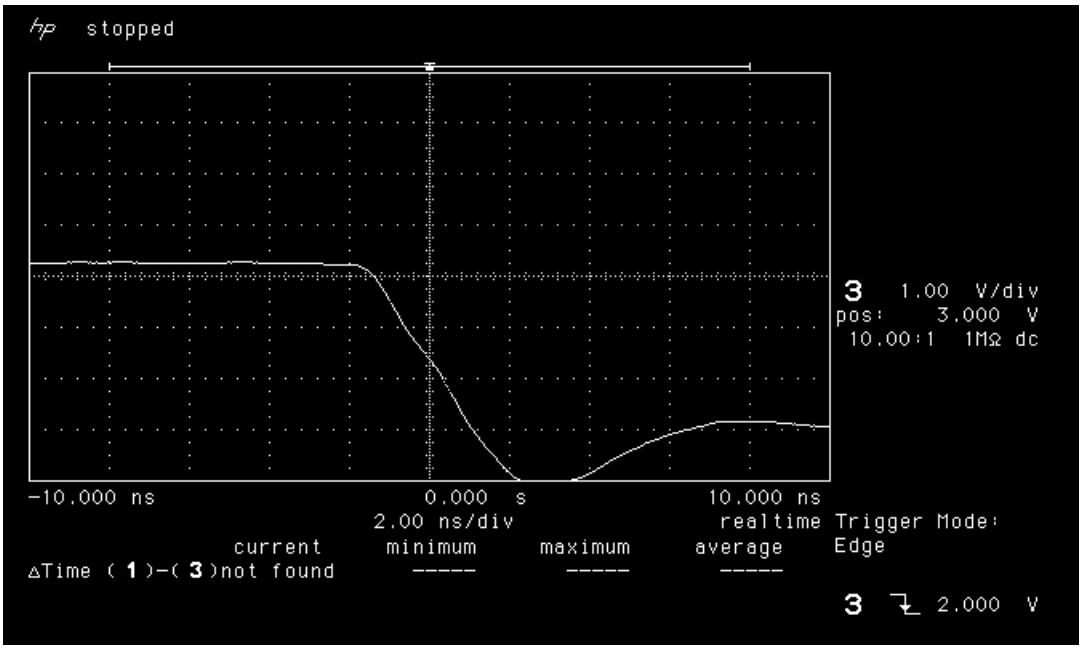

Figure 12a. Falling edge of LAN4904 pre-irradiation.

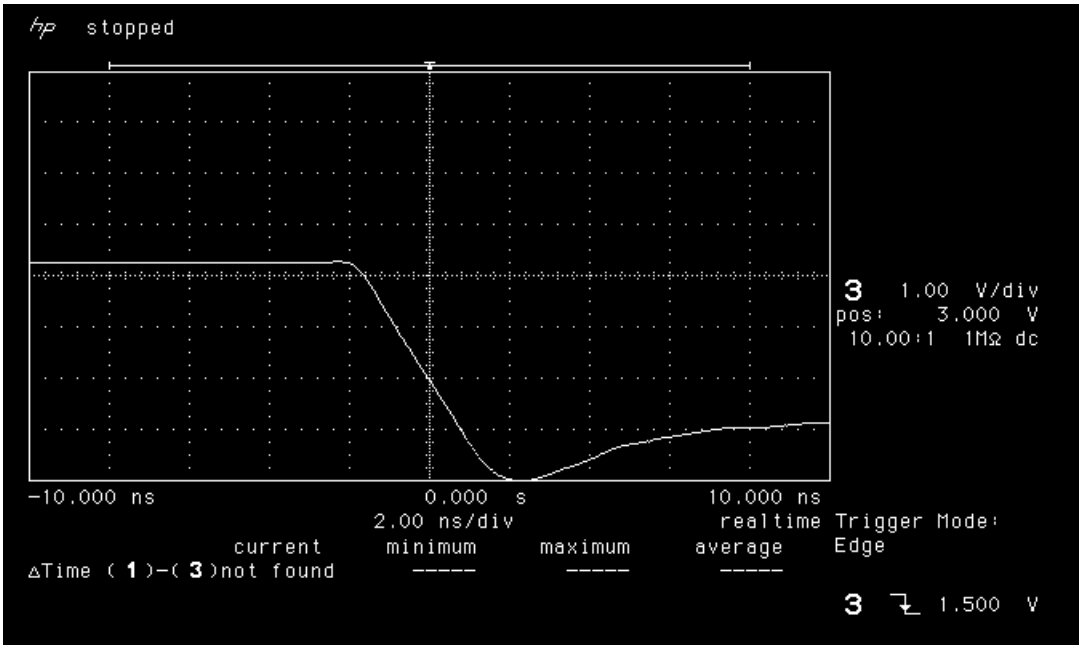

Figure 12b. Falling edge of LAN4904 post-annealing.

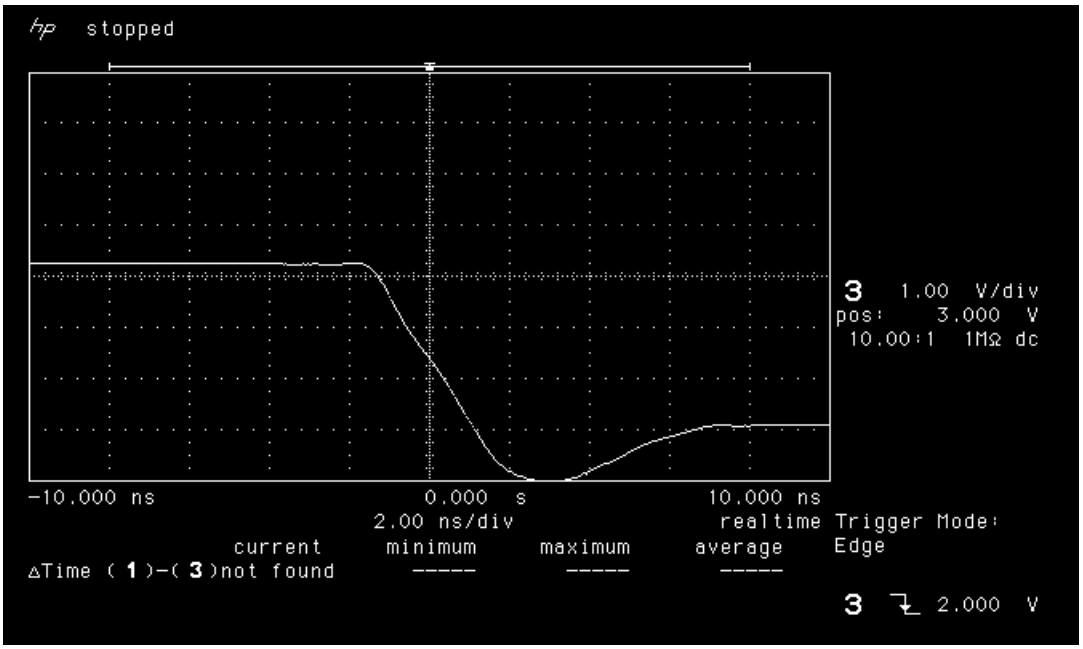

Figure 13a. Falling edge of LAN4905 pre-irradiation.

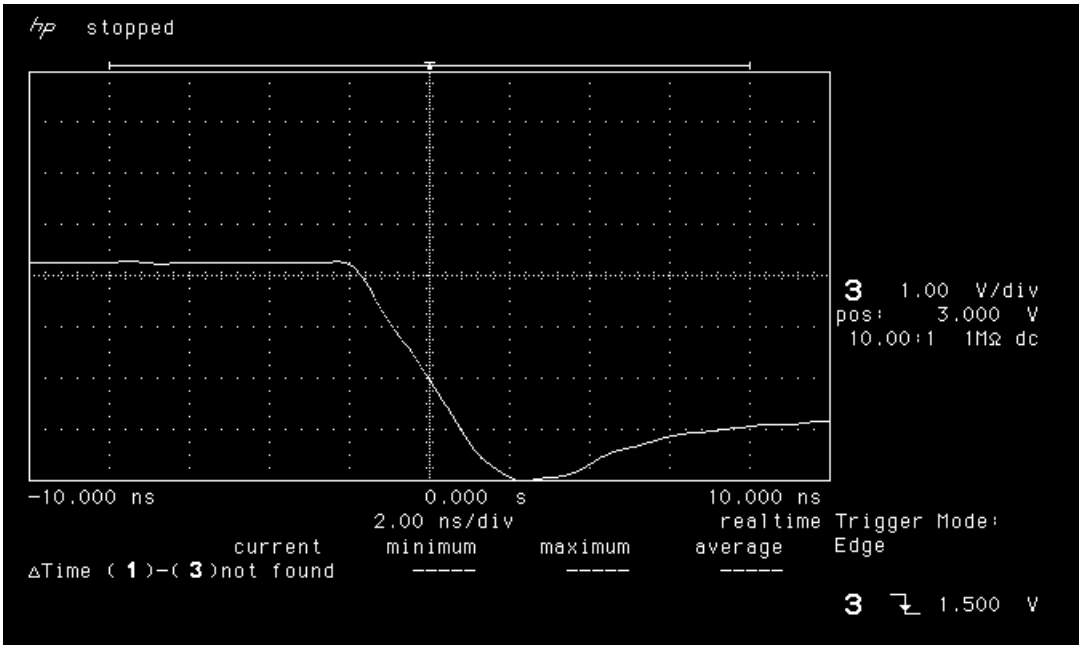

Figure 13b. Falling edge of LAN4905 post-annealing.

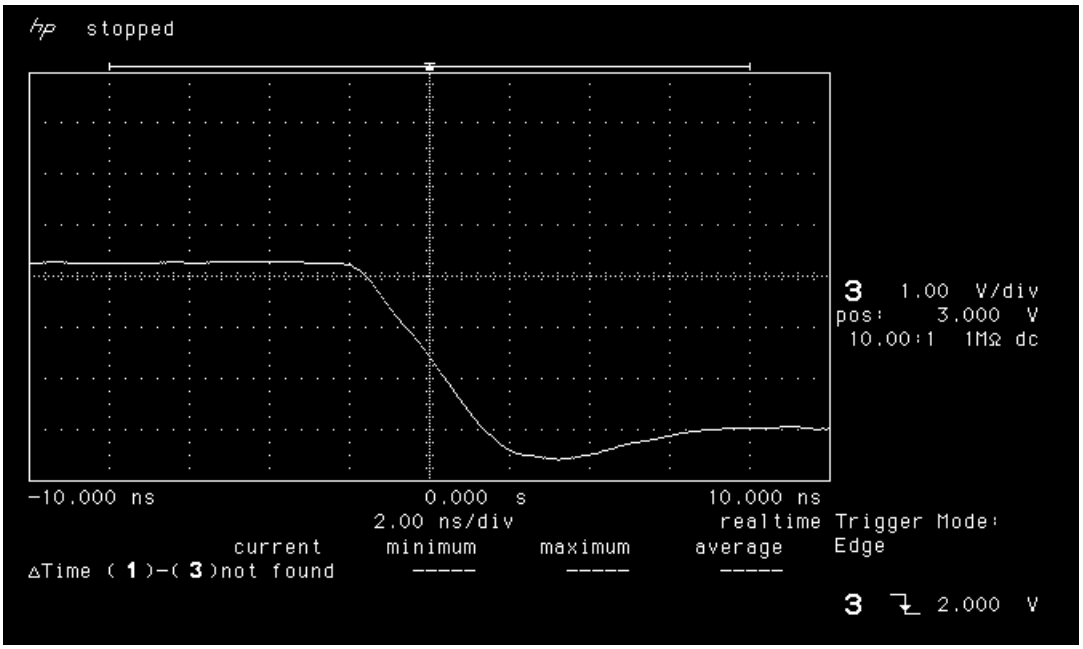

Figure 14a. Falling edge of LAN4906 pre-irradiation

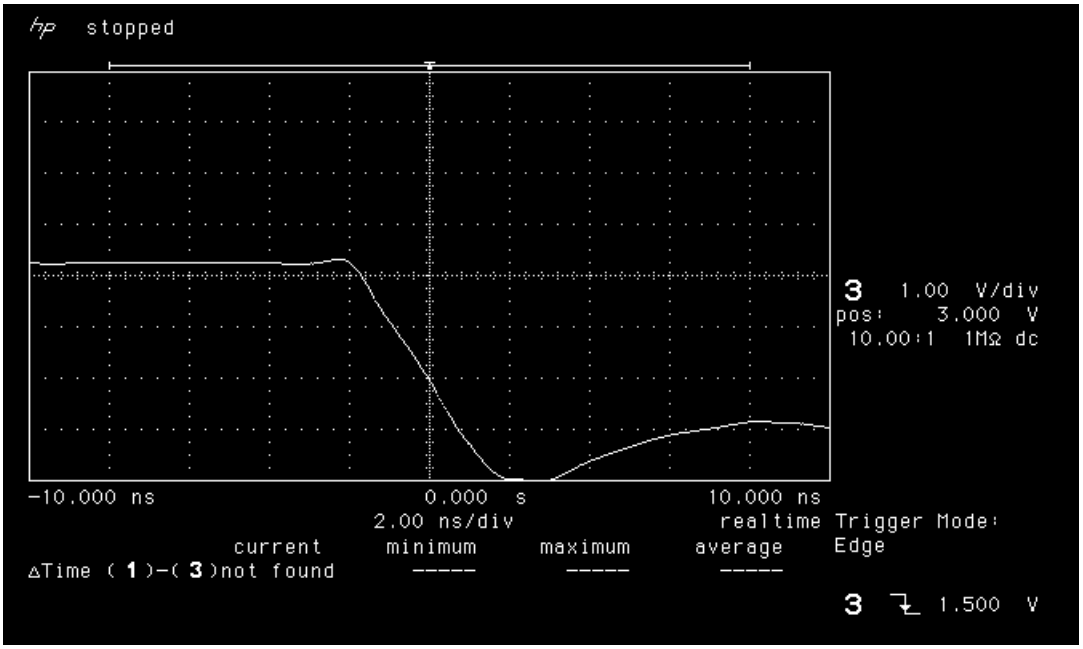

Figure 14b. Falling edge of LAN4906 post-annealing

7) Power-Up Transient

In each measurement, the rise time of the power supply voltage (V_{CC}) was 1.2ms. The board housing the DUT has minimum capacitance so that the transient current comes only from the DUT. Figures 15-18 show the oscilloscope pictures of the power-up transient. In each picture, there is a curve showing V_{CC} ramping from GND to 3.3V, and another curve showing I_{CC}. The scale is, 1V per division for V_{CC} and 100mA per division for I_{CC}. Post 90krad(Si) irradiation/annealing DUT have a radiation induced transient current during power up (see, for example, Figure 16b). However, this transient is very minute. In most case, it can be annealed out completely. Power-up transient current issue has been previously published in RADECS ("Total Dose and RT Annealing Effects on Startup Current Transient in Antifuse FPGA," by J.J. Wang, R. Katz, I. Kleyner, F. Kleyner, J. Sun, W. Wong, J. McCollum, and B. Cronquist, RADECS 99, 13-17 Sept 1999, pp. 274-278.)

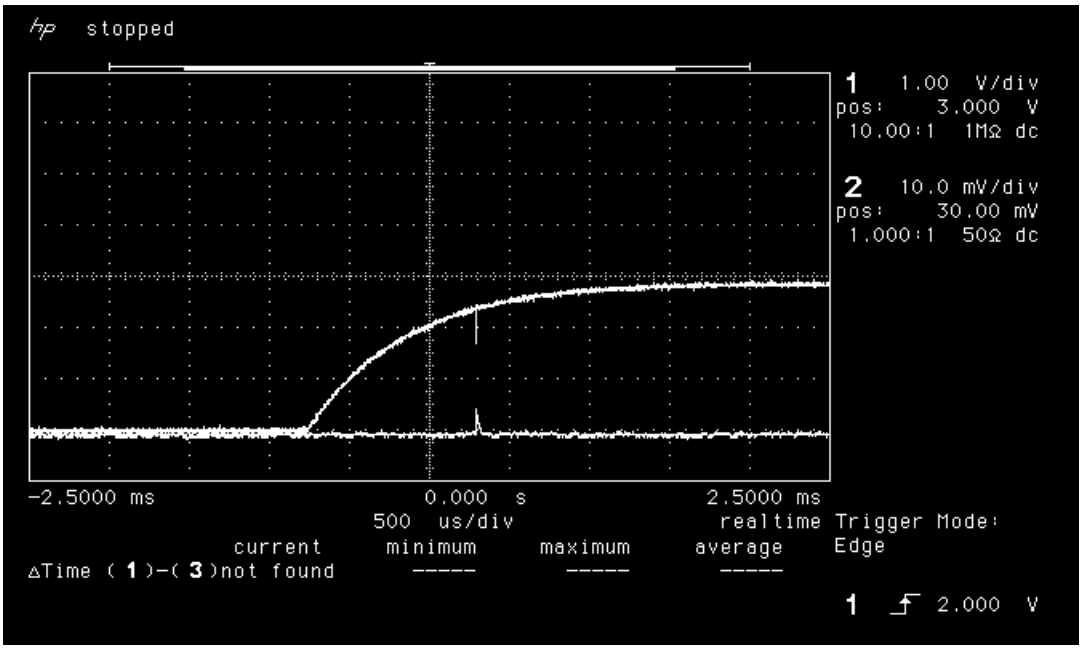

Figure 15a. Power-up transient of LAN4903 pre-irradiation.

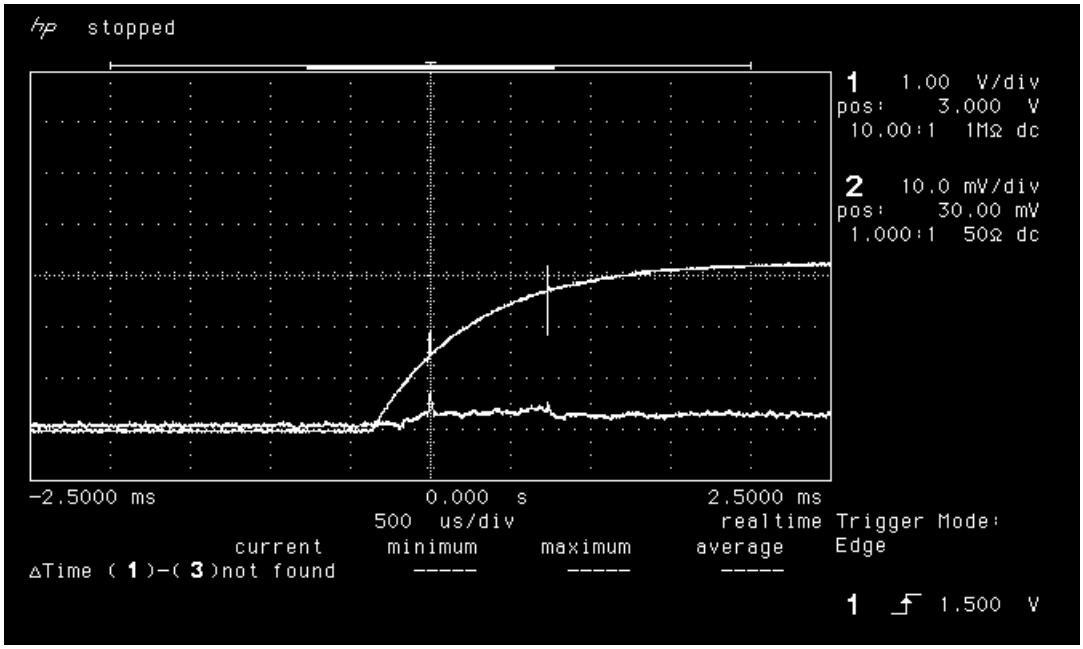

Figure 15b. Power-up transient of LAN4903 post-annealing.

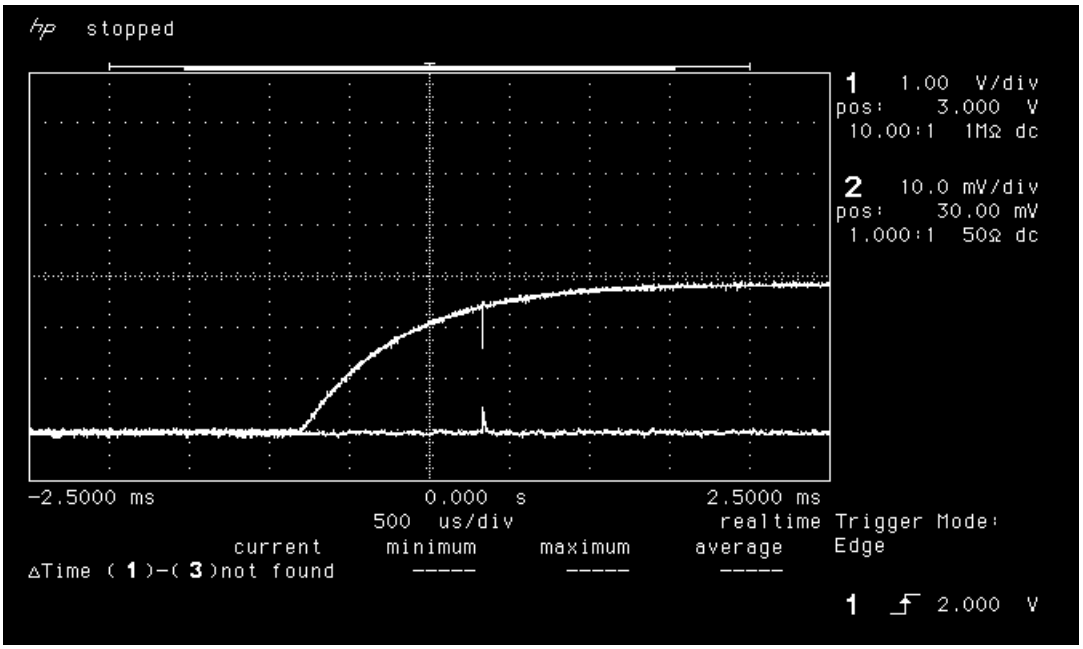

Figure 16a. Power-up transient of LAN4904 pre-irradiation.

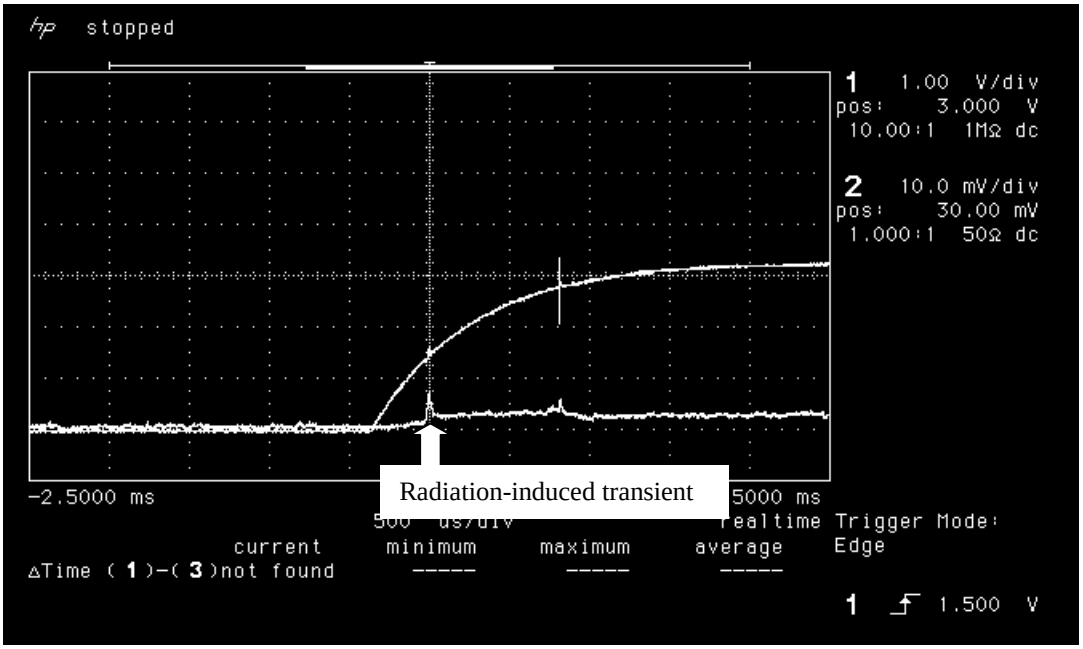

Figure 16b. Power-up transient of LAN4904 post-annealing.

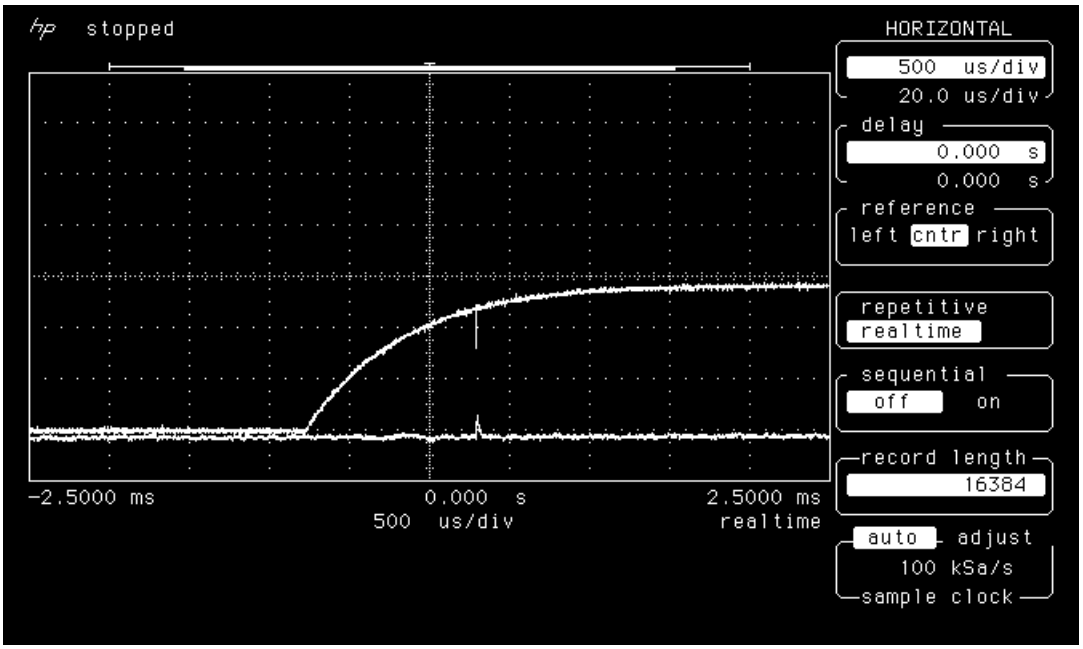

Figure 17a. Power-up transient of LAN4905 pre-irradiation.

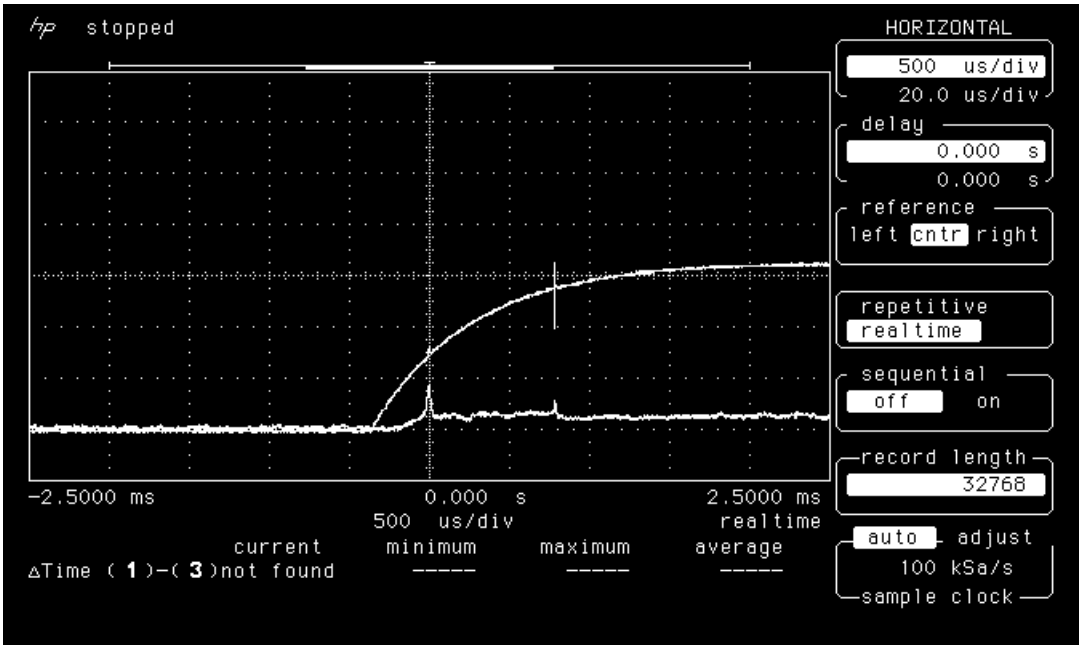

Figure 17b. Power-up transient of LAN4905 post-annealing.

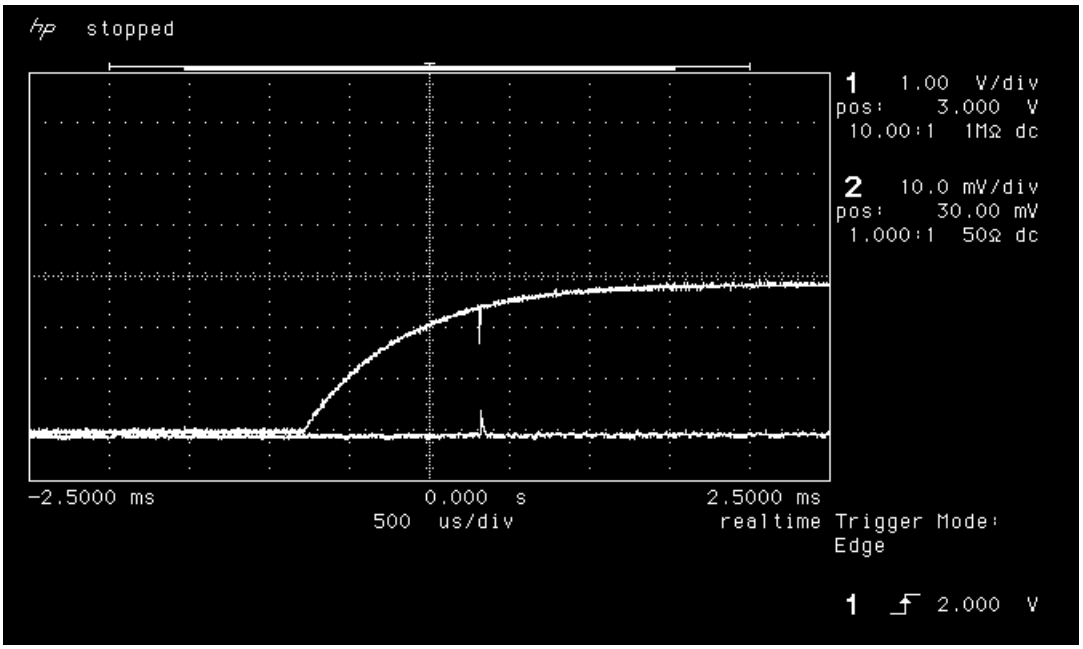

Figure 18a. Power-up transient of LAN4906 pre-irradiation

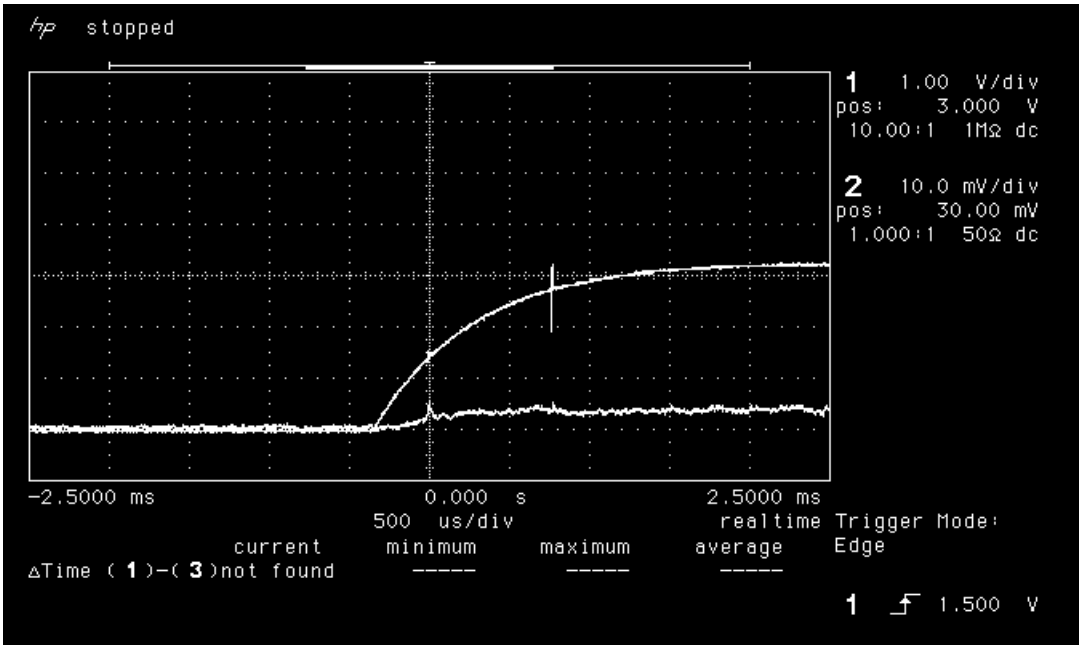

Figure 18b. Power-up transient of LAN4906 post-annealing