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Synplify Pro® for Actel Edition Release Notes

Version E-2010.09A, September 2010

Publication Version 01

Release Note Topics

About this Release

This E-2010.09A release includes software improvements for the Synplify Pro® Actel Edition product. See *New Actel Feature Support* on page 2 and *New Features and Enhancements* on page 4 for the cumulation of features and enhancements included in the release.

New Actel Feature Support

This section contains a summary of the new Actel-specific features and enhancements for version E-2010.09A. Topics include:

- New and Updated Actel Device Support
- SmartFusion Macro Support
- Actel Support for Libero/Designer 9.1

New and Updated Actel Device Support

The synthesis tool *adds* support for the following Actel device parts and packages:

Technology	Part	Package	Speed Grade
SmartFusion	A2F200M3F	288 CS	Std, -1
	A2F500M3G	288 CS	Std, -1
			-1
Fusion	AFS600	256 FBGA K	Std, -1
	AFS600	484 FBGA K	Std, -1
	AFS1500	256 FBGA K	Std, -1
	AFS1500	484 FBGA K	Std, -1
	M1AFS600	256 FBGA K	Std, -1
	M1AFS600	484 FBGA K	Std, -1
	M1AFS1500	256 FBGA K	Std, -1
	M1AFS1500	484 FBGA K	Std, -1
ProASIC3L	RT3PE600L	LGA484 CCGA484	Std, -1
	RT3PE3000L	LGA484 CCGA484 LGA896 CCGA896	Std, -1
ProASIC3	A3PN125	VQFP100	Std, -1, -2
Axcelerator	RTAX2000D	CQFP352	Std

Technology	Part	Package	Speed Grade
IGLOO	AGL250V2	CS284	Std
	AGL400V2	CS284	Std
	AGL250V5	CS284	Std
	AGL400V5	CS284	Std
	AGLN125V2	VQFP100	Std
	AGLN125V2	CS81	Std
	AGLN125V5	VQFP100	Std
	AGLN125V5	CS81	Std

The synthesis tool *removes* support for the following Actel device parts and packages:

Technology	Part	Package	Speed Grade
ProASIC3L	RT3PE600L	CCGA/LGA484	Std, -1
	RT3PE3000L	CCGA/LGA484 CCGA/LGA896	Std, -1

SmartFusion Macro Support

The Synplify Pro software supports the SmartFusion FAB_CCC and FAB_CCC_DYN macros.

DSP Cascade Chain Inference

The MATH18x18 block cascade feature supports the implementation of multi-input Mult-Add/Sub for devices with MATH blocks. The software packs logic into MATH blocks efficiently using hard-wired cascade paths, which improves the quality of results (QoR) for the design.

For details, see the online help or `reference.pdf`->*DSP Block Inference->DSP Cascade Chain Inference.*

Multiplier-Accumulators (MACs) Inference

The Multiplier-Accumulator structures use internal paths for adder feedback loops inside the MATH18x18 block instead of connecting it externally.

For details, see the online help or `reference.pdf`->*DSP Block Inference->Multiplier-Accumulators (MACs) Inference.*

Actel Support for Libero/Designer 9.1

This version of the software supports Actel's latest design environment.

New Features and Enhancements

This section contains a summary of the new features and enhancements for version E-2010.09A, which includes:

- Resolve Mixed Drivers Option
- Compiler Enhancements

Resolve Mixed Drivers Option

When a net is driven by a VCC or GND and active drivers, enable this option to connect the net to the GND or VCC. Resolve Mixed Drivers is a new device option on the Implementation Options panel.

For details, see the online help or `reference.pdf`->*Batch Commands and Scripts->Batch Commands for Synthesis->set_option*.

Compiler Enhancements

This release includes the following compiler enhancements:

- 64-bit Compiler Support
- Compiler Design Constraints
- Context Help Editor
- Verilog Enhancements
- SystemVerilog Enhancements
- VHDL 2008 Enhancements

64-bit Compiler Support

The FPGA synthesis software now runs the 64-bit compiler on 64-bit operating systems.

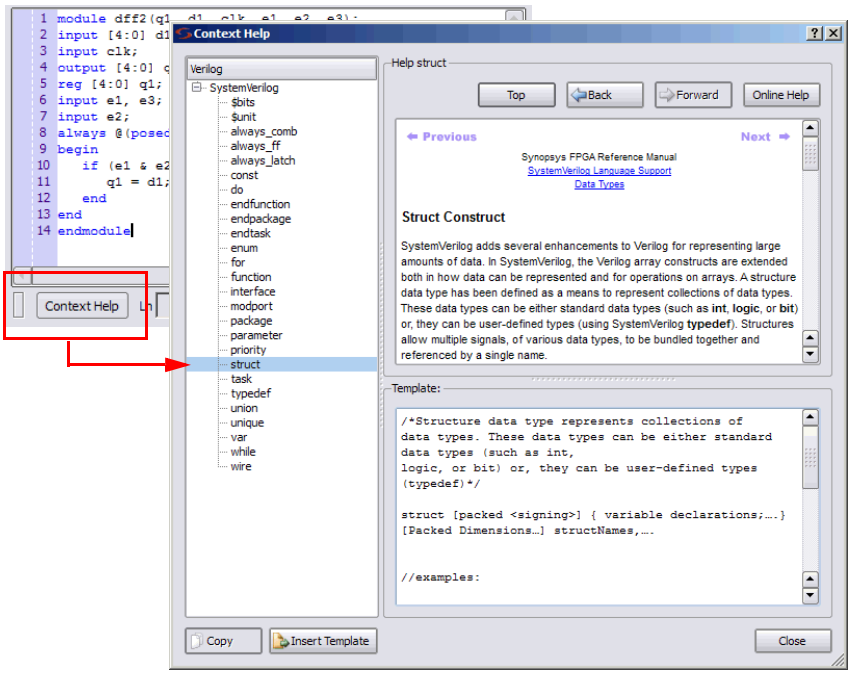
Compiler Design Constraints

The Compiler Design Constraint (`.cdc`) file provides a convenient way to specify supported attributes and directives, without making changes to your HDL files. During compilation, the tool passes all active `.cdc` files to the compiler. The compiler references the object names in these files with the original RTL objects to assign the corresponding directive or attribute.

For details, see the online help or `user_guide.pdf`->*Setting up a Logic Synthesis Project->Entering Attributes and Directives->Specifying Attributes and Directives in a .cdc File* and `reference.pdf`->*Synthesis Attributes and Directives->How Attributes and Directives are Specified->Compiler Design Constraint File Examples*

Context Help Editor

Use the Context Help button at the bottom of the GUI window, to display the keyword help for selected SystemVerilog constructs in an editor file. This editor window allows you to easily insert the template or copy-and-paste code into the design that you are going to synthesize.



For more information, see online help or `reference.pdf->`*`User Interface Overview->Windows and Views->Context Help Editor`*.

Verilog Enhancements

The following Verilog capabilities are available in the release:

- A new $clog2 constant math function has been defined that returns the value of log base 2 for the argument passed.
- Includes support for cross-module referencing which is a method of accessing an element across modules.
- A configuration block can be defined that specifies a set of rules for the exact source description to be applied to an instance or module. Configuration blocks are defined outside of a module definition. (Beta Support)

For details, see the online help or `reference.pdf->`

- *Verilog Language Support->Verilog 2001 Support->$clog2 Constant Math Function*
- *Verilog Language Support->Verilog 2001 Support->Cross-Module Referencing*
- *Verilog Language Support->Verilog 2001 Support->Configuration Blocks*

SystemVerilog Enhancements

The following SystemVerilog capabilities are available in the release:

- Streaming Operators Update

  Streaming operations can now be performed on both the left and right sides of the equation. Previously, the Synopsys Verilog compiler only supported streaming operations on the right side of the equation.

- Type Parameters

  SystemVerilog includes the ability for a parameter to also specify a data type.

- Set Membership Operator

  The set membership operator, also referred to as the *inside* operator, returns the value TRUE when the expression value is present in the value list.

For details, see the online help or `reference.pdf->`

- *SystemVerilog Language Support->Operators and Expressions->Streaming Operator*
- *SystemVerilog Language Support->Data Declaration->Type Parameters*
- *SystemVerilog Language Support->Operators and Expressions->Set Membership Operator*

VHDL 2008 Enhancements

The following VHDL 2008 capabilities are available in the release:

- Adds a new type of case-generate statement.
- Legalizes the concept of unconstrained arrays.
- Allows element types for records to be unconstrained.
- Supports matching case and matching select statements.

For details, see the online help or `reference.pdf->`

- *VHDL 2008 Language Support->Case-generate Statements*
- *VHDL 2008 Language Support->Unconstrained Data Types*
- *VHDL 2008 Language Support->Unconstrained Record Elements*
- *VHDL 2008 Language Support->Matching case and select Statements*

Documentation

This section includes the following documentation topics:

- Accessing PDF Documents
- Accessing Online Help

The Synopsys FPGA Synthesis product documentation set consists of the following:

Document	Format	Access
Online Help	HTML Help	See *Accessing Online Help* on page 8.
Document Type • User Guide • Reference Manual • Release Notes	PDF and HTML help	See *Accessing PDF Documents* on page 7.
• Error Messages	HTML Help	Select Help->Error Messages. Click on the error message in the log file or the Message Viewer window.

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

You can access PDF documents from the Documentation tab within SolvNet. To access PDF documents either from the software or without running the software, see the table below for details.

Synopsys FPGA Products

From Linux	From outside the software, select: • Open Acrobat Reader: `acroread` Open *`install_directory`*`/documents/`*`docfile`*
From Windows	• Start->Programs->Synopsys->Synplify Pro for Actel Edition E-2010.09A->Documents Then, select the desired document. • From inside the software for all platforms, select Help->Online Documents. In the Open dialog box, select the desired document: - `user_guide.pdf` - `reference.pdf` - `release_notes.pdf`

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Accessing Online Help

Topics include:

Synopsys FPGA Products

For the FPGA products, you can access help from within the software or outside of the tool.

Accessing Help from inside the tool	
All platforms	Press F1 or select Help->Help. For context-sensitive help, click F1 in a dialog box.
Accessing Help from outside the tool	
On a Windows machine	Select Start->Programs->Synopsys->Synplify Pro Actel Edition E-2010.09A->Help
From Linux	Run synplify_pro_help.

Displaying Graphics

In some cases, the online help graphics do not display correctly. This is usually because your Display setting is 256-Color. Reset it to 16-bit Color, then reopen the online help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

Annotated Properties for Analyst Behavioral Changes

Previously, the Annotated Properties for Analyst option was enabled by default and annotated properties were generated after you compile the design. However in this release, enable the Annotated Properties for Analyst option that is turned off by default and synthesize (compile and map) the design to generate annotated properties.

Solution: This will be re-evaluated in a future release.

HDL Analyst Crash Using Mouse Strokes

When you use the Pop Up mouse stroke in the top-level HDL Analyst view, the synthesis tool crashes.

Solution: This will be fixed in a future release.

Verilog Include Paths Missing from VCS Integration

If Verilog include paths have been added to your Project file, these paths are not automatically added to the VCS script.

Solution: You must add the Verilog include paths manually. To do this, use one of the following workarounds:

- From the Run VCS Simulator dialog box, add `+incdir+<include path>` in the Verilog Compile options field.
- Modify the VCS script file, adding the `+incdir+<include path>` to all or any relevant vlogan commands.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (.prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis UI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project UI.

Digital Line Detect Error Appears (Windows XP)

When launching the synthesis software, a Digital Line Detect error occasionally appears on a Dell PC running Windows XP.

Solution: Download the latest update from Dell Corporation. See the following URL for more information.

http://support.dell.com/support/downloads/format.aspx?releaseid=r84541&c=us&l=en&s=gen&cs

Alternatively, you can deselect the Digital Line Detect entry in your system configuration. To do this:

1. Select Run from the Start menu.
2. Type `msconfig` in the open field and click OK.

   The System Configuration Utility dialog box appears.
3. Select the Startup tab and scroll down to the Digital Line Detect entry.
4. Deselect the checkbox to disable it.

Invoking Tool can be Slow on Linux With Network Problems

Invoking the synthesis tools might be slow when you are experiencing network problems on Linux platforms, such as when a mounted drive is not accessible.

Solution: Delete the `$HOME/.config/Trolltech.conf` file to avoid caching. This might help to invoke the tool faster.

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