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Synplify Pro® for Microsemi Edition Release Notes

Version G-2012.09M-SP1, February 2013

Publication Version 01

Release Note Topics

About this Release

This G-2012.09M-SP1 release includes software features and enhancements for the Synplify Pro® Microsemi Edition product. For the complete summary of features and enhancements contained in this release and the baseline G-2012.09M release, see *G-2012.09M-SP1 Features and Enhancements* on page 2 and *G-2012.09M Features and Enhancements* on page 3.

G-2012.09M-SP1 Features and Enhancements

This section contains a summary of the features and enhancements for the G-2012.09M-SP1 release. Topics include:

New Device Support

This release provides logic synthesis support for the Microsemi SmartFusion2 devices.

MACC Inference

SmartFusion2 devices support 18x18-bit signed multiply-accumulate blocks. The architecture includes dedicated components called SmartFusion2 MACC blocks, which can perform DSP-related operations like multiplication followed by addition, multiplication followed by subtraction, and multiplication with accumulate.

The Synplify Pro tool extracts the following logic structures from the hardware description and maps them to MACC blocks:

- Multipliers
- Mult-Adds (multiplier followed by an adder)
- Mult-Subs (multiplier followed by a subtractor)
- Mult-Acc (multiplier-accumulator structures)

RAM Inference

SmartFusion2 devices support two types of RAM macros—RAM1K18 and RAM64x18. The Synplify Pro tool identifies the RAM structure from the RTL and implements it using RAM1K18 or RAM64x18 based on the size of the RAM.

The following criteria describes the default behavior for how the Synplify Pro software selects the RAM macro. You can override the default behavior by using the `syn_ramstyle` attribute.

- True Dual-Port Synchronous Read Memory; the software maps to RAM1K18 irrespective of the memory size.
- Simple Dual-Port or Single-Port Synchronous Memory:
  - If the RAM memory size is 4608 bits or more, the software maps to RAM1K18.
  - If the RAM memory size is greater than 12 bits and less than 4608 bits, the software maps to RAM64x18.
  - If the RAM memory size is less than or equal to 12 bits, the software maps to registers.
- Simple Dual-Port or Single-Port Asynchronous Memory; if the size of the memory is 12 bits or more, the software maps to RAM64x18. Otherwise, the software maps to registers.

You can apply `syn_ramstyle` to control memory mapping. To map to:

- RAM1K18, set `syn_ramstyle = "lsram"`
- RAM64x18, set `syn_ramstyle = "uram"`
- Registers, set `syn_ramstyle = "registers"`

Use this attribute to override the default RAM behavior.

Global Buffer Promotion

The synthesis tool promotes clock, asynchronous set/reset, and data nets on the global buffer (CLKINT) depending on the threshold values. The threshold values are as follows:

- Clock nets—2
- Asynchronous set/reset—12
- Data nets—5000

G-2012.09M Features and Enhancements

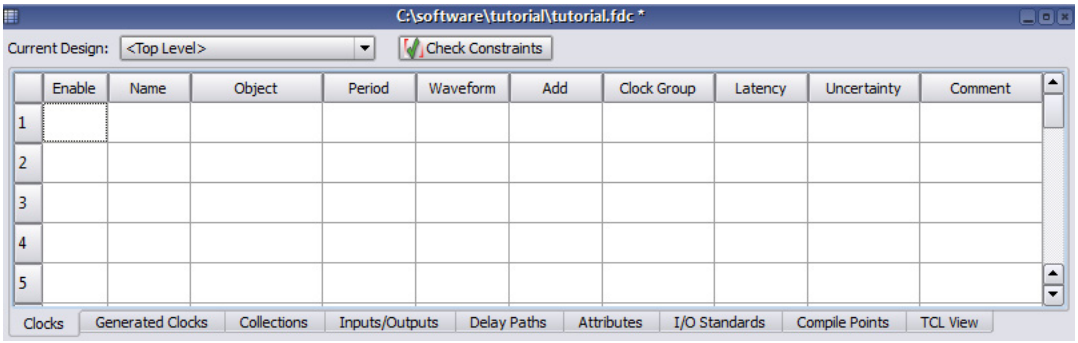
This section contains a summary of the features and enhancements for the baseline G-2012.09M release. Topics include:

New Constraints Style

The FPGA synthesis tool is replacing the legacy Synplify-style timing constraints (for example, define_clock and define_false_path) with the Synopsys standard timing constraints (for example, create_clock and set_false_path). A new FPGA Design Constraint (FDC) file is generated that contains these Synopsys standard timing constraints and the design constraints (for example: define_attribute and define_io_standard).

As a result of these updates, there are some changes in the use model:

- Instead of a constraint file created in the legacy SDC format, the tool now supports an FDC file that includes both timing and non-timing constraints (design constraints).
- For existing designs, use the sdc2fdc command to do a one-time conversion of the constraints from legacy SDC constraints to create an FDC file that contains Synopsys SDC standard timing constraints and non-timing constraints. See *sdc2fdc Conversion Script* on page 4.
- For new designs, the SCOPE editor has been enhanced to support the timing constraint changes, so that new constraints can be entered correctly.



For more information, see the online help or reference.pdf->Constraints for an overview about constraints and the SCOPE Constraints Editor for descriptions of the SCOPE panels.

For more information, see the online help or user_guide.pdf->Specifying Constraints for details on how to use the SCOPE editor.

sdc2fdc Conversion Script

Use the sdc2fdc command to do a one-time conversion of Synplify-style timing constraints (for example, define_clock and define_false_path) to Synopsys standard timing constraints (for example, create_clock and set_false_path). Load your Project file and from the Tcl command line in the synthesis tool, the sdc2fdc command scans the input SDC files and attempts to convert constraints for the implementation. The timing and design constraints are written to an FDC file and saved to your project. You can open this output file in SCOPE and analyze its results.

For more information, see the online help or user_guide.pdf->Specifying Constraints->Converting SDC to FDC and the reference.pdf->Utilities->sdc2fdc Tcl Shell Command.

Read Write Check on RAM

The Read Write Check on RAM option on the Device panel lets the synthesis tool insert bypass logic around the RAM to prevent a simulation mismatch between the RTL and post-synthesis simulations. The synthesis software does not insert bypass logic around the RAM that read and write to the same address simultaneously. Enable this option, when you want to simultaneously read and write to the same RAM location.

For more information, see the online help or reference.pdf->Designing with Microsemi Appendix for devices that support this option and Batch Commands and Scripts->Batch Commands for Synthesis->set_option for the Tcl syntax.

IP Encryption

Synopsys IP encryption options have been expanded to include additional recommendations from the IEEE P1735 working group as it moves towards an IEEE ballot. P1735 is an emerging standard, evolved from a donation of OpenIP plus other contributions, that allows IP vendors to safely distribute encrypted IP and allows EDA tools to read that IP. Both the OpenIP and IEEE 1735 standards will be supported during this transition period. For creators of IP, scripts are available in the release to simplify the IP encryption process.

For more information, see the online help or user_guide.pdf->Working with IP Input->Working with Encrypted IP.

HDL Analyst Enhancement

The HDL Analyst enhancements include the following:

- Enable the Display color-coded clock nets option from the General tab of the HDL Analyst Options dialog box to display clock nets with the color green in the HDL Analyst View.
- You can easily locate compile points of type {hard} in the Technology view because they are now displayed with the color green.

Interactive Attribute Examples

The Interactive Attribute Examples wizard lets you select pre-defined attributes to run in a project. Click Generate Run to run synthesis for the implementations. When synthesis completes:

- The Technology view opens to show how the selected attribute impacts synthesis.
- You can compare resource utilization and timing information between implementations in the Log Watch window.

To use this tool, see the online help or reference.pdf->User Interface Overview->Other Windows and Views->Interactive Attribute Examples.

Compiler Enhancements

Compiler enhancements for this release include:

- SystemVerilog Type Operator Support
- VHDL Implicit Data-type Defaults
- The orig_inst_of Property for Parameterized Modules
- VHDL 2008 Enhancements for Bit-string Literals

SystemVerilog Type Operator Support

SystemVerilog provides a type operator as a way of referencing the data type of a variable or an expression.

For details about syntax and coding examples, see the online help or reference.pdf->System-Verilog Language Support->Operators and Expressions->Type Operator.

VHDL Implicit Data-type Defaults

Type default propagation avoids potential simulation mismatches that are the result of differences in behavior with how initial values for registers are treated in the synthesis tools and how they are treated in the simulation tools.

With implicit data-type defaults, when there is no explicit initial-value declaration for a signal being registered, the VHDL compiler passes an init value through a syn_init property to the mapper, and the mapper then propagates the value to the respective register. Compiler requirements are based on specific data types. These requirements can be broadly grouped based on the different data types available in the VHDL language.

For details about syntax and coding examples, see the online help or reference.pdf->VHDL Language Support->VHDL Implicit Data-type Defaults.

The orig_inst_of Property for Parameterized Modules

The compiler uniquifies parameterized modules or instances and the inst_of property can be used to find the RTL name of the uniquified module/instance. Use the new orig_inst_of property to find the original module/instance name before it was uniquified.

For more information, see the online help or user_guide.pdf->Analyzing with HDL Analyst and FSM Viewer->Working in the Schematic Views->Viewing Object Properties.

VHDL 2008 Enhancements for Bit-string Literals

Bit-string literal support in VHDL 2008 includes:

- Support for characters other than 0 and 1 in the bit string, such as X or Z.
- Optional support for a length specifier that determines the length of the string to be assigned.
- Optional support for a signed (S) or unsigned (U) qualifier that determines how the bit-string value is expanded/truncated when a length specifier is used.
- Additional support for a base specifier for decimal numbers (D). The number of characters in the bit string can be determined by using the expression $(\log_2 n)+1$; where n is the decimal integer.

For more information, see the online help or reference.pdf->VHDL 2008 Language Support ->Operators->Bit-String Literals.

Platforms and Patches

This section includes platform support and other platform-specific information.

Platform Support

The software is supported on the following platforms and operating systems:

- Windows (x86_x64):
  - 7 Professional or Enterprise (32/64-bit)
  - Vista Enterprise or Business (32/64-bit)
  - XP Professional (32/64-bit)
- Linux (x86_x64):
  - Red Hat Enterprise Linux 4/5/6 (32/64-bit)

Required Operating System Patches

Running this software requires that the Linux operating system include specific patches. To determine whether your operating system requires patches, refer to the following procedure.

Checking the Installed Patches

All Linux-based FPGA synthesis applications include a script (syn_system_check) that is designed to check patches that have been installed and the patches that need to be installed or updated.

To use this script:

1. Install the product software.
2. Run the script by entering the following command in a shell:

   /*install_dir*/*product_version*/bin/syn_system_check

3. The script runs and generates a system check summary report that lists the patches and patch status (OK, Install, or Upgrade).
4. Consult the display and install or update any of the patches indicated.

Example

The following is a sample report.

```
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     Synplicity system check summary report for host 'synsun2'

 1.  /home/syn/user available size == 13728736 KB          [ OK ]
 2.  /tmp available size == 243192 KB                      [ OK ]
 3.  /var/tmp available size == 22069 KB                   [ OK ]
 4.  Current DISPLAY is set to 'user:0'                    [ Check user ]
 5.  Required Patch '106950-13'                            [ Install Patch ]
 6.  Upgrade from '106146-14'  to  '106146-31' Required    [ Upgrade Patch ]
 7.  Upgrade from '106327-08'  to  '106327-13' Required    [ Upgrade Patch ]
 8.  Upgrade from '106541-07'  to  '106541-19' Required    [ Upgrade Patch ]
 9.  Upgrade from '108376-12'  to  '108376-34' Required    [ Upgrade Patch ]
10.  sparc architecture                                    [ OK ]
11.  synsun2 solaris 5.7                                   [ OK ]


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Explanation of Operating system patches, following patches are
available at vendor's ftp site

[ 106146-31 ]   SunOS 5.7: M64 Graphics Patch
[ 106327-13 ]   32-Bit Shared library patch for C++
[ 106541-19 ]   SunOS 5.7: Kernel update patch
[ 106950-13 ]   SunOS 5.7: Linker Patch ( required by 106327-13 )
[ 108376-34 ]   OpenWindows 3.6.1: Xsun Patch

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```

Documentation

This section includes the following documentation topics:

- Accessing PDF Documents
- Accessing Online Help

The Synopsys FPGA Synthesis product documentation set consists of the following:

Document	Format	Access
Online Help	HTML Help	See *Accessing Online Help* on page 10.
Document Type • User Guide • Reference Manual • Release Notes	PDF and HTML help	See *Accessing PDF Documents* on page 9.
• Error Messages	HTML Help	Select Help->Error Messages. Click on the error message in the log file or the Message Viewer window.

Accessing PDF Documents

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online.

To access PDF documents either from the software or without running the software, see the table below for details.

Synopsys FPGA Products

From Linux	From outside the software, select: • Open Acrobat Reader: `acroread` Open *`install_directory`*`/documents/`*`docfile`*
From Windows	• Start->Programs->Synopsys->Synplify Pro for Microsemi Edition G-2012.09M-SP1->Documents Then, select the desired document. • From inside the software for all platforms, select Help->Online Documents. In the Open dialog box, select the desired document: - `user_guide.pdf` - `reference.pdf` - `release_notes.pdf`

Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Accessing Online Help

Topics include:

- Synopsys FPGA Products
- Displaying Graphics

Synopsys FPGA Products

For the FPGA products, you can access help from within the software or outside of the tool.

Accessing Help from inside the tool	
All platforms	Press F1 or select Help->Help. For context-sensitive help, click F1 in a dialog box.
Accessing Help from outside the tool	
On a Windows machine	Select Start->Programs->Synopsys->Synplify Pro Microsemi Edition G-2012.09M-SP1->Help.
From Linux	Run synplify_pro_help.

Displaying Graphics

In some cases, the online help graphics do not display correctly. This is usually because your Display setting is 256-Color. Reset the display to 16-bit Color, then reopen the online help.

Known Problems and Solutions

The following problems apply to supported features in the Synplify Pro tool.

Manually Copy Compile Point Sub-directories to Identify Implementation

When compile points are included in an existing FPGA implementation and a new Identify implementation is created, the compile-point related data is not copied to the Identify implementation.

Solution: Manually copy the sub-directories in the FPGA implementation to the new Identify implementation directory. In addition to the sub-directories, the top-level constraint file and all of the compile-point constraint files for the related modules must be enabled on the Constraints panel of the Implementation Options.

Up-to-date Checking Limitation for Sourced Tcl Files in the SDC File

When a design is run, the up-to-date checking feature automatically determines if a design needs to be re-synthesized or not. This feature can provide significant runtime improvements especially for team designs.

However, when you modify constraints in a Tcl file sourced within the constraints file (sdc), the software is not aware of these changes and does not force the design to be re-synthesized.

Solution: This will be fixed in a future release.

Handling State Machines in Different Clock Domains

If a state machine defined in the code feeds sequential elements in a different clock domain, using any encoding value other than the "original" can cause metastability. By default, the synthesis tools choose the optimal encoding value based on the number of states in the state machine. This can introduce additional decode logic that may cause metastability when it feeds sequential elements in a different clock domain.

Solution: As a workaround, use syn_encoding = "original" to guide the synthesis tool for these cases.

Verilog Include Paths Missing from VCS Integration

If Verilog include paths have been added to your Project file, these paths are not automatically added to the VCS script.

Solution: You must add the Verilog include paths manually. To do this, use one of the following workarounds:

- From the Run VCS Simulator dialog box, add `+incdir+<include path>` in the Verilog Compile options field.
- Modify the VCS script file, adding the `+incdir+<include path>` to all or any relevant vlogan commands.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis UI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project UI.

Digital Line Detect Error Appears (Windows XP)

When launching the synthesis software, a Digital Line Detect error occasionally appears on a Dell PC running Windows XP.

Solution: Download the latest update from Dell Corporation. See the following URL for more information.

http://support.dell.com/support/downloads/format.aspx?releaseid=r84541&c=us&l=en&s=gen&cs

Alternatively, you can deselect the Digital Line Detect entry in your system configuration. To do this:

1. Select Run from the Start menu.
2. Type `msconfig` in the open field and click OK.

   The System Configuration Utility dialog box appears.
3. Select the Startup tab and scroll down to the Digital Line Detect entry.
4. Deselect the checkbox to disable it.

Invoking Tool can be Slow on Linux With Network Problems

Invoking the synthesis tools might be slow when you are experiencing network problems on Linux platforms, such as when a mounted drive is not accessible.

Solution: Delete the `$HOME/.config/Trolltech.conf` file to avoid caching. This might help to invoke the tool faster.

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