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Identify® Actel EditionTool Set Release Notes

Version F-2012.03M-SP1, June 2012

Publication Version 01

Contents

About This Release

These release notes describe features and enhancements for the F-2012.03M-SP1 release of the Identify Actel Edition tool set.

Release F-2012.03M-SP1 Features and Enhancements

The following features and enhancements have been included in the F-2012.03M-SP1 release:

- Multiplexed Groups
- Bit Masking for Data Compression

Multiplexed Groups

The multiplexed group feature allows instrumented signals to be assigned to different groups that can then viewed in separate Identify debugger runs. This capability greatly reduces the amount of sample memory required to instrument the same number of signals. For more information, see *Multiplexed Groups* in Chapter 7 and *Selecting Multiplexed Instrumentation Sets* in Chapter 8 of the User Guide.

Bit Masking for Data Compression

A masking option has been added to data compression to selectively mask individual bits or buses from being considered as changing values within the sample data. Note that the values for the portion of the waveform corresponding to the masked bits is invalid during the compression interval. This option is only available through the Identify debugger Tcl shell command iice sampler -enablemask 1. For more information, see *Sampled Data Masking* in Chapter 8 of the *User Guide*. Please note that bit masking is not supported with state-machine or always-armed triggering.

Device Support

The F-2012.03M-SP1 release supports the following device families. With this release, device selection is specified solely in the synthesis tool and passed to the Identify instrumentor in the synthesis project file. Specifying a library in the synthesis tool that is not supported in the Identify tool set results in a “device not supported” message when attempting to launch the Identify instrumentor.

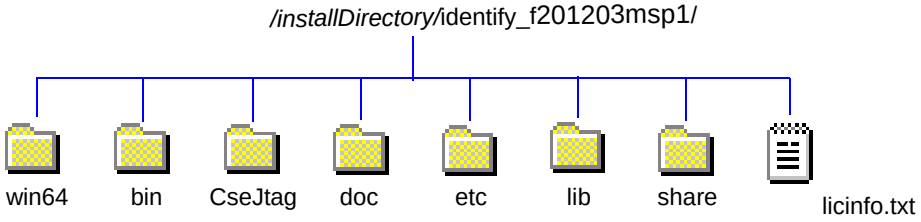
Fusion	IGLOO	IGLOOe
IGLOO PLUS	IGLOO2	ProASIC
ProASIC PLUS	ProASIC3	ProASIC3E
ProASIC3L	SmartFusion	

Installation

The directory where Identify is installed is referred to as the *installDirectory*. The installation subdirectory name consists of the Identify product name and an associated version number, in the current case, Identify_F201203msp1 (for version F-2012.03M-SP1). This naming convention permits multiple versions to be installed in the same product directory. The start menus, desktop icons, and uninstall names have an associated version number, in the current case, Identify F-2012.03M-SP1. For a list of the compatible Windows-based platforms, see *Platform Support* on page 4.

Downloading the Software

The Identify Actel Edition software is normally downloaded from an FTP site and installed directly from the downloaded exe file. Installing the Identify software creates the identify_f201203msp1 subdirectory in the installation directory. This directory contains the following files and subdirectories:



The contents of the files or sub-directories are as follows:

Directory	Contents
bin, win64	Executables for the Identify instrumentor and Identify debugger.
CseJtag	Drivers
doc	User documentation
etc	Location for user-defined startup scripts; template included
lib	Program data files
share	Includes the following subdirectories: • contrib – source directory for scripts executed on startup • vhdl – standard vhdl libraries • synthesis – program specific data files • demo_design – the bus_demo design
licinfo.txt	ASCII version of the Synopsys Software License and Maintenance Agreement for Synplicity Software Products.

Platform Support

The Identify F-2012.03M-SP1 release is compatible with the following Windows (x86/x64) platforms and operating systems:

- Windows 7 Professional or Enterprise (32/64-bit)
- XP Professional (32/64-bit)

Synopsys FPGA Synthesis and Third-Party Tool Compatibility

The F-2012.03M-SP1 release of the Identify Actel Edition software is compatible with the following Synopsys FPGA and third-party tools on the above platforms and operating systems.

Tool	Recommended Version
Synplify Pro (synthesis)	FPGA F-2012.03A-SP1 for ProASIC (500K) and ProASIC PLUS (PA) technologies
	FPGA F-2012.03M-SP1 for other technologies
Actel (place and route)	Libero SoC 10.1

Machine Requirements

Machine memory requirements vary according to the size and complexity of your designs. At a minimum, 1 Gbyte of RAM is required (2 Gbytes are recommended). Your machine's virtual memory (swap space) should be set to at least two times the capacity of the RAM.

Location of the cfg File

The Windows platforms do not permit applications to write to the C:/Windows directory. Because the Identify tools must update the userprefs.cfg initialization file, this file is written to the following directory locations:

On Windows 7 platforms, the software stores the `cfg` file at the following location:

```
C:\Users\userName\AppData\Roaming\Identify
```

On Windows XP platforms, the software stores the `cfg` file at the following location:

```
C:\Documents and Settings\userName\Application Data\Identify
```

Windows Memory Configuration

For all memory configurations, Windows uses a default virtual address space of 4 GBytes; 2 GBytes allocated to user processes (applications) and 2GBytes allocated to the operating system and kernel-mode drivers. On Windows Server 2003 systems and Windows XP Pro systems (with Service Pack 2) that have 1 GByte or more of physical memory, the memory allocation between applications and operating system can be modified to increase the user-process memory allocation to 3 GBytes (and reduce the operating system memory allocation to 1 GByte). For the most up-to-date information for reconfiguring memory allocation on a compatible system, see *How to Set the /3GB Startup Switch in Windows* and related topics on the Microsoft TechNet (http://www.microsoft.com/technet).

Configuring the Windows Firewall for Client Access

Windows XP Service Pack 2 (SP2) and later enhance the security capabilities of the Windows operating system. If you are using a Windows XP machine with an SP2 or later update as your floating license server, you must configure the XP firewall application to allow client access to the floating license ports.

The license manager daemon (lmgrd) and the snpslmd license daemon are separate processes and each requires a separate port to run its associated driver. For floating licenses, you must define a PORT variable for the snpslmd license daemon and then add the ports to the list of exceptions in the firewall application.

Do the following:

1. Open the license file and edit it to define the variable for the snpslmd license daemon by adding a PORT variable to the VENDOR line.

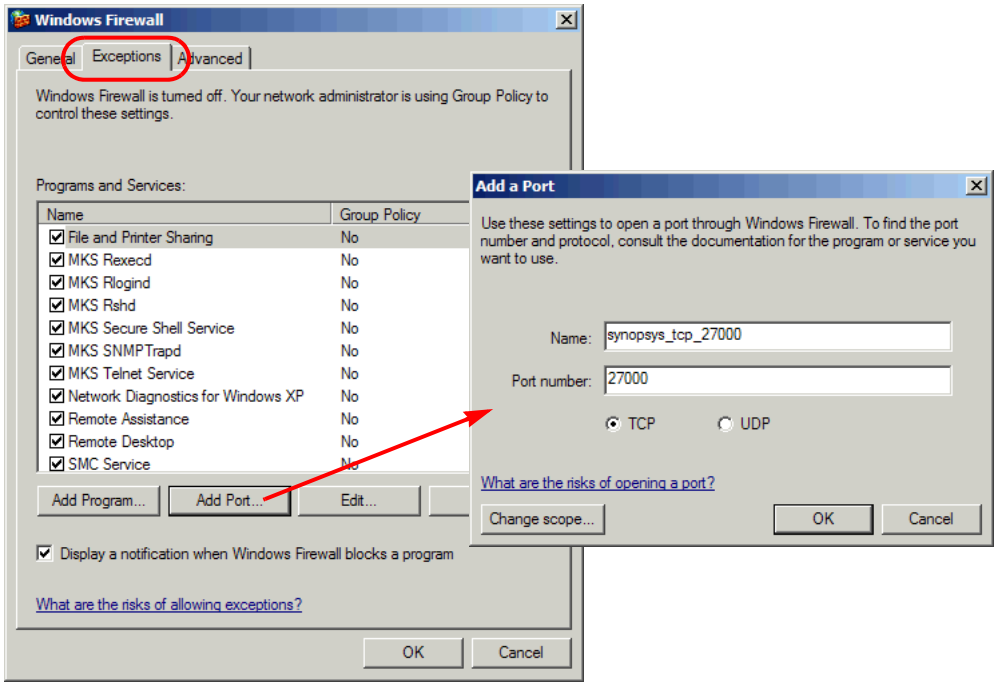
   The following is an example:

   ```
   SERVER <server_name> FLEXID=9-089Dxxxx 27000
   VENDOR snpslmd c:\synopsys\scl_11.1\windows\bin\snpslmd.exe PORT=27001
   INCREMENT synplifypro snpslmd 2010.12 31-dec-2011 1 \
   ...
   ```

   Next, you must add the port values to the Exceptions list in the Windows Firewall application.

2. From the Control Panel, open the Windows Firewall application.

3. Click the Exceptions tab, and then click the Add Port button to display the Add a Port dialog box.



4. Add the TCP port for the license manager daemon by doing the following in the Add a Port dialog box:
   - In the Name field, specify a name for the TCP port. For example, synopsys_tcp_27000.
   - In the Port number field, enter the assigned TCP port value from the license file. Using the sample license file as an example, enter 27000.
   - Click OK in the Add a Port dialog box to accept the entry and close the dialog box.
5. Specify the port for the snpslmd license daemon as follows:
   - Click the Add Port button to redisplay the Add a Port dialog box, and then set the following options.
   - In the Name field, specify a name for the snpslmd license daemon port. For example, synopsys_port_27001.
   - In the Port number field, enter the assigned PORT value from the license file. Using the sample license file as an example, enter 27001.
   - Click OK in the Add a Port dialog box to accept the entry and close the dialog box.
6. Verify that the port names you assigned are included in the Programs and Services list of the Exceptions pane.
7. Click OK in the Windows Firewall dialog box to exit the Windows Firewall application.

Identify Documentation

The following documentation is included with the F-2012.03M-SP1 release of the Identify tool set:

- Identify Actel Edition User Guide
- Identify Actel Edition Reference Manual
- Identify Actel Edition Tutorial
- Identify Actel Edition Quick Start Guide
- Synopsys Software License and Maintenance Agreement

Accessing Documents using the Acrobat Reader

PDF documents display in Adobe Acrobat Reader. You can download the latest Acrobat Reader at no cost from Adobe's website (www.adobe.com). The PDF files provided are optimized for output to a laser printer, not for viewing online. From within the software, you can open the PDF documents by selecting Help->Online Documents and selecting the appropriate PDF. You can also access PDF documents without running the software by selecting Start->Programs->Synopsys->Identify F-2012.03M-SP1->Documents and then selecting the desired PDF document

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Note: Do not use the View->Full Screen option when viewing documents in Acrobat Reader unless you are sure you want this full magnification. On some applications, this selection takes over the monitor and there is no apparent way to access other running tasks or windows. If you do happen to use the Full Screen option, you can use Ctrl-l to undo it.

Resolved Issues

The following issues have been resolved by the Identify F-2012.03M-SP1 release:

Resolved Issue: When IEEE P1735 encryption was used in the design, the compiler generated an incorrect database file for Identify. This file resulted in a database assertion error within the Identify instrumentor which prevented the non-encrypted portion of the design from being instrumented (STAR 9000524946).

Resolved Issue: In a purely VHDL design, a Verilog version of the syn.dics file was automatically created which effectively made the implementation a mixed-language design (VHDL design files plus Verilog syn.dics file). As a result, the compiler did not automatically reorder the VHDL design files which caused some designs to fail when the file order was not correct in the project and the top-level module was not defined (STAR 9000486136).

Resolved Issue: Attempting to use Arrange VHDL Files to re-arrange the order of VHDL files in a project was not effective in changing the file order (STAR 9000486138).

Resolved Issue: When using data compression with bit masking, an assertion error was reported when attempting to mask the most-significant bit for a specific signal (STAR 9000526275).

Resolved Issue: When invoking the Identify Instrumentor from the command line, including the location and type of synthesis tool command line arguments opened the Identify Instrumentor in the GUI mode, but did not allow the project to be opened from the Open Project button (STAR 9000451295).

Resolved Issue: Use of the SystemVerilog setting in Synplify caused a compile error in Identify (STAR 9000426257).

Resolved Issue: Previously, when the UI called the compiler for an Identify implementation, the UI called c_ver for both Verilog and VHDL designs and did not call c_hdl. As Verilog designs using DesignWare require the VHDL compiler, a compiler error occurred without the call to c_hdl (STAR 9000520393).

Important Issues and Workarounds

The following issues have been identified with the Identify F-2012.03M-SP1 release:

Problem: When using data compression with always-armed triggering enabled, both the trigger position and the captured sample prior to the trigger are incorrect for the internal_memory (BRAM) buffer type setting (STAR 9000526277).

Workaround: This problem is scheduled to be addressed in a future release.

Problem: When using data compression with cross-triggering enabled, the trigger position is incorrect for the internal_memory (BRAM) buffer type setting (STAR 9000526349).

Workaround: This problem is scheduled to be addressed in a future release.

Problem: If a Synplify project is loaded using a UNC (network) path, the Identify instrumentor errors out with the message "*Could not open IDC file identify.idc for writing*" when attempting to save the instrumentation (STAR 9000546221).

Workaround: Map the UNC path to a Windows drive and load the project from the Windows drive.

Problem: When compile points are included in an existing FPGA implementation and a new Identify implementation is created, the compile-point related data is not copied to the Identify implementation (STAR 9000487229).

Workaround: Manually copy the sub-directories in the FPGA implementation to the new Identify implementation directory. In addition to the sub-directories, the top-level constraint file and all of the compile-point constraint files for the related modules must be enabled on the Constraints panel of the Implementation Options.

Problem: When using VHDL, if the trigger signal (scalar) is of type std_logic, the value must be enclosed in single quotes in both the UI and the shell as shown in the following command (STAR 9000483412):

```
watch enable -iice IICE -condition 0 /my_signal {'0'}
```

Problem: Entering a scalar signal without quotes or in double quotes results in an error. Conversely, vectors must be entered without quotes as shown in the following command:

```
watch enable -iice IICE -condition 0 /my_bus {1010}
```

Workaround: Make sure that all scalars are enclosed in single quotes and that vectors are entered without quotes.

Problem: The message suppression feature available with the synthesis tools cannot be used to suppress (or change the severity of) messages generated by Identify (STAR 9000484518).

Workaround: Be sure to disable message suppression when using an Identify implementation.

Problem: If an implementation includes an edf black-box module, the Identify instrumentor errors out complaining about an undefined module (STAR 9000315931).

Workaround: Replace the edf black box with some RTL or a functional edf module.

Problem: Use of external triggers via the import trigger mechanism causes an excessive use of internal block RAM due to sampling of the trigger as well as the creation of a look-up table. The problem is most notable when the maximum of eight imported triggers is selected. A better mechanism to import triggers that uses fewer resources will be available in a future release (STAR 9000462154).

Workaround: Add an extra input to the top-level RTL code and instrument the input as a trigger only.

Problem: Cross-triggering can cause Identify Debugger to crash if a trigger condition is not set for each IICE (STAR 9000359582).

Workaround: Set a trigger for each IICE (even a dummy trigger).

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