PCN Number: 0907

PCN Change Level: Major

PCN Date: June 29, 2009

Subject: Changes to Datasheet Specification for Military Temperature and MIL-STD-883 Class B ProASIC^{PLUS}® FPGAs

Dear Customer,

This notification provides notice that Actel will make changes to the datasheet specifications for the military temperature and MIL-STD-883 Class B ProASIC^{PLUS} FPGAs (http://www.actel.com/documents/ProASICPlus_DS.pdf). Changes will be made in three separate areas, explained below, in order to improve test yield and product availability. No products other than the military temperature and MIL-STD-883 Class B versions of ProASIC^{PLUS} are affected at this time. A full list of the affected part numbers is provided in Appendix A. Actel will begin shipping product in compliance with the revised datasheet specifications no earlier than 90 days after the date on this PCN.

1. 3.3 V I/O V_{OH} and V_{OL} specification changes

Actel is making changes to the 3.3 V V_{OH} and V_{OL} specifications. Specifically, changes have been made to the drive currents at which 3.3 V V_{OH} and V_{OL} voltage levels are measured and are now split by slew rate. The old and new specifications are listed below.

Old specification, from ProASIC^{PLUS} datasheet v5.7:

Table 1-22 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V)**

Symbol	Parameter	Conditions	Commercial/Industrial/ Military/MIL-STD-883 [1, 2]			Units
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OH} = –14 mA I_{OH} = –24 mA I_{OH} = –6 mA I_{OH} = –12 mA	 0.9*V_{DDP} 2.4 0.9*V_{DDP} 2.4			V
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive (OB33P) 3.3 V I/O, Low Drive (OB33L)	 I_{OL} = 15 mA I_{OL} = 20 mA I_{OL} = 28 mA I_{OL} = 7 mA I_{OL} = 10 mA I_{OL} = 15 mA			 0.1V_{DDP} 0.4 0.7 0.1V_{DDP} 0.4 0.7	V

Actel Corporation
2061 Stierlin Court, Mountain View, CA 94043
Phone: 650.318.4200 Fax 650.318.4600

New specification, from ProASIC^{PLUS} datasheet v5.8:

Table 1-24 • **DC Electrical Specifications (V_{DDP} = 3.3 V ±0.3 V and V_{DD} = 2.5 V ±0.2 V) Applies to Military Temperature and MIL-STD-883B Temperature Only**

Symbol	Parameter	Conditions	Military/MIL-STD-883B[1] Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage 3.3 V I/O, High Drive, High Slew (OB33PH)	I_{OH} = –8 mA I_{OH} = –16 mA	0.9*V_{DDP} 2.4			V
	3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL)	I_{OH} = –3mA I_{OH} = –8mA	0.9*V_{DDP} 2.4			
	3.3 V I/O, Low Drive , High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	I_{OH} = –3 mA I_{OH} = –8 mA	0.9*V_{DDP} 2.4			
V_{OL}	Output Low Voltage 3.3 V I/O, High Drive, High Slew (OB33PH)	I_{OL} – 12 mA I_{OL} = 17 mA I_{OL} = 28 mA			0.1V_{DDP} 0.4 0.7	V
	3.3V I/O, High Drive, Normal/ Low Slew (OB33PN/OB33PL))	I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA			0.1V_{DDP} 0.4 0.7	
	3.3 V I/O, Low Drive, High/ Normal/Low Slew (OB33LH/ OB33LN/OB33LL)	I_{OL} = 4 mA I_{OL} = 6 mA I_{OL} = 13 mA			0.1V_{DDP} 0.4 0.7	

2. Phase-Locked Loop (PLL) specification changes

Actel is making changes to the PLL specifications. Changes are being made to the Input, VCO (Voltage Controlled Oscillator), and Output frequencies, and the acquisition time.

The old and new specifications are listed below.

Old specification, from ProASIC^{PLUS} datasheet v5.7, page 1-21:

Parameter	Value			Notes
Frequency Ranges				
Reference Frequency f_{IN} (min.)	1.5 MHz			Clock conditioning circuitry (min.) lowest input frequency
Reference Frequency f_{IN} (max.)	180 MHz			Clock conditioning circuitry (max.) highest input frequency
OSC Frequency f_{VCO} (min.)	24 MHz			Lowest output frequency voltage controlled oscillator
OSC Frequency f_{VCO} (max.)	180 MHz			Highest output frequency voltage controlled oscillator
Clock Conditioning Circuitry f_{OUT} (min.)	6 MHz			Lowest output frequency clock conditioning circuitry
Clock Conditioning Circuitry f_{OUT} (max.)	180 MHz			Highest output frequency clock conditioning circuitry
Long Term Jitter Peak-to-Peak Max.*				
Temperature	**Frequency MHz**			
	f_{VCO}<10	**10<f_{VCO}<60**	**f_{VCO}>60**	
25°C (or higher)	±1%	±2%	±1%	Jitter(ps) = Jitter(%)*period For example: Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps
0°C	±1.5%	±2.5%	±1%	
–40°C	±2.5%	±3.5%	±1%	
–55°C	±2.5%	±3.5%	±1%	
Acquisition Time from Cold Start				
Acquisition Time (max.)	30 µs			$f_{VCO} \leq 40$ MHz
Acquisition Time (max.)	80 µs			$f_{VCO} > 40$ MHz
Power Consumption				
Analog Supply Power (max.*)	6.9 mW per PLL			
Digital Supply Current (max.)	7 µW/MHz			
Duty Cycle	50% ±0.5%			
Input Jitter Tolerance	5% input period (max. 5 ns)			Maximum jitter allowable on an input clock to acquire and maintain lock.

*Note: *High clock frequencies (>60 MHz) under typical setup conditions*

Actel Corporation
2061 Stierlin Court, Mountain View, CA 94043
Phone: 650.318.4200 Fax 650.318.4600

New specification, from ProASIC^{PLUS} datasheet v5.8, page 1-21:

Parameter	Value $T_J \leq -40°C$	Value $T_J > -40°C$	Notes
Frequency Ranges			
Reference Frequency f_{IN} (min.)	2.0 MHz	1.5 MHz	Clock conditioning circuitry (min.) lowest input frequency
Reference Frequency f_{IN} (max.)	180 MHz	180 MHz	Clock conditioning circuitry (max.) highest input frequency
OSC Frequency f_{VCO} (min.)	60	24 MHz	Lowest output frequency voltage controlled oscillator
OSC Frequency f_{VCO} (max.)	180	180 MHz	Highest output frequency voltage controlled oscillator
Clock Conditioning Circuitry f_{OUT} (min.)	$f_{IN} \leq 40$ = 18 MHz $f_{IN} > 40$ = 16 MHz	6 MHz	Lowest output frequency clock conditioning circuitry
Clock Conditioning Circuitry f_{OUT} (max.)	180	180 MHz	Highest output frequency clock conditioning circuitry
Acquisition Time from Cold Start			
Acquisition Time (max.)	80 µs	30 µs	$f_{VCO} \leq 40$ MHz
Acquisition Time (max.)	80 µs	80 µs	$f_{VCO} > 40$ MHz
Long Term Jitter Peak-to-Peak Max.*			
Temperature		**Frequency MHz**	
		f_{VCO}< 10 / 10<f_{VCO}<60 / f_{VCO} >60	
25°C (or higher)		±1% ±2% ±1%	Jitter(ps) = Jitter(%)*period For example: Jitter in picoseconds at 100 MHz = 0.01 * (1/100E6) = 100 ps
0°C		±1.5% ±2.5% ±1%	
–40°C		±2.5% ±3.5% ±1%	
–55°C		±2.5% ±3.5% ±1%	
Power Consumption			
Analog Supply Power (max.*)		6.9 mW per PLL	
Digital Supply Current (max.)		7 µW/MHz	
Duty Cycle		50% ±0.5%	
Input Jitter Tolerance		5% input period (max. 5 ns)	Maximum jitter allowable on an input clock to acquire and maintain lock.

Note: **High clock frequencies (>60 MHz) under typical setup conditions*

Actel Corporation
2061 Stierlin Court, Mountain View, CA 94043
Phone: 650.318.4200 Fax 650.318.4600

In addition, in the ProASIC^{PLUS} datasheet v5.8, the following constraints have been added to the PLL locking condition:

Table 1-10 • **PLL I/O Constraints**

	$T_J \leq -40°C$		Value $T_J > -40°C$
I/O Type	PLL locking is guaranteed only when using low drive strength and low slew rate I/O. PLL locking may be inconsistent when using high drive strength or high slew rate I/Os		No Constraints
SSO	APA300	Hermetic packages ≤ 8 SSO	With FIN ≤ 180 MHz and outputs switching simultaneously
		Plastic packages ≤ 16 SSO	
	APA600	Hermetic packages ≤ 16 SSO	
		Plastic packages ≤ 32 SSO	
	APA1000	Hermetic packages ≤ 16 SSO	
		Plastic packages ≤ 32 SSO	
	APA300	Hermetic packages ≤ 12 SSO	With FIN ≤ 50 MHz and half outputs switching on positive clock edge, half switching on the negative clock edge no less than 10nsec later
		Plastic packages ≤ 20 SSO	
	APA600	Hermetic packages ≤ 32 SSO	
		Plastic packages ≤ 64 SSO	
	APA1000	Hermetic packages ≤ 32 SSO	
		Plastic packages ≤ 64 SSO	

3. Schmitt-trigger specification changes

Actel is making changes to the 3.3 V V_{IL} specifications for Schmitt-trigger inputs. Specifically, the maximum V_{IL} specification has changed from 0.8 V to 0.7 V for 3.3 V Schmitt-trigger input operation. The old and new specifications are listed below.

Old specification, from ProASIC^{PLUS} datasheet v5.7, table 1-22:

V_{IL}[7]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode		 –0.3 –0.3 –0.3		 0.8 0.8 0.7	 V

New specification, from ProASIC^{PLUS} datasheet v5.8, table 1-24:

V_{IL}[5]	Input Low Voltage 3.3 V Schmitt Trigger Inputs 3.3 V LVTTL/LVCMOS 2.5 V Mode		 –0.3 –0.3 –0.3		 0.7 0.8 0.7	 V

Actel will ship product screened in compliance with the specifications stated in v5.8 of the datasheet, starting no earlier than 90 days following the date of this PCN. Customers who require product sooner than this and who can accept material screened to the v5.8 specifications are requested to sign a separate acknowledgement and return it to their Actel Sales Manager in order to expedite the scheduling and shipment of their backlog.

If you have any questions, please contact Actel's Application Technical Support at tech@actel.com.

Regards,

Actel Corporation

Actel Corporation
2061 Stierlin Court, Mountain View, CA 94043
Phone: 650.318.4200 Fax 650.318.4600

Appendix A

List of Affected Devices

APA300-FG144M	APA600-CQ208B
APA300-FGG256M	APA1000-BG456M
APA300-CQ208M	APA1000-FGG896M
APA300-CQ352B	APA1000-CGS624M
APA600-FG256M	APA1000-LG624B
APA600-PQG208M	APA1000-CQ352M
APA600-CQ208M	APA300-BGG456M
APA600-CQ352B	APA300-FG256M
APA1000-FG896M	APA300-PQG208M
APA1000-PQG208M	APA300-CQ352M
APA1000-LG624M	APA600-BGG456M
APA1000-CQ208B	APA600-PQ208M
APA300-BG456M	APA600-CGS624B
APA300-FGG144M	APA600-CQ352M
APA300-PQ208M	APA1000-BGG456M
APA300-CQ208B	APA1000-PQ208M
APA600-BG456M	APA1000-CGS624B
APA600-FGG256M	APA1000-CQ208M
APA600-CGS624M	APA1000-CQ352B