August 28, 2007

PCN Number: 0714

PCN Change Level: Major

Subject: FSM Bug – Synplify® 8.6.2H in Libero® IDE 7.3, 7.3 SP1, and 7.3 SP2

Dear Customer,

This notification provides information regarding a finite state machine (FSM) bug in the Synplify 8.6.2H synthesis software. This software is developed by Synplicity and is offered by Actel to our customers as a bundled product in the Libero IDE software suite. The Synplify 8.6.2H version shipped by Actel is based upon the Synplify 8.8 version on general release by Synplicity. Actel has worked closely with Synplicity to evaluate alternatives and advise our customers of the best course of action. This notice does not apply to versions other than Libero IDE v7.3.

The description of the problem is as follows:

- There is a bug in the FSM Compiler in the Synplify 8.6.2H synthesis software. This bug can result in missing states.
- This bug was introduced in the Synplify 8.8 general release software and fixed in version 8.8.0.4.
- While it was not immediately recognized, this problem was also introduced in the Actel Edition Synplify 8.6.2H that shipped in Actel's Libero IDE v7.3 software suite, which first shipped in January 2007. Libero IDE 7.3 SP1 and SP2 also utilize Synplify 8.6.2H.
- All Actel devices are affected.
- The fault applies only to a subset of FSMs generated by the FSM Compiler and FSM Explorer in Synplify 8.6.2H. FSMs generated by hand or by software other than version 8.6.2H, 8.8, or 8.8.0.2 of Synplify are not affected. The fault condition, if present, will appear in the netlist produced by Synplify. Post-synthesis simulation of all state machines in the design will detect the fault, if it is present. In the fault condition, the defective state machine will be non-functional and will not simulate correctly.

Corrective actions taken to resolve the problem are described below:

- The bug is fixed in Synplify 8.8A1, which is included in Actel's Libero IDE v8.0 software. Download this software version from the Actel website at http://www.actel.com/download/software/libero/.
- New and changed optimizations have been added in Synplify 8.8A1.
- An intensive code review of all related functions was conducted to ensure that this problem is resolved. New test cases have been added to the test suite.

Actel Corporation
2061 Stierlin Court, Mountain View, CA 94043
Phone: 650.318.4200 Fax 650.318.4600

Actel recommends that customers do the following:

- All Synplify 8.6.2H users should immediately upgrade to Libero IDE v8.0 and Synplify 8.8A1. Download Libero IDE v8.0 from http://www.actel.com/download/software/libero/.
  Due to a bug in the CLKINT timing model in Synplify 8.8A1, Axcelerator and RTAX-S users should upgrade to Synplify 8.8A2, which can be downloaded from http://www.actel.com/download/software/synplify/.
- Customers who have not used FSM Explorer or FSM Compiler in Synplify 8.6.2H are not exposed to this fault. However, Actel always recommends using the latest version of software, and therefore, we recommend that customers upgrade to Libero IDE 8.0.
- FSM faults may be detected by reviewing the .srr file that is generated by Synplify. This file shows all FSMs compiled by FSM Compiler or FSM Explorer, and lists the encoding for all the state machines in a design along with associated notes and warnings. Users should check the list for consistency against their HDL design description and check for any unexpected warnings. Examples of warnings that should be investigated by the user are as follows:
  – Warning: Removing sequential instance <instance name or state name>[bit] of view:PrimLib.dffr(prim) because it is equivalent to instance <instance name or state name>[bit]
  – Warning: Removing sequential instance <instance name or state name>[bit] of view:PrimLib.dffr(prim) because there are no references to its outputs
  – @W:MO129 :"d:\data\designs\test\hdl\test_master.vhd":291:3:2 91:20|Sequential instance master.test_presstate[0] has been reduced to a combinational gate by constant propagation
- If FSM Explorer or FSM Compiler in Synplify 8.6.2H have been used to develop a design, customers are advised to ensure that all FSMs are adequately simulated. If the fault condition exists, it will be immediately obvious from the post-synthesis simulation results and will appear as a non-functional state machine (the FSM will not advance between states, or FSM signals will be missing). If these error conditions are observed, the design should be resynthesized and recompiled using Synplify 8.8A1 and Libero IDE v8.0. If it is not possible to upgrade to Libero IDE v8.0, turn off FSM Explorer and FSM Compiler, resynthesize using Synplify 8.6.2H, and recompile using Libero IDE v7.3.
- If devices have already been programmed with designs compiled using Libero IDE v7.3, customers should ensure that parts have had adequate functional testing, with special emphasis on correct operation of finite state machines.
- If programmed parts are found to contain a non-functional or faulty state machine, and it is not possible to reprogram these parts, please contact your local Actel sales office.
- Users should note that some Synplify optimizations have been enhanced in 8.8A1 from versions prior to 8.6.2H, so netlists may differ. In some cases, FSM registers may be legitimately optimized away because bits are unused. If the user wants to preserve those bits, setting design attributes may satisfy that requirement.

If you have any questions, please contact Actel's Application Technical Support at tech@actel.com.

Regards,

Actel Corporation

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