January 12, 2007

PCN Number: 0625

PCN Change Level: Minor

Subject: Routed Clock Timing on Axcelerator® and RTAX-S

Dear Customer,

Under certain, very rare circumstances, the SmartTime tool in Actel's Designer and Libero® Integrated Design Environment (IDE) software can slightly underestimate the clock delay when using the routed clock on Axcelerator and RTAX-S devices. This PCN discusses the issue and describes the solution. Note that this issue applies only to the routed clock (CLK); the hardwired clock (HCLK) is not affected.

Background

In the AX and RTAX-S architecture, each device is comprised of core tiles. For example, an AX2000 or RTAX2000S device includes 16 core tiles in a 4x4 array. Each core tile is served by four routed clock segments, which run along the middle of the core tile. Logic modules, I/O cells, and SRAM cells are served by ribs branching off the central routed clock segments. Each of these ribs is called a routed clock half-tile row (HTR). See Figure 1 for more information.

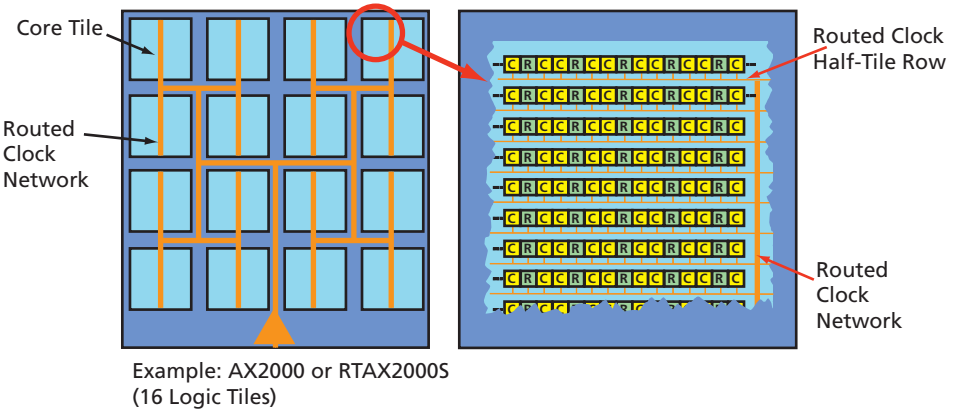

Figure 1 • Figure 1: AX Routed Clock Half-Tile Row (HTR) Architecture

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Issue

The maximum number of loads that any HTR can serve is 44. The loads are separated into the following groups:

- 12 R-cells
- 24 C-cells
- 2 SRAM cell loads
- 6 I/O registers (2 I/O cells with 3 registers each)

In order to exceed 16 loads, the HTR must be connected to loads other than just R-cells. In almost all designs, the number of loads applied to each HTR is less than 16. The SmartTime timer provides an accurate assessment of CLK delay if the load on each HTR is 16 or less. However, if the load applied to an HTR exceeds 16, then the CLK delay will be slightly underestimated by the SmartTime tool. The degree to which SmartTime underestimates the CLK delay is dependent on operating temperature, device speed grade, and the actual number of loads on the HTR, but it is not worse than 1.1 ns. Table 1 lists the data. Actel has observed only one customer design where an HTR exceeded 16 loads. This design was targeted to a commercial Axcelerator FPGA.

Table 1 • Additional Routed Clock Insertion Delay

Temperature	Increase in Clock Insertion Delay (ps)		
	17 to 24 Loads	25 to 36 Loads	More than 36 Loads
Standard Speed Grade			
–55°C	526	671	768
25°C	612	780	892
125°C	740	944	1,079
–1 Speed Grade			
–55°C	447	571	653
25°C	521	663	759
125°C	640	803	919
–2 Speed Grade			
–55°C	393	501	573
25°C	457	582	666
125°C	553	705	807

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Solution

Actel has made changes to the timing models in the SmartTime tool and has also made changes in how Axcelerator and RTAX-S designs are compiled. These changes eliminate the problem, and were introduced in Designer v7.2 SP1. New designs and existing designs are handled differently and are described in the following sections.

New Designs

Designer v7.2 SP1 will limit the fanout of the CLK network to a maximum of 16 loads per HTR, when at least 1 R-cell clock pin is connected to the HTR. If no R-cell clock pin is connected to the HTR, then the fanout limit will not be applied. The software will assume that the loads are purely combinatorial and are not sensitive to clock skew on the routed clock.

Pre-Existing Designs

When Designer v7.2 SP1 or later encounters a design created with a previous version of Designer software, and if the design has an HTR load greater than 16, it will print a warning in the log file, stating that the HTR loading maximum has been exceeded. The timing of the HTR with loading greater than 16 will be amended to reflect the updated timing models in v7.2 SP1, in accordance with table 1 in this document. Designer v7.2 SP1 will not make any place-and-route changes to eliminate any HTR loads greater than 16.

Recommendations

The likelihood of customer designs having HTR loads greater than 16 is very small. However, Actel recommends that customers upgrade their Designer software to the latest version and recompile their Axcelerator or RTAX-S designs in order to be certain that no HTR loading violations exist. If an HTR loading violation is found to exist, customers are requested to contact their Actel FAE for further guidance.

For questions, please contact Actel's Application Technical Support at tech@actel.com.

Regards,

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