June 13, 2006

PCN Number: 0609

PCN Change Level: Minor

Subject: RAM Simulation Model for Axcelerator® and RTAX-S FPGAs and Error Detection and Correction (EDAC) Core Design Modifications

Dear Customer,

The purpose of this letter is to provide you with information regarding embedded user static RAM (SRAM) in the RTAX-S and Axcelerator families of devices. When using the Error Detection and Correction (EDAC) core in SmartGen v7.1 and prior versions with certain applications, it was discovered that the simulation library model may produce incorrect results when simultaneous reads and writes occur to a single address. This can occur when the internal scrubber logic is performing a read or write (correcting an error) while the external logic is accessing the memory. The data that is read during this operation may be indeterminate due to the timing of the read/write cycle. The original RAM simulation model for this condition was incorrect.

This issue is being addressed in a revision of the Axcelerator and RTAX-S embedded user static RAM simulation model and the EDAC core, which will be available in SmartGen v7.2. The new version of the EDAC core verifies that neither reads nor writes are in progress before performing a scrub or write back of corrected data. This guarantees that an external read / internal (scrubber) write or external write / internal read cannot occur. However, it is still possible to perform a simultaneous external read and write, which is described below.

The changes to the EDAC core available in SmartGen v7.2 are as follows:

- The EDAC core will have logic added to ensure that internal reads and writes are not performed simultaneously with external reads and writes.
- Additional changes are being implemented in the independently clocked EDAC. You must control the operation of the scrubber by enabling and disabling scrubbing. When the scrubber is on, access to external memory is not supported; in the independently clocked EDAC implementation, scrubbing will not occur while user memory accesses are taking place. You must assert STOP_SCRUB and wait for two RCLK or two WCLK cycles before performing a read or write access. You may restart scrubbing by deasserting STOP_SCRUB. Since the scrub address register will not be reset when the scrubber is stopped, the scrubber will continue scrubbing from the retained address. Please note that the independently clocked EDAC behavior with respect to address retention is different from that of the single clock EDAC. The scrub address can be reset to zero by asserting BYPASS while STOP_SCRUB is active. Using BYPASS this way requires two clock cycles to become effective. Please refer to the application note *Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs* for additional information. The updated version of the application note will be available in July.

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- The simulation library model will be updated to accurately reflect the behavior of the silicon.
- The testbenches will be updated to allow verification of the core modifications.
- Timing diagrams will be added to the *Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs* application note. This document will also contain example code that will describe the implementation of a warning flag that detects simultaneous reads/writes to a single address. You may want to consider including this function in your design. Because of port compatibility with the current version of the core, this function was not added to the baseline version of the core in SmartGen v7.2.
- The EDAC core modifications will have a negligible impact to gate count and timing.
- The new EDAC core, simulation library model, and testbenches will all be available in SmartGen v7.2.
- The Axcelerator and RTAX-S datasheets will be updated to reflect the actual operation of the embedded user memory.

Recommendations:

- All RTAX-S and Axcelerator customers are recommended to simulate their design using the RTAX-S or Axcelerator embedded user static RAM simulation model in the Libero® Integrated Design Environment (IDE) v7.2 release.
- For customers utilizing the Actel EDAC macro in their designs, Actel recommends that you review the updated application note, *Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs*, to determine if you should regenerate the EDAC core using the new version in SmartGen v7.2.

SmartGen v7.2 is targeted to be available in July for direct download from the Actel website as a part of the Libero IDE / Designer v7.2 release. Please contact your regional FAE for assistance.

Regards,

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