SmartGen Hard Multiplier v1.0

Handbook

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

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Trademarks

Table of Contents

Introduction

At the basic level, SgHardMult (SmartGen RTAX-DSP Multiplier) performs a single 18x18 two's complement signed multiplication. You can choose the width of the operands (at pre-synthesis configuration time), whether one of the operands is a constant and whether any of the operands or the result is registered. Implementation is limited to those device families that contain MATH blocks (Axcelerator only at this time).

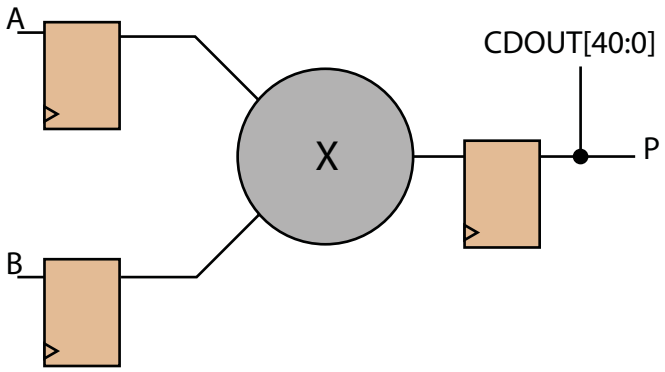

Figure 1 · SgHardMult Block Diagram

The SgHardMult block diagram is shown in Figure 1. Several aspects of SgHardMult can be configured with a user interface that generates a structured netlist in Verilog or VHDL. For a detailed description of the user interface settings, refer to Table 2-2 on page 10.

Key Features

SgHardMult has the following features:

- A structural netlist generator in Verilog or VHDL
- Configurable widths of operands A and B between 2 and 18
- Optional assignment of operand A to a 18 bit two's complement constant
- Optional registers for A, B or P (and CDOUT[40:0]) with a common rising-edge clock, individual active-low asynchronous clear and individual active-high enable signals
- Additional output (for cascading to the next MATH block) CDOUT[40:0], which is a copy of P, sign-extended to 41 bits

Core Version

This handbook applies to SgHardMult v1.0.

Utilization and Performance

SgHardMult can be used with any devices in the RTAX-DSP family. You must create a project with Axcelerator in the Libero IDE to use the SgHardMult macro. A summary of the data for SgHardMult is listed in Table 1.

Table 1 · SgHardMult Device Utilization and Performance

Family	FPGA Resources			Performance
	Sequential	Combinatorial	MATH	
RTAX-DSP	0	0	1	> 143 MHz

Note: Data used in this table was otained using typical synthesis and layout settings under STD Speed Grade and MIL operating conditions.

The benchmarks were obtained using the macro configuration settings shown in Table 2.

Table 2 · SgHardMult Benchmark Options

Configuration Option	Setting
Input Port A	
Use Constant	Unselected
Constant Value	N/A
Width	18
Register Port	Selected
Input Port B	
Width	18
Register Port	Selected
Output Port P	
Register Port	Selected
Target FPGA	
Die	RTAX4000D

1 Functional Block Description

SgHardMult, shown in Figure 1 on page 5, consists of a single MATH18x18 macro configured for two's complement signed multiply operation, shown in the equations below.

P = A x B

CDOUT[40:0] = P

Register Usage

All internal registers are TMR hardened to eliminate radiation-induced single-event upsets (SEU). They have a common rising-edge clock, individual active-low asynchronous clear and individual active-high enable signals. The pinout for internal registers is shown in Figure 1-1.

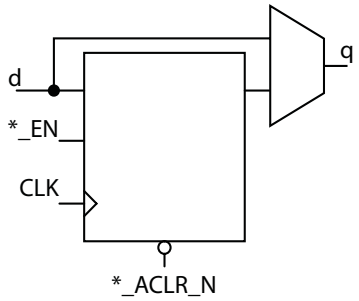

Figure 1-1 · Pinout of Internal Registers

When SgHardMult is configured to use registers for any of the operands, the input and output ports shown in Table 1-1 appear in the generated macro.

Table 1-1 · SgHardMult Register Ports

Register Port	Port Name		
	Rising-Edge Clock	Active-low Asynchronous Clear	Active-high Enable
A	CLK	A_ACLR_N	A_EN
B		B_ACLR_N	B_EN
P (and CDOUT[40:0])		P_ACLR_N	P_EN

2 Interface Description

Ports

Figure 2-1 shows the SgHardMult input and output ports. The ports shown are a superset of all possible ports. Only a subset of the ports are used in any given SgHardMult configuration.

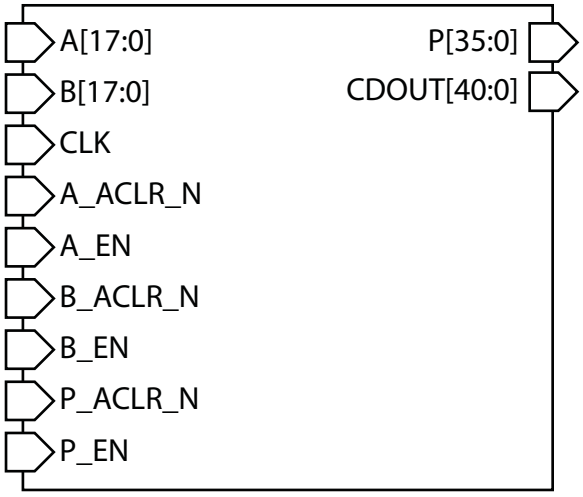

Figure 2-1 · SgHardMult Pinout Diagram

The port signals for the SgHardMult macro are defined in Table 2-1.

Table 2-1 · SgHardMult Ports

Signal	Input/Output	Polarity	Description
A	Input	High	Input data A
B	Input	High	Input data B
CLK	Input	Rising	Input clock for A, B, P and CDOUT[40:0] registers
A_ACLR_N	Input	Low	Asynchronous reset for data A registers
A_EN	Input	High	Enable for data A registers
B_ACLR_N	Input	Low	Asynchronous reset for data B registers
B_EN	Input	High	Enable for data B registers
P_ACLR_N	Input	Low	Asynchronous reset for result P (and CDOUT[40:0]) registers
P_EN	Input	High	Enable for result P (and CDOUT[40:0]) registers
P	Output	High	Result data: P = A x B
CDOUT[40:0]	Output Cascade	High	Cascade output of result P. CDOUT is a copy of P, sign-extended to 41 bits. The entire bus must either be dangling or drive an entire CDIN[40:0] of another MATH block in cascaded mode.

Configuring the SgHardMult Macro

SgHardMult settings for configuring the macro are listed in Table 2-2. You can double-click the SgHardMult macro in the Project Manager Catalog or open and configure the macro in SmartDesign (see "SmartDesign" on page 11).

Table 2-2 · SgHardMult Configuration Descriptions

Name	Valid Range	Description
Input Port A		
Use Constant		Sets input port A to constant
Constant Value (Hex)	-2^{17} to (2^{17} - 1)	Two's complement value of A, if A is constant. Values shorter than 18 bits are padded with zeros. Negative values must be a full 18 bits wide.[1]
Width	2 to 18	Width of input port A (if A is not constant); if shorter than 18 bits it is sign-extended [2]
Register Port		Registers input port A (if A is not constant)
Input Port B		
Width	2 to 18	Width of input port B; if shorter than 18 bits it is sign-extended [2]
Register Port		Registers input port B
Output Port P		
Register Port		Registers output port P (and CDOUT[40:0])
Target FPGA		
Die	RTAX2000D or RTAX4000D	Target device

1. *E.g. 0x1FFFF means +131071 (2^{17} – 1), while 0x3FFFF means –1*
2. *E.g. if the width is 8, a value of 0x7F means +127 and a value of 0xFF means –1*

Tool Flows

Licenses

SgHardMult is included for free in the Libero® IDE Project Manager Catalog and does not require a separate license to instantiate and use in Actel devices. The complete structural netlist is provided for the macro.

SmartDesign

SgHardMult is available for download from the Libero® Integrated Design Environment (IDE) IP Catalog via the web repository. Once it is listed on the catalog, the macro can be instantiated using SmartDesign. To use it, double-click or drag it from the Arithmetic section of the Catalog onto the Canvas. For information on using SmartDesign to configure, connect, and generate cores, see the Libero IDE online help.

Figure 3-1 shows the SgHardMult configuration window. The configuration window displays the configuration options for each input port and output port. After configuring and generating the macro instance, you can simulate basic functionality. The macro can then be instantiated as a component of a larger design.

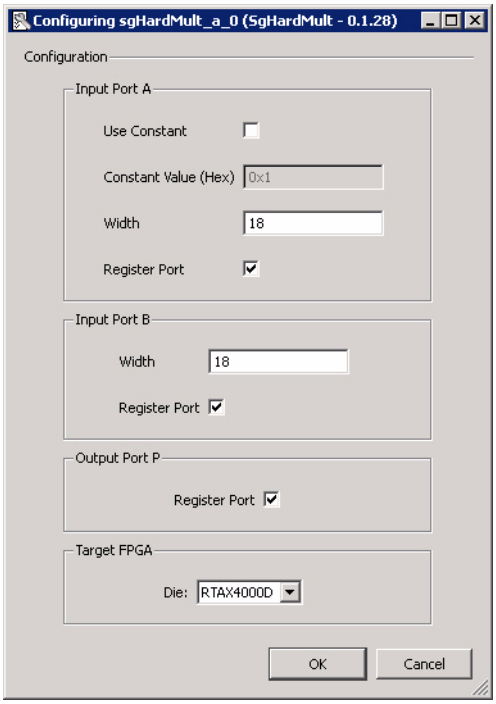

Figure 3-1 · SgHardMult Configuration Window

Place-and-Route in the Libero IDE

After running synthesis on the instantiated design, click the Place&Route button in the Project Manager to open Designer. SgHardMult requires no special place-and-route settings.

A

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From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
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Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

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You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

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Actel Corporation *• 2061 Stierlin Court • Mountain View, CA 94043 • USA*
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Actel Europe Ltd*. • River Court, Meadows Business Park • Station Approach, Blackwater • Camberley Surrey GU17 9AB • United Kingdom*
Phone +44 (0) 1276 609 300 • Fax +44 (0) 1276 607 540

Actel Japan *• EXOS Ebisu Building 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan*
Phone +81.03.3445.7671 • Fax +81.03.3445.7668 • http://jp.actel.com

Actel Hong Kong *• Room 2107, China Resources Building • 26 Harbour Road • Wanchai • Hong Kong*
Phone +852 2185 6460 • Fax +852 2185 6488 • www.actel.com.cn

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