SmartGen Hard Multiplier Adder/Subtractor v1.0

Handbook

Actel
POWER MATTERS

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Introduction

At the basic level, SgHardMultAddSub (SmartGen RTAX-DSP Multiplier-Adder/Subtractor) performs a single 18x18 two's complement signed multiplication along with an addition or subtraction with a third operand. You can choose the width of the operands (at pre-synthesis configuration time), the source of the third operand, whether any of the operands is a constant and whether any of the operands or the result is registered. Implementation is limited to those device families that contain MATH blocks (RTAX-DSP only at this time).

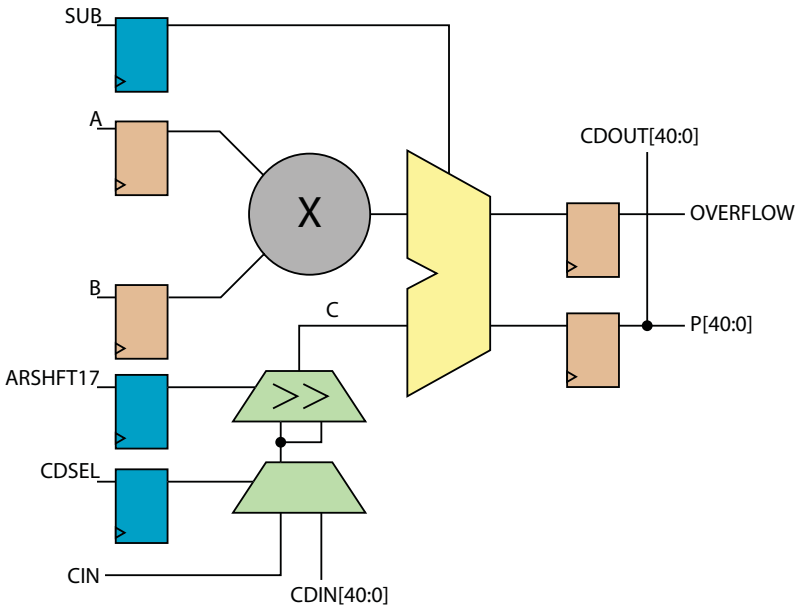

Figure 1 · SgHardMultAddSub Block Diagram

The SgHardMultAddSub block diagram is shown in Figure 1. Blue registers indicate control signals and brown registers are for data. Several aspects of SgHardMultAddSub can be configured with a user interface that generates a structured netlist in Verilog or VHDL. For a detailed description of the user interface settings, refer to Table 2-2 on page 13.

Key Features

SgHardMultAddSub has the following features:

- A structural netlist generator in Verilog or VHDL
- Configurable widths of operands A and B between 2 and 18
- Optional assignment of operand A to an 18-bit two's complement constant
- Configurable widths of operand CIN between 2 and 41
- Optional assignment of operand CIN to a 41-bit two's complement constant
- Optional operand CDIN[40:0] (cascaded from previous MATH block)
- Static or dynamic selection between CIN and CDIN[40:0] for the source of C operand
- Optional operation of Arithmetic-right-shift of operand C by 17 bits
- Static or dynamic selection between addition or subtraction operation
- Optional registers for A, B, P[40:0] (along with CDOUT[40:0] and OVERFLOW), CDSEL, ARSHFT17 or SUB with a common rising-edge clock, individual active-low asynchronous clear and individual active-high enable signals

- Additional output (for cascading to the next MATH block) CDOUT[40:0], which is a copy of P[40:0]

Core Version

This handbook applies to SgHardMultAddSub v1.0.

Utilization and Performance

SgHardMultAddSub can be used with any devices in the RTAX-DSP family. You must create a project with Axcelerator in the Libero IDE to use the SgHardMultAddSub macro. A summary of the data for SgHardMultAddSub is listed in Table 1.

Table 1 · SgHardMultAddSub Device Utilization and Performance

Family	FPGA Resources			Performance
	Sequential	Combinatorial	MATH	
RTAX-DSP	0	0	1	> 135 MHz

Note: Data in this table was obtained using typical synthesis and layout settings under STD Speed Grade and MIL operating conditions.

The benchmarks were obtained using the macro configuration settings shown in Table 2.

Table 2 · SgHardMultAddSub Benchmark Options

Configuration Option	Setting
Function	Multiplier with Adder/Subtractor
Input Port A	
Use Constant	Unselected
Constant Value (Hex)	N/A
Width	18
Register Port	Selected
Input Port B	
Width	18
Register Port	Selected
Input Ports CIN/CDIN/CDSEL	
Input Source(s)	CDIN from Previous math Block and Routed CIN
Constant Value (Hex)	N/A
CIN Width	41
Register CDSEL Port	Selected

Table 2 · SgHardMultAddSub Benchmark Options

Configuration Option	Setting
Input Port ARSHFT17	
Arithmetic Right Shift of Cascaded Input	Selected
Register Port	Selected
Output Port P	
Register Port	Selected
Input Port SUB	
Register Port	Selected
Target FPGA	
Die	RTAX4000D

Functional Block Description

SgHardMultAddSub, shown in Figure 1 on page 5, consists of a single MATH18x18 macro configured for two's complement signed multiply operation followed by addition or subtraction, as shown in Table 1-1.

Table 1-1 · SgHardMultAddSub Operand Table

P[40:0] =	C + (A x B), when SUB = 0
	C - (A x B), when SUB = 1
CDOUT[40:0]=	P[40:0]
OVERFLOW	if C +/- (A x B) > 2^{40} -1, then OVERFLOW = 1
	if C +/- (A x B) < -2^{40}, then OVERFLOW = 1
	otherwise, OVERFLOW = 0

Operand C is defined in Table 1-2.

Table 1-2 · Truth Table for Propagating Data for Operand C

CDSEL_q	ARSHFT17_q	Operand C
0	0	CIN[40:0]
0	1	{{17{CIN[40]}}, CIN[40:17]}
1	0	CDIN[40:0]
1	1	{{17{CDIN[40]}}, CDIN[40:17]}

Register Usage

All internal registers are TMR hardened to eliminate radiation-induced single-event upsets (SEU). They have a common rising-edge clock, individual active-low asynchronous clear and individual active-high enable signals. The pinout for internal registers is shown in Figure 1-1.

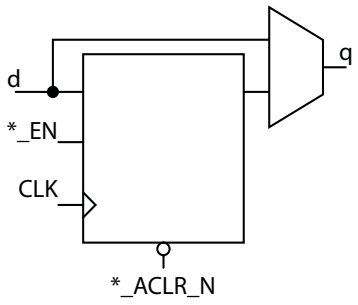

Figure 1-1 · Pinout of Internal Registers

When SgHardMultAddSub is configured to use registers for any of the operands, the input and output ports shown in Table 1-3 appear in the generated macro.

Table 1-3 · SgHardMultAddSub Register Ports

Register Port	Port Name		
	Rising-Edge Clock	Active-low Asynchronous Clear	Active-high Enable
A	CLK	A_ACLR_N	A_EN
B		B_ACLR_N	B_EN
SUB		SUB_ACLR_N	SUB_EN
CDSEL		CDSEL_ACLR_N	CDSEL_EN
ARSHFT17		ARSHFT17_ACLR_N	ARSHFT17_EN
P (along with CDOUT[40:0] and OVERFLOW)		P_ACLR_N	P_EN

2 Interface Description

Ports

Figure 2-1 shows the SgHardMultAddSub input and output ports. The ports shown are a superset of all possible ports. Only a subset of the ports are used in any given SgHardMultAddSub configuration.

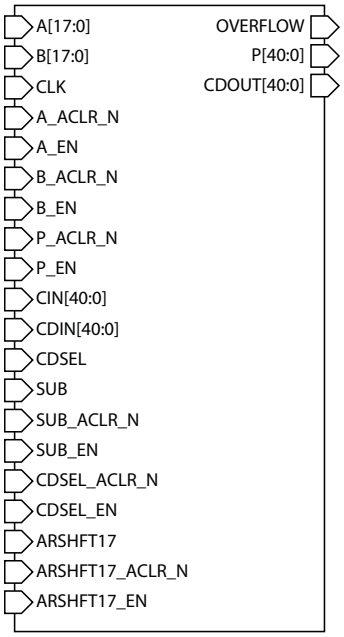

Figure 2-1 · SgHardMultAddSub Pinout Diagram

The port signals for the SgHardMultAddSub macro are defined in Table 2-1.

Table 2-1 · SgHardMultAddSub Ports

Signal	Input/ Output	Polarity	Description
A	Input	High	Input data A
B	Input	High	Input data B
CLK	Input	Rising	Input clock for A, B, CDSEL, SUB, ARSHFT17, P[40:0] (along with CDOUT[40:0] and OVERFLOW) registers.
A_ACLR_N	Input	Low	Asynchronous reset for data A registers
A_EN	Input	High	Enable for data A registers
B_ACLR_N	Input	Low	Asynchronous reset for data B registers
B_EN	Input	High	Enable for data B registers
P_ACLR_N	Input	Low	Asynchronous reset for result P[40:0] (along with CDOUT[40:0] and OVERFLOW) registers

Table 2-1 · SgHardMultAddSub Ports

Signal	Input/ Output	Polarity	Description
P_EN	Input	High	Enable for result P[40:0] (along with CDOUT[40:0] and OVERFLOW) registers
CIN	Input	High	Routed input for operand C See Table 1-2 on page 9 for information on how CIN is propagated to operand C
CDIN[40:0]	Input	High	Cascaded input for operand C The entire bus must be driven by an entire CDOUT[40:0] of another MATH block. See Table 1-2 on page 9 for information on how CDIN[40:0] is propagated to operand C
SUB	Input	High	Subtract operation P[40:0] = C + (A x B) when SUB = 0 P[40:0] = C - (A x B) when SUB = 1 Refer to Table 1-2 on page 9 to see how operand C is derived from CIN or CDIN[40:0]
CDSEL	Input	High	Select source of operand C When CDSEL = 1, propagate CDIN[40:0] When CDSEL = 0, propagate CIN
ARSHFT17	Input	High	When asserted, a 17-bit arithmetic right-shift is performed on operand C going into the accumulator
SUB_ACLR_N	Input	Low	Asynchronous reset for SUB register
SUB_EN	Input	High	Enable for SUB register
CDSEL_ACLR_N	Input	Low	Asynchronous reset for CDSEL register
CDSEL_EN	Input	High	Enable for CDSEL register
ARSHFT17_ACLR_N	Input	Low	Asynchronous reset for ARSHFT17 register
ARSHFT17_EN	Input	High	Enable for ARSHFT17 register
P[40:0]	Output	High	Result data: P[40:0] = C + (A x B) when SUB = 0 P[40:0] = C - (A x B) when SUB = 1 Refer to Table 1-2 on page 9 to see how operand C is derived from CIN or CDIN[40:0]

Table 2-1 · SgHardMultAddSub Ports

Signal	Input/ Output	Polarity	Description
CDOUT[40:0]	Output Cascade	High	Cascade output of result P[40:0]. CDOUT is a copy of P[40:0]; the entire bus must either be dangling or drive an entire CDIN[40:0] of another MATH block in cascaded mode.
OVERFLOW	Output	High	If C +/- (A x B) > 2^{40} -1 then OVERFLOW = 1 If C +/- (A x B) < -2^{40}, then OVERFLOW = 1 Otherwise, OVERFLOW = 0 Refer to Table 1-2 on page 9 to see how operand C is derived from CIN or CDIN[40:0]

Configuring the SgHardMultAddSub Macro

SgHardMultAddSub settings for configuring the macro are listed in Table 2-2. You can double-click the SgHardMultAddSub macro in the Project Manager Catalog or open and configure the macro in SmartDesign (see "SmartDesign" on page 15).

Table 2-2 · SgHardMultAddSub Configuration Descriptions

Name	Valid Range	Description
Function		Selects macro function Multiplier with Adder, Multiplier with Subtractor, or Multiplier with Adder/Subtractor
Input Port A		
Use Constant		Sets input port A to constant
Constant Value (Hex)	-2^{17} to (2^{17} - 1)	Two's complement value of A, if A is constant. Values shorter than 18 bits are padded with zeros. Negative values must be a full 18 bits wide.[1]
Width	2 to 18	Width of input port A (if A is not constant); if shorter than 18 bits it is sign-extended [2]
Register Port		Registers input port A (if A is not constant)
Input Port B		
Width	2 to 18	Width of input port B; if shorter than 18 bits it is sign-extended [2]
Register Port		Registers input port B
Input Ports CIN/CDIN/CDSEL		
Input Sources		Source(s) of operand C, such as CIN Routed from Fabric, CIN Constant, CDIN from Previous Math Block, CDIN from Previous Math Block and Routed CIN, CDIN from Previous Math Block and Constant CIN; see Table 1-2 on page 9

Table 2-2 · SgHardMultAddSub Configuration Descriptions

Name	Valid Range	Description
Constant Value (Hex)	-2^{40} to (2^{40} - 1)	Two's complement value of CIN, if CIN is constant. Values shorter than 41 bits are padded with zeros. Negative values must be a full 41 bits wide.[3]
CIN Width	2 to 41	Width of input port CIN; if shorter than 18 bits it is sign-extended [2]
Register CDSEL Port		Registers input port CDSEL
Input Port ARSHFT17		
Arithmetic Right Shift of Cascaded Input		Selects Arithmetic right-shift of operand C. See Table 1-2 on page 9 for information on obtaining values for operand C
Register Port		Registers input port ARSHFT17
Output Port P		
Register Port		Registers output port P[40:0] (along with CDOUT[40:0], and OVERFLOW)
Input Port SUB		
Register Port		Registers input port SUB
Target FPGA		
Die	RTAX2000D or RTAX4000D	Target device

1. *E.g. 0x1FFFF means +131071 (2^{17} - 1), while 0x3FFFF means -1*
2. *E.g. if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1*
3. *E.g. 0xFFFFFFFFFF means +(2^{40} - 1), while 0x1FFFFFFFFF means -1.*

3 Tool Flows

Licenses

SgHardMultAddSub is included for free in the Libero® IDE Project Manager Catalog and does not require a separate license to instantiate and use in Actel devices. A complete structural netlist is provided for the macro.

SmartDesign

SgHardMultAddSub is available for download from the Libero® Integrated Design Environment (IDE) IP Catalog via the web repository. Once it is listed on the Catalog, the macro can be instantiated using SmartDesign. To use it, double-click or drag it from the Arithmetic section of the Catalog onto the Canvas. For information on using SmartDesign to configure, connect, and generate cores, see the Libero IDE online help.

Figure 3-1 shows the SgHardMultAddSub configuration window. The configuration window displays the configuration options for each input port and output port. After configuring and generating the macro instance, you can simulate basic functionality. The macro can then be instantiated as a component of a larger design.

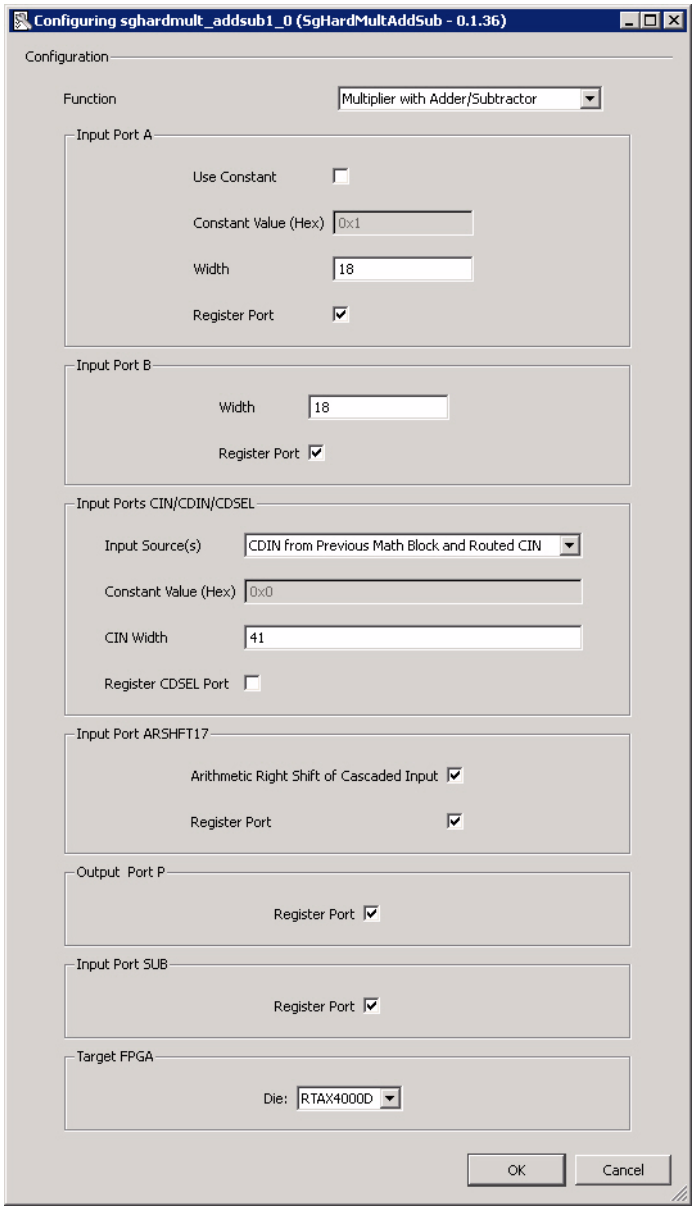

Figure 3-1 · SgHardMultAddSub Configuration Window

Place-and-Route in the Libero IDE

After running synthesis on the instantiated design, click the Place&Route button in the Project Manager to open Designer. SgHardMultAddSub requires no special place-and-route settings.

A

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Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

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The technical support email address is tech@actel.com.

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Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

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