Rate This Document

Mixed Signal Power Manager for Fusion

User's Guide

Actel
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

© 2010 Actel Corporation. All rights reserved.

Printed in the United States of America

Part Number: 50200167-2

Release: June 2010

No part of this document may be copied or reproduced in any form or by any means without prior written consent of Actel.

Actel makes no warranties with respect to this documentation and disclaims any implied warranties of merchantability or fitness for a particular purpose. Information in this document is subject to change without notice. Actel assumes no responsibility for any errors that may appear in this document.

This document contains confidential proprietary information that is not to be disclosed to any unauthorized person without prior written consent of Actel Corporation.

Trademarks

Actel, Actel Fusion, IGLOO, Libero, Pigeon Point, ProASIC, SmartFusion and the associated logos are trademarks or registered trademarks of Actel Corporation. All other trademarks and service marks are the property of their respective owners.

Table of Contents

Introduction

This document provides you with the basic information required to use and demonstrate the Mixed Signal Power Manager (MPM) system in conjunction with the Actel Fusion® Advanced Development Kit (FADK) board. You should read the *Fusion Advanced Development Kit User's Guide* before attempting to use this user's guide. MPM is a reference design which is programmed into a Fusion device and can be controlled and modified by the MPM GUI .

Based on Fusion FPGA technology, the MPM delivers superior power monitoring, power sequencing, closed-loop trimming, and power-up and power-down control of up to 16 external power supplies. You do not need to deal with FPGA design tools to configure power management sequencing, levels, or thresholds; the MPM design is programmed into the Fusion device through an easy-to-use standalone graphical user interface (GUI) tool. The GUI enables you to configure power management for up to 16 external power supplies and drive output signals as the monitored voltages meet or deviate from the user-programmed operating limits, all without opening Actel's Libero® Integrated Design Environment (IDE). This adds more flexibility by leveraging Fusion's flash FPGA technology, reduces total parts count on the board level, and increases system reliability by eliminating single points of failure. MPM delivers highly configurable integrated power management using the highly reliable, low power, flash-based Fusion mixed signal FPGA.

This document assumes some knowledge of MPM or similar application-specific standard product (ASSP) applications.

System Summary

This guide and the demonstrator are targeted towards the FADK board. An I/O level diagram of the MPM system is shown in Figure 1.

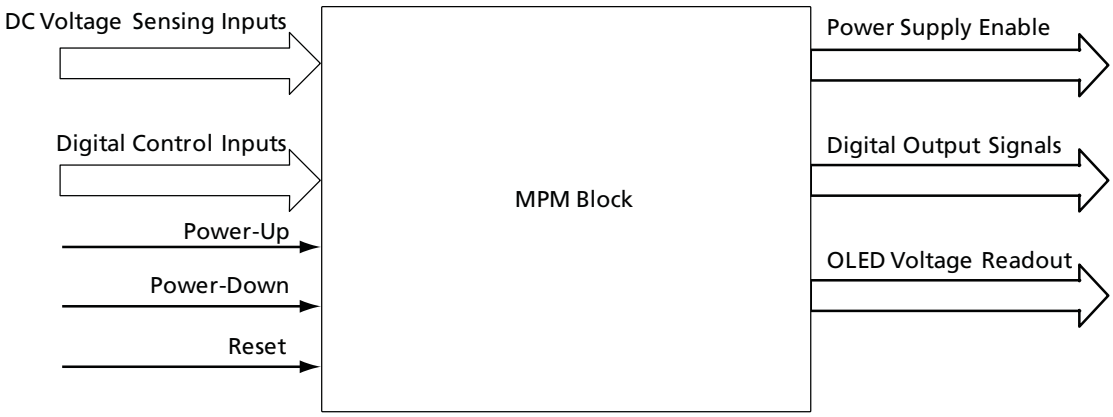

Figure 1 · MPM I/O

Figure 2 shows a typical system-level diagram using 1 channel of the MPM.

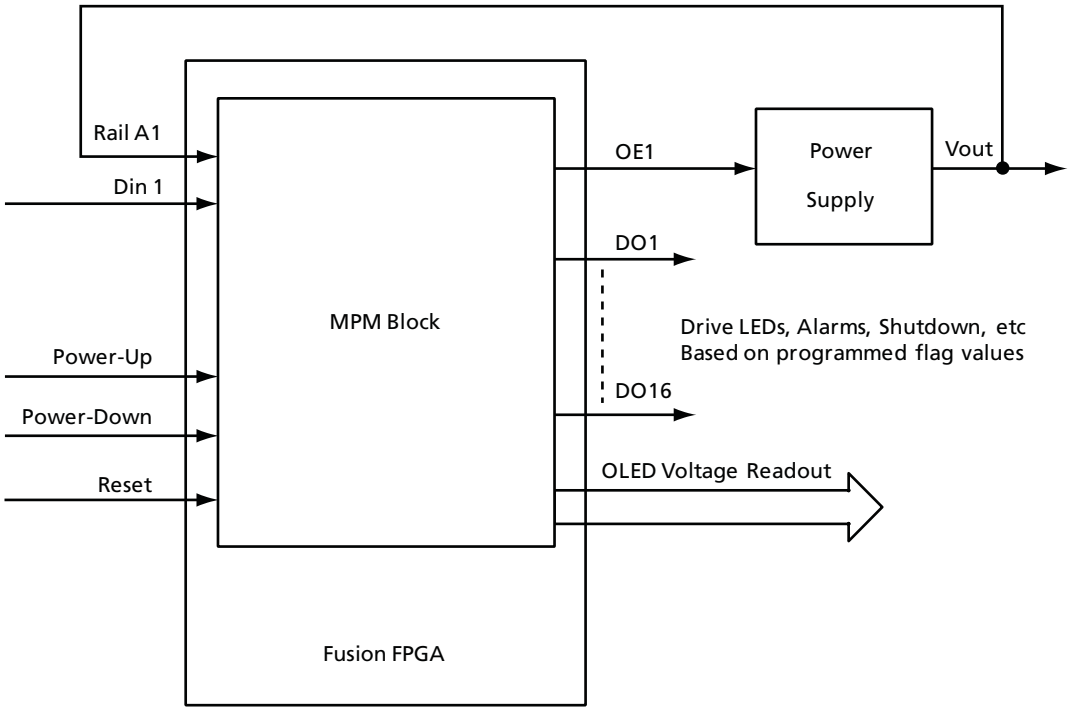

Figure 2 · Typical System-Level Diagram

Figure 3 shows an MPM system as it is implemented on the FADK board.

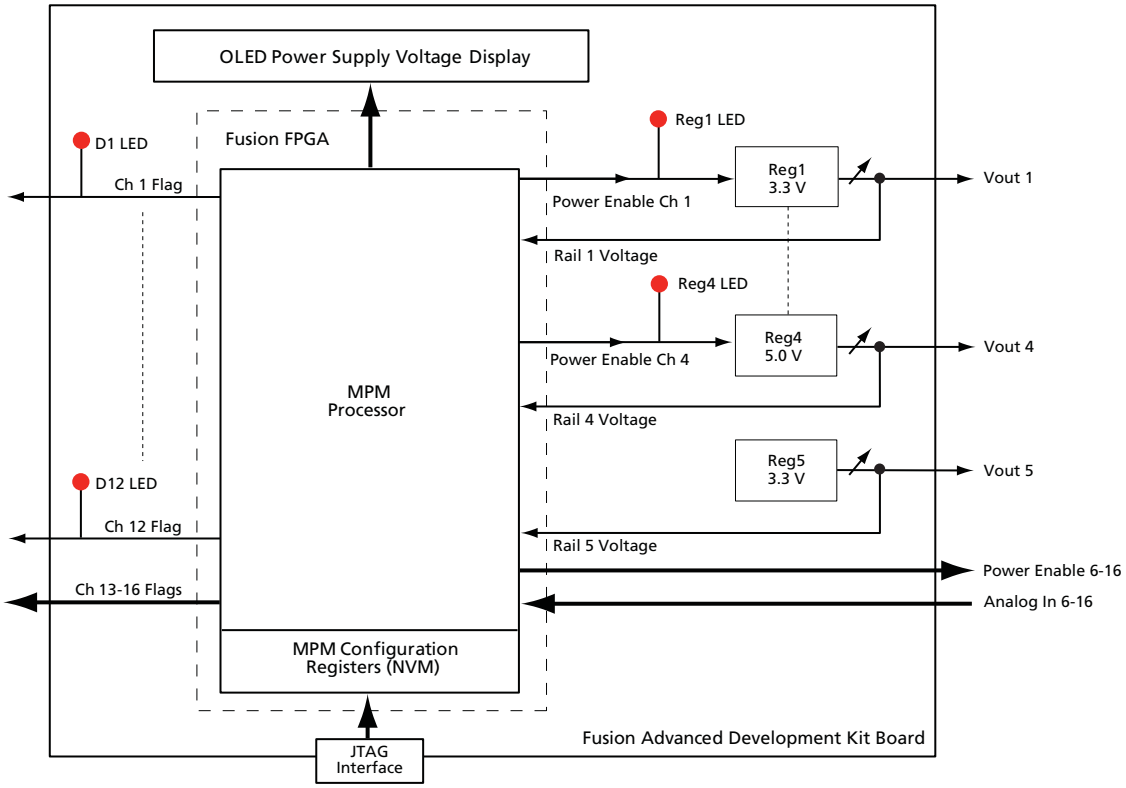

Figure 3 · MPM System Block Diagram

Using the MPM GUI, you configure all MPM input and output requirements. You write to the Fusion AFS nonvolatile memory (NVM) using a low-cost programming stick (LCPS) via the joint test action group (JTAG) interface. This sets all threshold flag levels, output signals, power sequencing, and debug level settings for MPM operation. For more information on MPM configuration, refer to "GUI Configuration Tabs" on page 10. Once programmed, no external functions or connections are required for MPM to function, as it is a standalone application.

When using the FADK board, you are not required to add any manual connections to either the mixed signal header or the 40-pin P8051 header. Refer to "Extended Board Capabilities" on page 21 for more information. MPM functionality is demonstrated using the four regulators on the board, which have fixed connections to the MPM design. These 4 regulators act as independent power supplies that are controlled by the MPM. To access other channels beyond these four voltage regulators, or to access the digital I/O, you must use the mixed signal header or the 40-pin header.

Output voltages from the on-board regulator power supplies are displayed on the OLED at the top of the FADK board. However, this is not a required part of the autonomous MPM design. The OLED is used only as part of the reference design for demonstration and debugging purposes.

1 MPM Graphical User Interface (GUI)

Overview

MPM includes a Windows®-based executable standalone GUI (the MPM GUI) that enables you to access the register data stored in the FPGA NVM. The nonvolatile memory MPM operation, including voltage limits, digital input and outputs settings, and power sequencing settings are stored in the NVM within the Fusion FPGA.

Each screen in the GUI has help guidelines displayed in the right pane. Refer to the "GUI Configuration Tabs" on page 10 section for more information.

Installation

The MPM software, which consists of a GUI and configuration software, is a standalone program. However, a valid installation of the Actel Flashpro software is required to program devices with MPM data. For more information on Flashpro, refer to the Actel website: www.actel.com/products/hardware/program_debug/flashpro.

The MPM installer is a standalone executable. To install the software, double-click the executable file and follow the steps outlined in the installer. When the installation is complete, a configuration file is created:

<homedir>/Application Data/actel/MpmConfigurator/MpmConfig.txt.

This is an example configuration file:

```
BoardType=FADK
StaplTemplate=C:\\Actel\\MPM\\template\\Template.stp
TclScript=C:\\Actel\\MPM\\output\\MPMloader.tcl
StaplFile=C:\\Actel\\MPM\\output\\MPM.stp
MemFile=C:\\Actel\\MPM\\output\\MPM.mem
DebugLevel=ALL
FlashproPath=C:\\Actel\\Libero_v8.5\\FlashPro\\bin\\flashpro.exe
```

The configuration file can be manually edited to alter file paths. The only relevant configuration that should be altered in MpmConfig.txt is the DebugLevel parameter, which determines how much debug information is displayed on the OLED. For most users, the default (RAILS, which displays rail voltages only) is sufficient. To include several debug displays (real-time counter and output tests), change this configuration setting to ALL. To display nothing on the OLED, change this configuration setting to NONE.

The first time you run the MPM software, a prompt will appear to locate the FlashPro executable.

GUI Configuration Tabs

Power

The Power tab (Figure 1-1) is used to assign requirements for each voltage rail to be controlled, such as the nominal voltage, threshold/flag voltages, and power-up/-down sequences. For more information, refer to the side panel help by clicking on the associated boxes.

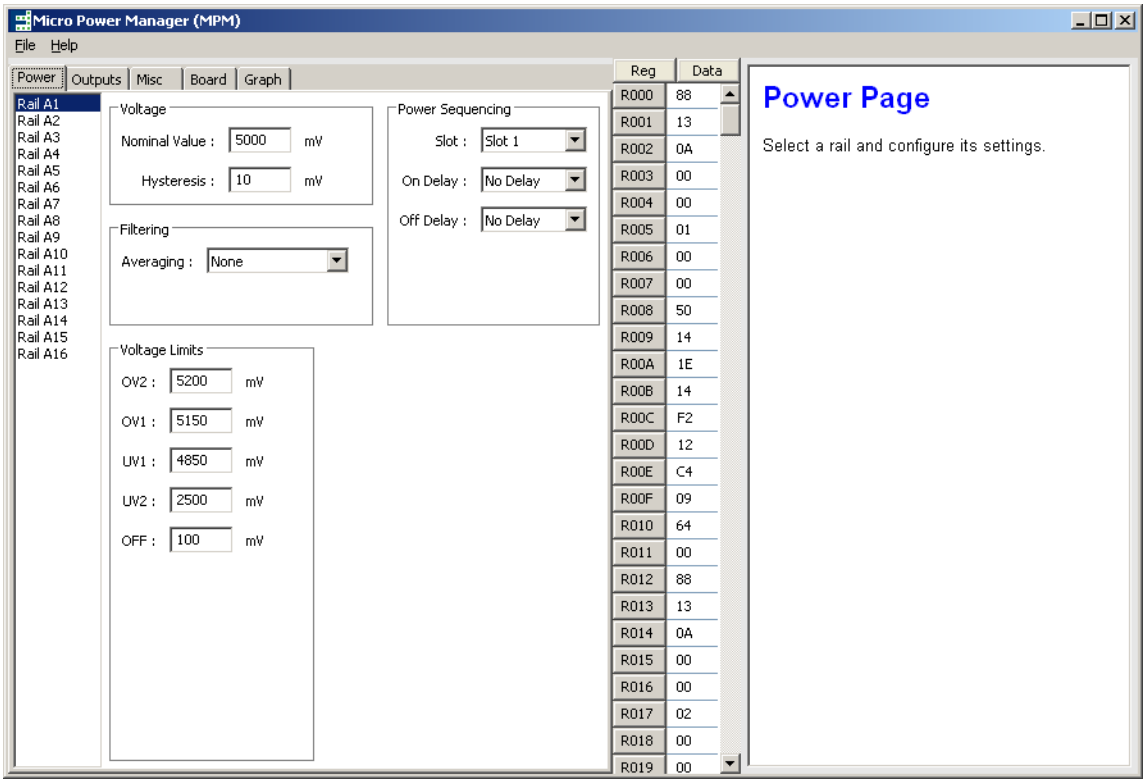

Figure 1-1 · Power Tab

Outputs

The Outputs tab (Figure 1-2) is used to define the condition for and polarity of the assertion of 16 digital outputs. This tab also enables you to utilize the 16 digital inputs to control the output logic via the digital input panel. For more information, refer to the side panel help by clicking on the associated boxes.

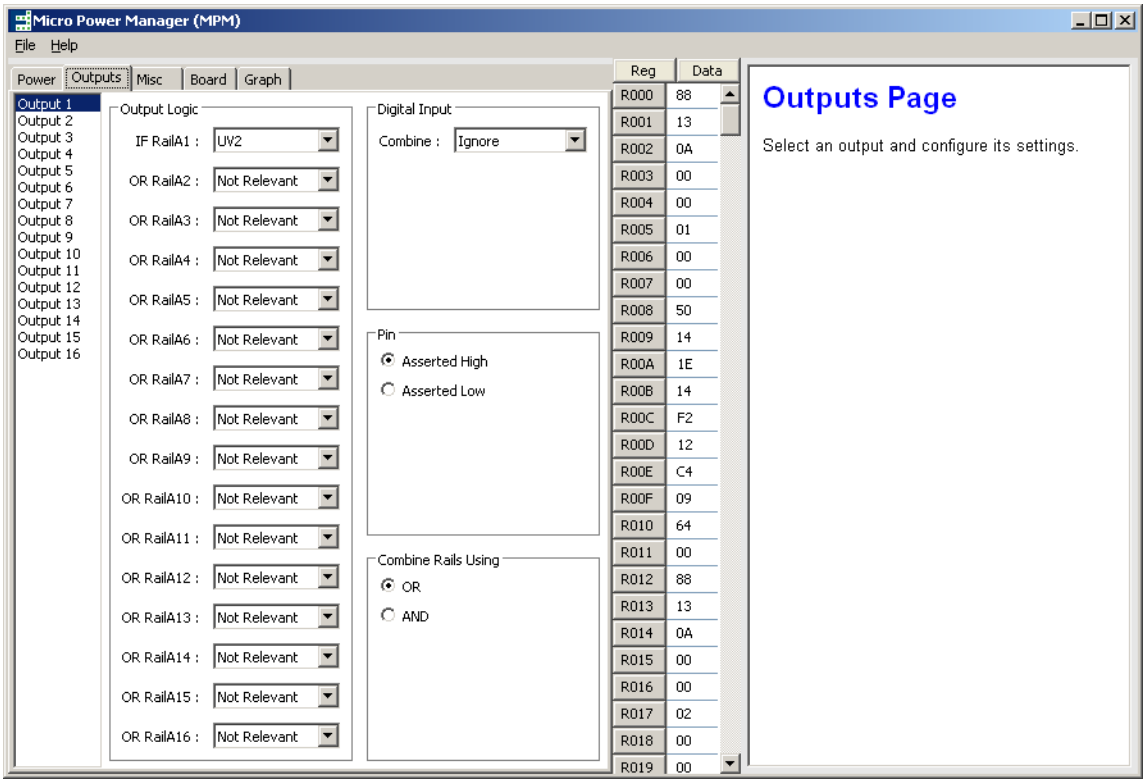

Figure 1-2 · Outputs Tab

Misc

The Misc tab (Figure 1-3) is used to configure calibration settings and actions on power-up and power-off. For more information, refer to the side panel help by clicking on the associated boxes.

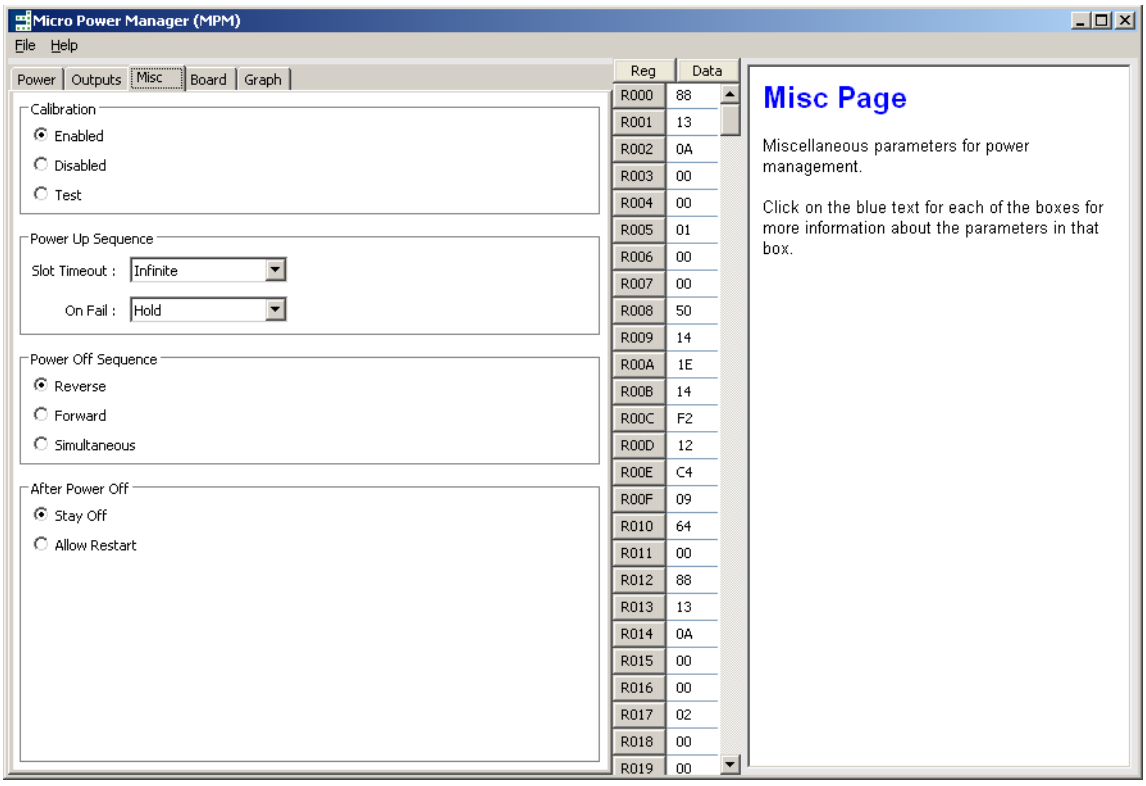

Figure 1-3 · Misc Tab

Board

The Board tab (Figure 1-4) is a reference guide and provides the pinouts of rails, enable signals, digital inputs, and digital outputs. You can change the names of these items by altering the associated cell in the custom name column. If you are targeting a board other than the FADK board, the pre-loaded tables will not be valid and you must select the **Other** radio button. For more information, refer to the side panel help by clicking on the associated boxes.

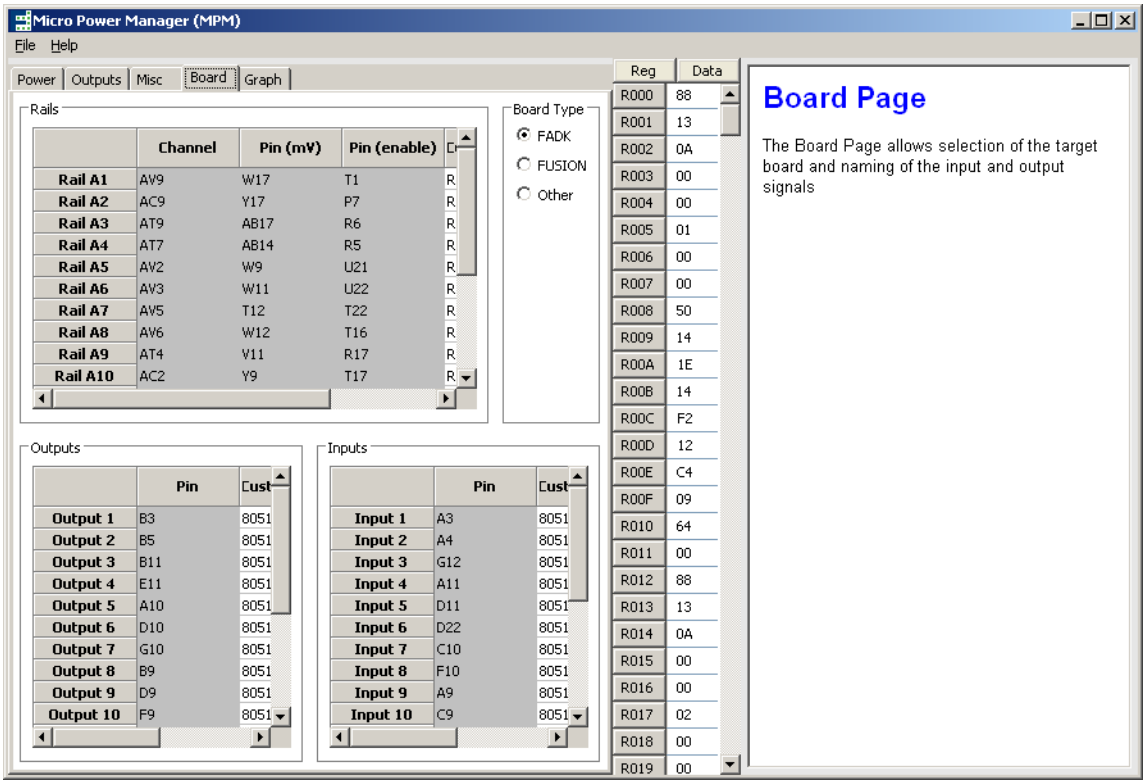

Figure 1-4 · Board Tab

Graph

The Graph tab (Figure 1-5) is a visual representation of the power-up and power-down sequencing. It is meant to be used as a visual guideline only, displaying only relative time frames of power-up and power-down as a result of sequencing requirements entered on the Power tab. Rise and fall times are not accurate and voltage levels are not taken into account. For more information, refer to the side panel help by clicking on the associated boxes.

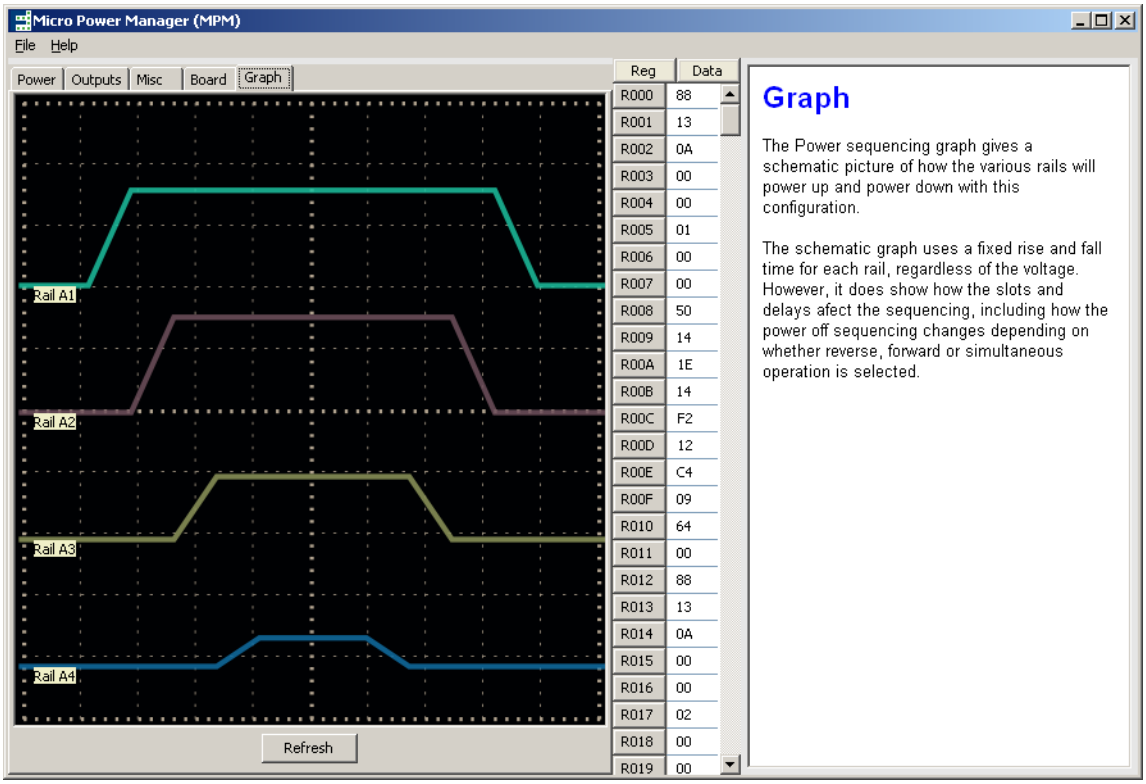

Figure 1-5 · Graph Tab

Programming the Device

In the MPM GUI, the column of buttons marked R and followed by a number (Figure 1-6) displays a register map for the configuration data. This relates to how the parameters are stored in the FPGAs NVM.

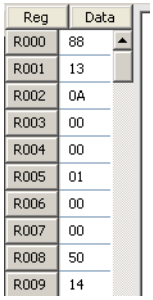

Figure 1-6 · Register Data

The File menu contains the Write Device and Write NVM menu options.

Write Device programs the NVM register values and the FPGA device with the MPM circuit design. Write Device is required when the Fusion mixed signal FPGA device is either blank or programmed with a different design. You can perform updates to flags and settings using the Write NVM menu option.

Write NVM writes the configuration created using the various tabs in the MPM GUI and programs the register values shown in the column of buttons marked R, followed by a number.

Note: When using the FADK board, you are required to use an LCPS programmer module (included in the Fusion Advanced Development Kit) to program the Fusion device on the board.

2 Demonstration

After loading a demonstration program (MPMDemo.txt) into the MPM and programming the M1AFS1500 FPGA on the Fusion Advanced Development Kit (Figure 2-1 on page 18), the reference design supplied with this user's guide will demonstrate the following:

1. Powering up of Reg1, Reg2, Reg3, and Reg 4 with 1 second delays, assuming nominal voltage has been reached and sampled by the analog input channels AV1, AV2, AV3, and AV4
   - Observe the LEDs for Reg1, Reg2, Reg3, Reg4, and Output Channel LEDs D1, D2, D3, and D4 light up sequentially.
2. Powering down of Reg1, Reg2, Reg3, and Reg with 1 second delays
   - Observe the LEDs for Reg4, Reg3, Reg2, Reg1, and Output Channel LEDs D4, D3, D2, and D1 turn off sequentially, in reverse order of the power-up sequence.
3. As controlled by Regulator Potentiometer (RPOT) 5 (0 to 3.3 V), observe the Output Channel LEDS D5, D5, D7, and D8 enabled as Undervoltage 1, Undervoltage 2, Overvoltage 1, and Overvoltage 2 are reached.
4. Validate the voltage regulator output levels through the OLED readout as the potentiometers are adjusted.

Note: This demonstration assumes you are familiar with the Fusion Advanced Development Kit (FADK) board.

Associated files for this demonstration can be downloaded from the Actel website: www.actel.com/download/rsc/?f=MixedSignal_Power_Manager_DF.

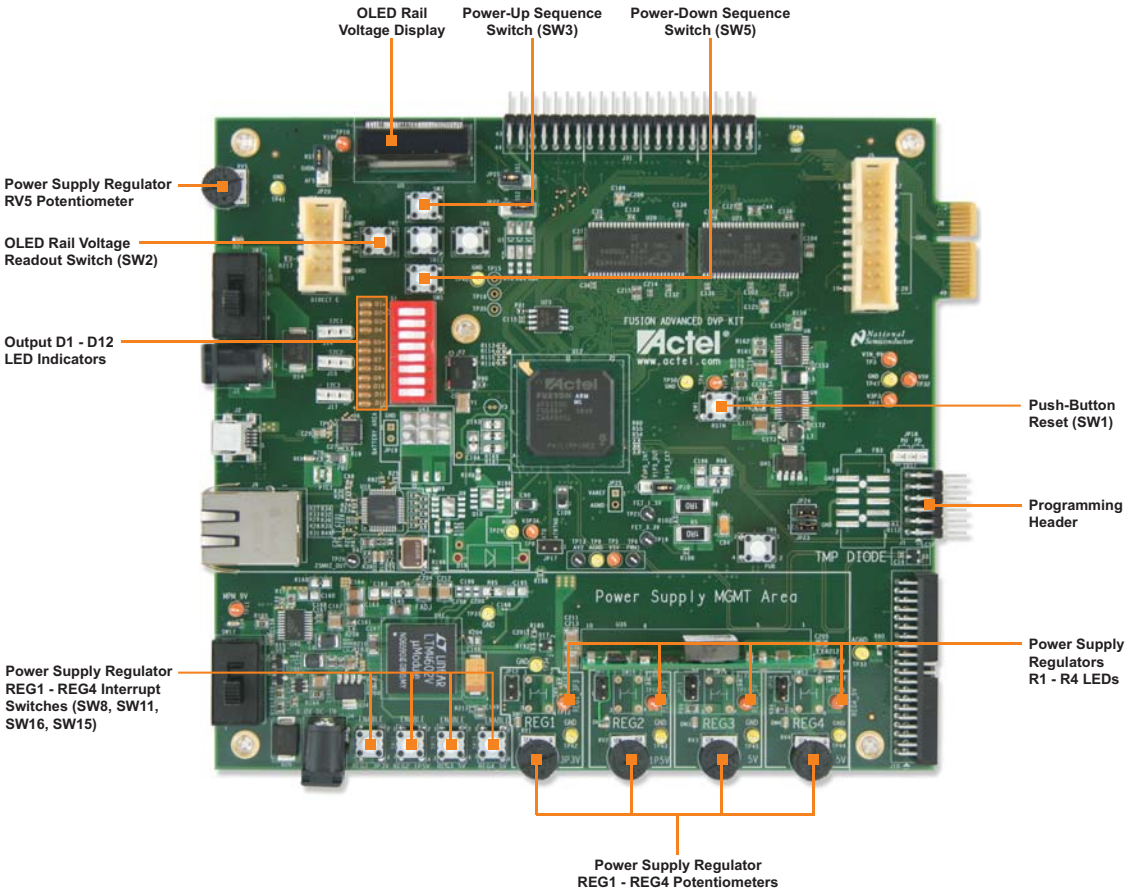

Figure 2-1 · Fusion Advanced Development Kit Board

To perform the demonstration:

1. Download the MPM software and the MPMDemo.txt file to a PC.
2. Install the MPM software, FlashPro Software, and drivers to a PC.

   Note: FlashPro3 drivers can be located on the <FlashPro>/Drivers folder
3. Attach the two external power supplies to the FADK board and plug them into the power outlet.
4. Attach the low-cost programming stick to the FADK board.
5. Attach the 2 USB cables to the FADK board and plug the other end of the cables into the USB ports on your PC.
6. Turn the REG1, REG2, REG3, and REG4 potentiometers (RPOTs) all the way to the left (counterclockwise) position (maximum voltage).
7. Adjust the RV5 potentiometer to approximately mid-range.
8. Turn on the power supply switches on the FADK board.
9. Open the MPM software by clicking the MPM icon on the PC desktop.
10. You can browse the Power, Outputs, Misc, Board, and Graphs tabs on the MPM GUI to get familiar with them. Clicking inside a box on the GUI (such as the Power box) will display help instructions on the right side of the GUI.

11. From the File menu, select Load Values. Browse to and select the MPMDemo.txt file that you downloaded from the web. This is the MPM reference design which will be demonstrated on the FADK board, and will drive all data that you see in the MPM GUI tabs, as described below.
12. On the Power tab, left side, click down through Rails A1, A2, A3, A4, and A5. As you do this, note the nominal and over/under voltage (OV and UV) values in the Voltage and Voltage Limits boxes. DO NOT CHANGE THE VALUES IN THE GUI AT THIS TIME.

    As you click through the rails, note the power sequencing selections that have been made in the power sequence selection box. For example, Rail 1 is assigned to time Slot 1, with a delay of 1 second for power up (after initialization) and a delay of 1 second for power down. Analog filtering is not used for this demonstration. You can view the registers and data that will be used for these selections, but it is not necessary to make any changes here.
13. On the Outputs tab, left side, click down through Outputs 1, 2, 3, and 4. Note that the conditions for the output logic are already set. Outputs 1, 2, 3, and 4 will be enabled as analog input rails sense nominal voltages as determined on the Power tab. DO NOT MAKE ANY CHANGES TO THE PROGRAMMED VALUES AT THIS TIME. No other conditions are set for Outputs 1, 2, 3, and 4 to be enabled. Notice on the Pin box that the program will assert the output pin active Low.
14. On the Outputs tab, left side, click through Outputs 5, 6, 7, and 8. Note that the demonstration program instructs the outputs to go active when analog input Rail 5 senses overvoltage 1 and 2 and undervoltage 1 and 2, as specified for Rail 5 on the Power tab.
15. Select the Misc tab. Note that the Power Off Sequence has been selected to be Reverse, which means the reverse sequence of the power-up sequence.
16. From the File menu, select Write Device. This will load the Fusion M1AFS1500 FPGA device on the Fusion Advanced Development Kit board with the MPM core module and the specific reference design for the MPM demonstration, as driven from the MPMDemo.txt file. If the software can not find the FlashPro software, you must browse to the location of the FlashPro.exe file for the device programming to occur. FlashPro software can be downloaded at no charge from Actel's website and you do not need a license.
17. As the M1AFS1500 is being programmed, you will see a Command Line screen pop up on the PC. DO NOT CLICK THIS SCREEN OFF UNTIL YOU ARE TOLD TO DO SO AT THE END OF THE PROGRAMMING PROCESS. During the programming cycle, a yellow led will flash on the low-cost programming stick. When the FPGA programming is complete, the programming stick LED will turn green.
18. Momentarily press the FADK board reset switch (SW1).
19. Momentarily press the enable switch (SW3).
20. Assuming the RPOTS REG1–REG4 were rotated completely counterclockwise (maximum voltage output condition), the LEDs for regulators 1, 2, 3, and 4 will turn on at 1 second intervals. This demonstrates, per the MPM GUI selection, that each regulator, which represents a power supply, is powered up sequentially, having been assigned to time slots 1, 2, 3, and 4.

    Note: Sequencing to the next time slot is based on the previous regulator (power supply) having reached an undervoltage 1 level. RPOTs should already be at maximum voltage to ensure the subsequent channel turns on.
21. Per the assignments on the Power tab in the MVM GUI, the program is designed to enable the outputs when the power supply attains a nominal value. Since RPOTS REG1–REG4 are set to maximum value, the output indicator LEDS D1–D4 are not on. By adjusting the any of the RPOTS 1–4 to mid-range, you can observe the output LEDs D1–D4 turning on as the nominal voltage is achieved. These values can be observed in the OLED display by pressing the SW2 momentary. Channel A in the OLED is for voltage Rail A1/REG1, channel B is for Rail A2/REG2, channel C is for Rail A3/REG3, channel D is for Rail A4/REG4, and Channel E is for RailA5/RV5. The OLED can cycle beyond Channel E; however, this is beyond the current MPM program, and depends on external power supplies.
22. Adjust all RPOTS so that their respective outputs, LED D1, D2, D3, and D4, are continuously on.
    - Nominal for Rail A1 is 3.3 V (3,300 mV)
    - Nominal for Rail A2 is 1.5 V (1,500 mV)

- Nominal for Rail A3 is 5.0 V (5,000 mV)
- Nominal for Rail A4 is 4.8 V (4,800 mV)

23. The MPM also has the capability of immediately interrupting and disabling a power supply rail. This is demonstrated by pressing any or all of the ENABLE momentary contact switches located at the bottom of the FADK board, to the left of the on-board regulators, ENABLE REG1–REG4.
24. To demonstrate the power-down sequence programmed into the MPM, momentarily press contact switch SW5, located under the OLED display. You will note that the power-down sequence is the opposite of the power-up sequence: turning off regulator power supplies R4, R3, R2, and R1 at 1 second intervals.
25. Lastly, based on the MPM GUI output assignments for Rail A5, the output LEDs D5, D6, D7, and D8 will turn on based on the voltage value and position of RPOT 5. D6 and D5 are for overvoltage 1 and 2 respectively, and D7 and D8 are for undervoltage 1 and 2 respectively.

    Verify the voltage values by pressing SW2 until the E voltages can be viewed in the OLED.

    Rotate the RPOT5 clockwise to reduce the voltage to meet the undervoltages of 2,600 mV for UV1 and 2,400 mV for UV2.

    Rotate the RPOT5 counterclockwise to meet overvoltages 3,000 mV for OV1 and 3,200 mV for OV2, and notice the output LEDs for D5 – D8 turn on as the thresholds are reached. Outputs D5 – D8 should be off as RPOT is centered (approximately), as the voltage reaches the nominal voltage of 2,800 mV.
26. This is the end of the pre-programmed demonstration based on the imported MPMDemo.txt file.

Further Evaluation of MPM

To do further evaluation of the MPM capabilities, you can modify any of the values on the Power, Output, Misc, or Board tabs of the MPM GUI. When you are finished making the adjustments, select Write NVM from the File menu to try the program on the board.

The M1AFS1500 FPGA on the FADK board has already been loaded with the MPM core program based on the above demonstration and FPGA programming. From that point, in order to change the values in the MPM core, you only need to reprogram the internal nonvolatile memory (NVM) within the MPM/Fusion core. Reprogramming the NVM core only takes a few seconds. Be sure to wait for the LED on the low-cost programming stick to turn green, and the message in the FlashPro programming window on the PC that states the program has finished loading.

3 Extended Board Capabilities

For additional board capabilities, refer to the *Fusion Advanced Development Kit User's Guide*.

Board Pinout and Channel Mapping

Table 3-1 through Table 3-4 list the pinouts and provide a description of all I/Os shown in Figure 1 on page 5. You must build all necessary circuits for channels 5 and higher.

Table 3-1 · Analog I/O Pinout

Name	FADK Regulator #	Description	FADK Output LED #
Rail A1	Reg1	On-board 3.3 V switching regulator output (3P3V)	D1
Rail A2	Reg2	On-board 1.5 V switching regulator output (1.5 V)	D2
Rail A3	Reg3	On-board 5 V switching regulator output (5 V)	D3
Rail A4	Reg4	On-board 5 V LDO regulator output (5 V)	D4
Rail A5	–	POT-regulated (RV5) output voltage (0 to 3.3 V)	D5
Rail A6	–	Mixed signal header (J10) pin 5	–
Rail A7	–	Mixed signal header (J10) pin 7	–
Rail A8	–	Mixed signal header (J10) pin 11	–
Rail A9	–	Mixed signal header (J10) pin 13	–
Rail A10	–	Mixed signal header (J10) pin 2	–
Rail A11	–	Mixed signal header (J10) pin 6	–
Rail A12	–	Mixed signal header (J10) pin 8	–
Rail A13	–	Mixed signal header (J10) pin 12	–
Rail A14	–	PWM1 output voltage	–
Rail A15	–	PWM2 output voltage	–
Rail A16	–	Gate driver demonstration output voltage	–

Table 3-2 · Digital Input Pinout

Name	Description
DIN[0]	P8051 legacy header (J31) pin 1
DIN[1]	P8051 legacy header (J31) pin 3
DIN[2]	P8051 legacy header (J31) pin 5
DIN[3]	P8051 legacy header (J31) pin 7
DIN[4]	P8051 legacy header (J31) pin 9
DIN[5]	P8051 legacy header (J31) pin 11
DIN[6]	P8051 legacy header (J31) pin 13
DIN[7]	P8051 legacy header (J31) pin 17
DIN[8]	P8051 legacy header (J31) pin 19
DIN[9]	P8051 legacy header (J31) pin 21
DIN[10]	P8051 legacy header (J31) pin 23
DIN[11]	P8051 legacy header (J31) pin 27
DIN[12]	P8051 legacy header (J31) pin 29
DIN[13]	P8051 legacy header (J31) pin 31
DIN[14]	P8051 legacy header (J31) pin 33
DIN[15]	P8051 legacy header (J31) pin 35

Table 3-3 · Digital Output Pinout

Name	Description
DOUT[0]	P8051 legacy header (J31) pin 2
DOUT[1]	P8051 legacy header (J31) pin 4
DOUT[2]	P8051 legacy header (J31) pin 8
DOUT[3]	P8051 legacy header (J31) pin 10
DOUT[4]	P8051 legacy header (J31) pin 12
DOUT[5]	P8051 legacy header (J31) pin 14
DOUT[6]	P8051 legacy header (J31) pin 18
DOUT[7]	P8051 legacy header (J31) pin 20
DOUT[8]	P8051 legacy header (J31) pin 22
DOUT[9]	P8051 legacy header (J31) pin 24
DOUT[10]	P8051 legacy header (J31) pin 26
DOUT[11]	P8051 legacy header (J31) pin 30
DOUT[12]	P8051 legacy header (J31) pin 32
DOUT[13]	P8051 legacy header (J31) pin 34
DOUT[14]	P8051 legacy header (J31) pin 36
DOUT[15]	P8051 legacy header (J31) pin 38

Table 3-4 · Enable Output Pinout

Name	Description
POWER_ENABLE[0]	On-board 5V switching regulator enable (REG3_EN)
POWER_ENABLE[1]	On-board 5V LDO regulator enable (REG4_EN)
POWER_ENABLE[2]	On-board 3.3V switching regulator enable (REG1_EN)
POWER_ENABLE[3]	On-board 1.5V switching regulator enable (REG2_EN)
POWER_ENABLE[4]	Mixed signal header (J10) pin 27
POWER_ENABLE[5]	Mixed signal header (J10) pin 29
POWER_ENABLE[6]	Mixed signal header (J10) pin 31
POWER_ENABLE[7]	Mixed signal header (J10) pin 80
POWER_ENABLE[8]	Mixed signal header (J10) pin 22
POWER_ENABLE[9]	Mixed signal header (J10) pin 24
POWER_ENABLE[10]	Mixed signal header (J10) pin 26
POWER_ENABLE[11]	Mixed signal header (J10) pin 30
POWER_ENABLE[12]	Mixed signal header (J10) pin 32
POWER_ENABLE[13]	Mixed signal header (J10) pin 34
POWER_ENABLE[14]	Mixed signal header (J10) pin 36
POWER_ENABLE[15]	P8051 legacy header (J31) pin 37

Board Operation

Power-Up and Power-Down

By default, power-up and power-down are triggered by the up SW3 push-button and the down SW5 push-button, respectively.

However, by jumpering pins 21 to 23 of the mixed signal header, power-up becomes triggered by a rising edge on pin 19 of the mixed signal header. Similarly, jumpering pins 33 to 35 of the mixed signal header causes power-down to be triggered by a rising edge on pin 25 of the mixed signal header.

In a typical application, both jumpers should be placed as described above and pin 19 (power-up) should be tied to VDD. This would cause power-up to be triggered on MPM reset. Connecting a digital output to pin 25 would cause power-down to be triggered by the assertion of a particular output. This can be used to create a system (Figure 3-1) that powers down when a particular condition is met (as defined in the Outputs tab of the MPM GUI).

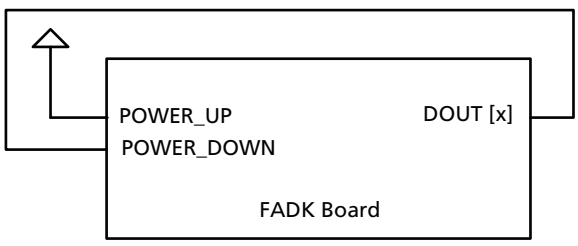

Figure 3-1 · Typical Power-Up and Power-Down Application

Push Buttons

Besides the up and down buttons used for power-up and power-down, the left SW2 and right SW6 push-buttons are used to cycle through the OLED displays.

Light-Emitting Diodes (LEDs)

Digital output signals (DOUT[7:0]) are tied to LEDs labeled on the board as D8, D7,D6, D5, D4, D3, D2, and D1 and are active Low.

Regulators

The FADK board contains four voltage regulators, located at the bottom right-hand corner of the board in the power supply management area. These four voltage regulators are as follows:

- 3.3 V switching regulator (LM3100MH)
- 1.5 V switching regulator (LP38693MP-ADJ)
- 5 V DC/DC switching regulator (ATA010A0X3Z)
- 5 V LDO regulator (LTM4602)

The output voltage for each regulator can be varied by approximately 20% from the nominal voltage by using the small thumb POTs at the bottom right of the board (RV1, RV2, RV3, and RV4).

When enabled, each regulator can be disabled (to simulate a black-out condition, for example) by pushing and holding the enable push-buttons at the bottom left of the board (SW8, SW11, SW16, and SW15).

Jumper Settings

To ensure proper OLED operation, observe the following jumper settings:

- JP20: pins 1-2
- JP21: pins 1-2
- JP22: pins 2-3

Additionally, since closed-loop trimming is not implemented in the MPM Phase 0 implementation, the PWM feedback networks must be left unconnected by ensuring that the following jumpers are not placed: JP12, JP13, JP14, and JP15.

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

Index

Actel is the leader in low power and mixed signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at www.actel.com.

Actel Corporation *• 2061 Stierlin Court • Mountain View, CA 94043 • USA*
Phone 650.318.4200 • Fax 650.318.4600 • Customer Service: 650.318.1010 • Customer Applications Center: 800.262.1060

Actel Europe Ltd*. • River Court, Meadows Business Park • Station Approach, Blackwater • Camberley Surrey GU17 9AB • United Kingdom*
Phone +44 (0) 1276 609 300 • Fax +44 (0) 1276 607 540

Actel Japan *• EXOS Ebisu Building 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan*
Phone +81.03.3445.7671 • Fax +81.03.3445.7668 • http://jp.actel.com

Actel Hong Kong *• Room 2107, China Resources Building • 26 Harbour Road • Wanchai • Hong Kong*
Phone +852 2185 6460 • Fax +852 2185 6488 • www.actel.com.cn

50200167-2/6.10