UG0065
User Guide
Fusion Starter Kit

Microsemi
Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

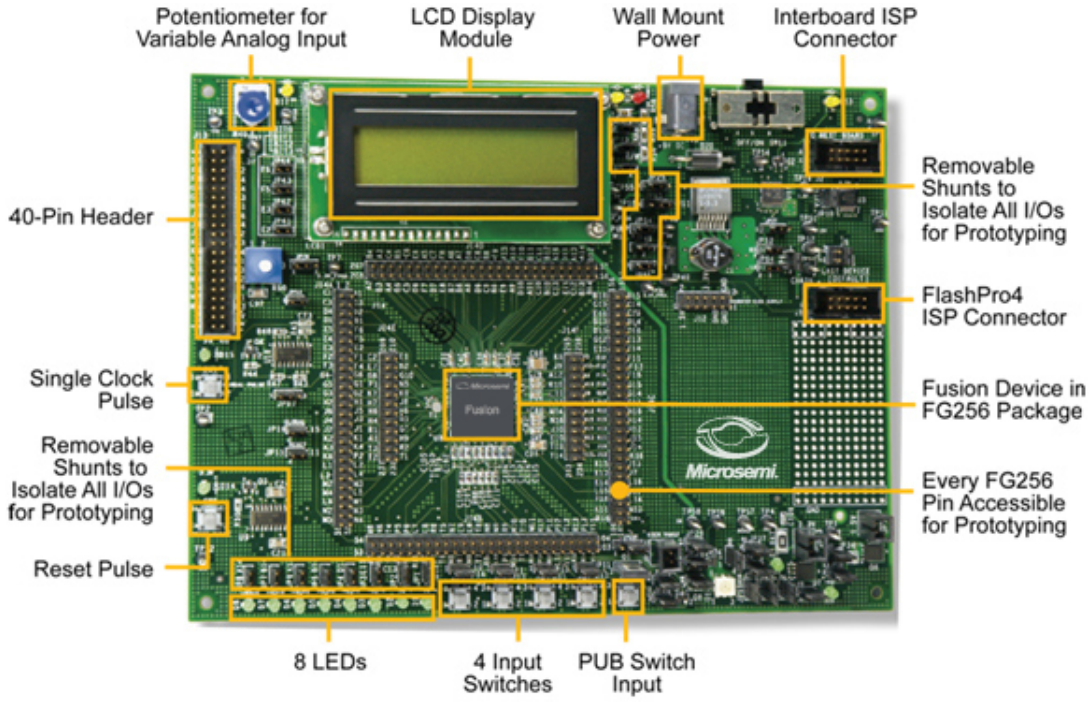
The following is a summary of the changes in revision 6.0 of this document.

- Updated chapter Introduction, page 2.
- Libero SoC software license information was updated from Gold to Silver. For more information, see Software Installation, page 3.

2 Introduction

This guide provides the information required to easily evaluate Fusion devices.

Figure 1 • **The Fusion Evaluation Board**



2.1 Kit Contents

The following table lists the contents of the Fusion Starter Kit.

Table 1 • **Kit Contents**

Item	Quantity
Evaluation board with an AFS600-FG256 Fusion device	1
FlashPro4 programmer	1
9 V power supply with International adapters	1

3 Installation and Settings

This section provides information about software and hardware settings required to run the pre-programmed demo design in the Fusion Evaluation Board.

3.1 Software Installation

Download and install the latest release of Microsemi Libero® SoC v11.5 or later, from the Microsemi website and register for your free Silver license. For instructions on how to install Libero SoC and SoftConsole, see the *Libero Software Installation and Licensing Guide*.

3.2 Hardware Installation

FlashPro v4.1 or later is required to use the Fusion Starter Kit. For software and hardware installation instructions, see the *FlashPro for Software User Guide*.

3.3 Testing the Evaluation Board

Refer to Test Procedures for Board Testing, page 64.

3.4 Programming the Test File

To retest the evaluation board at any time, use the test program to reprogram the board. Use the `TOP_AFS.stp` file with an AFS600-FG256 fitted on the board.

This design is currently implemented for the AFS600 die size. For a device of a different size, it is possible to recompile the design into other device sizes. For information about retargeting the device, see the *Libero IDE User Guide*. The design files are available under https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/fusion/fusion-starter-kit#documents.

For instructions on programming the device using FlashPro v4.1, see the *FlashPro for Software User Guide*.

4 Hardware Components

This chapter describes the hardware components of the Fusion Evaluation Board.

4.1 Fusion Evaluation Board

The Fusion Evaluation Board consists of the following:

- Wall-mount power supply connector, with switch and LED indicator
- Jumpers to select either 1.5 V or 3.3 V for I/O Bank0 or Bank1
- 10-pin 0.1"-pitch programming connector compatible with Altera connections
- 40 MHz oscillator and two independent manual clock options for global reset and pulse
- Eight LEDs (driven by outputs from the device)
- Jumpers (allow disconnection of all external circuitry from the FPGA)
- Two monostable pulse generator switches (“global” and “reset”)
- Four switches (provide input to the device)
- Potentiometer for variable analog input
- Large alphanumeric LCD to facilitate detailed message outputs from the FPGA application
- Multicolor LED for illustrating PWM fan control and temperature measurement
- 1.5 V and 3.3 V MOSFET-driven fan control circuits with shrouded headers for external fans

For further information, refer to the following appendices:

- Appendix: FG256 Package Connections for AFS600 Devices, page 67
- Appendix: Board Schematics, page 78

4.2 Board Description and Usage

The Fusion Evaluation Board has various advanced features that are covered in later sections of this chapter. The Fusion architecture provides access to a one-chip flash FPGA solution containing both analog and digital components, including a built-in flash drive.

Note that the AFS600-FG256 Microsemi FPGA is soldered directly to the board. The Fusion Starter Kit board is available only in a directly soldered configuration. Socketed configurations are not available.

Full schematics are available on the Starter Kit at: https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/fusion/fusion-starter-kit#documents. The electronic schematics can be enlarged on screen to show more detail than will be shown when this manual is printed.

4.3 Power Supplies

A 9 V power supply is provided with the kit. There are two power supply components on the board to provide 1.5 V and 3.3 V to the Fusion FPGA. An additional +5 V voltage bank is provided for use by the LCD module and in illustrating an analog voltage input to the analog aspects of the Fusion Evaluation Board.

The external +9 V positive-center power supply provided to the board via connector J18 goes to a voltage regulator chip, U11. This regulator has been protected against application of a reverse supply voltage by a reverse polarity protection diode. As soon as the external voltage is connected to the board, the red “power applied” LED (D19, the only red LED on the board) illuminates to indicate that an external supply has been connected to the board. As soon as switch SW11 is moved to the ON position (to the right, as labeled on the board “OFF/ON”), the disabling ground signal is removed from pin 7 of U11, and the regulator begins to provide power at its output.

The U11 switching voltage regulator provides a dedicated 3.3 V supply at its output. The board's 3.3 V supply feeds a separate regulator that delivers 1.5 V via U15. Although all Fusion FPGAs can also support 1.8 V and 2.5 V I/O standards, these voltages are not provided on the Fusion Evaluation Board. The 1.5 V supply is required for the core voltage of the Fusion family, and the 3.3 V supply is required for extended I/O bank capability, such as for LVTTL. The presence of these voltages is indicated by two yellow LEDs (D13 for 1.5 V and D11 for 3.3 V) located at the top right of the board. Each LED is labeled with the voltage it represents and its component identifier. Both voltages are selectable on I/O banks 0

and 1 (the two northernmost banks on a Fusion device). Note that only the larger Fusion devices (AFS600 and AFS1500) have five I/O banks.

The 3.3 V supply can also be used to provide the VPUMP programming voltage. This VPUMP voltage may be provided to the chip during programming by connecting a FlashPro3 programmer to the J1 interface and selecting VPUMP from the FlashPro v4.1 (or later) programming software, and may also be provided directly to the chip from the board. The user simply leaves the JP54 jumper in place to apply the 3.3 V supply to the VPUMP pin (M12) of the FG256-packaged FPGA. If both FlashPro3 and the board are selected to provide VPUMP, the connection on the board will override; FlashPro3 will detect that a voltage is available, issue an information message in the programming software, and then tristate its VPUMP output pin, allowing the board to provide all the power.

The board must be powered up during programming, as the chip's core voltages must be provided and VJTAG must be detected by the FlashPro3 programmer before it can set its JTAG signal voltages to the right level. The value of VJTAG can be set to 1.5 V or 3.3 V on the board by setting the position of jumper JP27 to join pins 1 and 2 for 1.5 V and pins 2 and 3 for 3.3 V. It is recommended that VJTAG be left at 3.3 V on the Fusion Evaluation Board because an interboard buffer chip is used that has limited low-voltage capability and needs the higher setting of 3.3 V to ensure good signals at the output of the buffer chip array U3.

The LCD has its own dedicated 5 V power supply, all components of which, including the regulator U20, are mounted on the circuit board underneath the LCD module. A yellow LED (D17) representing 5 V supply availability is positioned at the top left of the board.

The external +9 V power supply is rated at 2.2 A maximum. On page 1 of the dedicated schematics and in Figure 61, page 81, it will be noted that the 3.3 V supply is rated at 5 A maximum. The derived power supply of 1.5 V is rated at 2 A maximum, and the LCD 5 V power supply is rated at 500 mA.

The components at U11 (LM2678S-3.3) and U20 (LM2674M-5.0) are rated for an input voltage range of +8 V to +40 V, so a wide range of power supplies may be used with the board with no worry of over-voltage conditions occurring from inadvertent usage of the wrong power supply. It is expected that the voltage provided will be positive at the center pin of connector J18 and grounded on the outside. There is protection on the Fusion Evaluation Board for reverse voltages to prevent damage, but correct polarity must be provided for the board to function. Note that greater heating of the regulator chips will occur with higher voltages. Microsemi recommends that only the included power suply or an equivalent substitute be used with the Fusion Starter Kit, as it has been rated for the Fusion Evaluation Board and any Microsemi daughter cards that may be attached to the board.

4.3.1 Daughter Card Power Supply Connections

Limited power may be supplied by the Fusion Evaluation Board to a daughter card. The connector for the daughter card (header J12) is shown on page 5 of the dedicated schematics and in Figure 64, page 84. All the FPGA voltages of 1.5 V and 3.3 V are provided to the daughter card via a 12-pin, 0.1"-pitch connector. The reason for 12 pins is that this is compatible with the 12 pins used on the ProASIC3 Starter Kits and makes the daughter cards potentially compatible between the kits. The voltages are arranged with no-connection pins interspersing the voltage pins to prevent use of a jumper to inadvertently short a supply rail to ground by connecting differing supply rails together. This is not to protect the power supply regulators, as these will go high-impedance when an over-voltage condition is detected, but to protect the FGPA from a higher voltage being unintentionally applied to the 1.5 V core. Three of the 12 pins are ground pins to provide more than sufficient current return capability for future Microsemi daughter cards that will work with the Fusion Evaluation Board. The remaining pins are no-connection to prevent accidental shorting.

4.3.2 Power Supplies and Chaining Boards Together

There is a special note to be made of VPUMP connections when chaining boards together. This is detailed here. Microsemi recommends that the reader, unless experienced with Microsemi Starter Kit boards, return to this section after reading Figure 4.4, page 6.

When joining multiple Fusion or ProASIC3 Starter Kit boards together via the chain programming connection, connect J2 on one board to J1 on the next board in the chain using a standard 10-pin, 0.1"-pitch programming cable. Ideally, twisted-pair ribbon cabling should be used for this connection. The length of the cable should be kept as short as possible, as multiple boards connected to form a JTAG

chain of Fusion and ProASIC3/E and/or ARM®-enabled Fusion or ProASIC3 devices will provide much greater noise pick-up and may degrade the TCK clock for devices remote from the FlashPro3 programmer. Microsemi recommends that VJTAG be set at 3.3 V to help with signal integrity when chaining boards together. On all boards the jumper at JP10, if connected, is used for providing VJTAG to a downstream board that needs to know what VJTAG setting is being used by your board (e.g., some arbitrary board of your own design that you wish to supply with the VJTAG voltage used by the Fusion component). In most normal cases, this shunt should be disconnected. The shunt normally in this location can be safely stored across pins 11 and 12 or 9 and 10 of the J12 daughter card power supply connector. For particularly long chains, the value of TCK used during programming should be reduced. The lowest value it can take is 1 MHz.

To date, only one revision of the Fusion Evaluation Board has been produced. This first version of the board is labeled REV1 next to the AFS-EVAL-BRD1 label on the board. If the Fusion Evaluation Board is connected in a chain to ProASIC3/E boards, the documentation relating to the ProASIC3/E board should be read in detail to determine the appropriate connection setting, depending on the version of the ProASIC3/E board being used. The following notes are only for the Fusion Evaluation Board.

4.3.2.1 Procedure for Rev1 Fusion Evaluation Boards

4.3.2.1.1 To determine if the board is a Rev1 board:

To identify a Rev1 board, examine the front of the board and look for the part number located just beneath the large Actel logo silkscreened on the board. The part number will be “AFS-EVAL-BRD1” followed by “REV1”.

4.3.2.1.2 To chain Rev1 boards together:

All boards, starting from the board nearest the FlashPro3 programmer, should have the shunt moved from the default location connecting pins 3 and 4 of the J5 header to connect pins 1 and 2 of the J5 header. On the board and schematic this is labeled “CHAIN” (pins 1 and 2) and “LAST DEVICE (DEFAULT)” (pins 3 and 4). Only the very last board in the chain should have the shunt remaining across pins 3 and 4 of the J5 connector.

When connecting these boards together via a connection from J2 of one board to J1 of another board, VPUMP will be connected from one board to another. When powering up one board with a connector in place, notice that the 1.5 V and 3.3 V LEDs will light on the board to which no power has been applied, and the FPGA on that board, if programmed, will start operating. This is clearly an inappropriate situation for a large chain of boards. This is caused by having connector JP54 supplying VPUMP to other boards in the chain, as VPUMP is itself connected to the 3.3 V supply output that is used to generate the other FPGA voltages on a board. To prevent VPUMP from being used as the 3.3 V supply, you should remove the shunt that is in place on the JP54 connector to force JP54 open-circuit. To prevent loss of the shunt, it may safely be stored on the J12 header for the daughter card power supply, as it is impossible to cause a short by joining any adjacent pins.

4.4 Programming the AFS-EVAL-BRD1 with a FlashPro3

The base board used for all Fusion starter kits is the AFS-EVAL-BRD1.

In an AFS EVAL KIT the Microsemi part number for the board is AFS-EVAL-BRD600-SA. The part number indicates that the board is fitted with an AFS600-FG256 part, directly soldered (-SA) to the board.

4.4.1 Connecting the FlashPro3 Programmer to the Board

Connect the FlashPro3 programmer to your computer via the USB cable. Follow the instructions in the *FlashPro for Software User Guide* to install the software and connect to the FlashPro3 programmer. The amber (yellow) power LED on the FlashPro3 should be illuminated at this stage. If it is not, recheck the procedure in the FlashPro user’s guide until you obtain a steady amber (yellow) power LED illumination.

Make sure the board power switch SW11 is in the OFF position and only the red board external power LED is illuminated on the board.

Connect the FlashPro3 programmer to the board via the 10-pin programming cable supplied with the programmer hardware. The connector to use on the board is labeled “FP3” and is the lower shrouded

and keyed header J1. The pin 1 location on the cable indicated by the red ribbon running along the side of the cable will be on the left side as it enters into the board. After connecting the FlashPro3 programmer, using the FlashPro software, select **Analyze Chain** from the **File** menu. If all is well, the appropriate device ID for the Fusion part will appear in the software display on the PC. If you suspect a JTAG communication issue, try changing the VJTAG voltage to 3.3 V using JP27.

4.4.2 Programming or Re-Programming the Example Design

On the Fusion Starter Kit CD, you will find a *Designer* directory containing a STAPL file for programming the target design. Select the *TOP_AFS.STP* file from the CD and use that as the STAPL file in the FlashPro v4.1 software. Clicking **PROGRAM** will erase, program, and verify the part. The total programming time is approximately 2 minutes and 30 seconds.

4.4.3 Jumpers for Isolating Switches and LEDs from the FPGA

The many jumpers on the Fusion Evaluation Board are provided to allow the user to disconnect various switch combinations or LEDs from the FPGA I/O banks.

The jumpers are shown in the schematic and are labeled on the top-layer silkscreen as JP*, where * is a number. All jumpers are also labeled with the FPGA I/O pin number to which they are connected, e.g., JP54, for 3.3 V connection of VPUMP to the FPGA, is labeled “M12”, which indicates that it is connected to pin M12. Similarly, SW4 has a jumper above it called JP14 that is labeled “C10”, indicating that SW4 is connected through to pin C10 of the FPGA when this jumper is in place.

Figure 2, page 8 shows the board’s silkscreen layer overlaid with a grid, and Table 2, page 9 describes the function of each jumper and its location.

By disconnecting jumpers JP11, JP12, JP13, and JP14, momentary push button switches SW1, SW2, SW3, and SW4, respectively, can be disconnected from the FPGA such that the I/O pins B11, A11, C11, and C10, respectively, may be used for other purposes. Disconnecting jumpers JP1–JP8 will disconnect LEDs D1–D8 from FPGA I/O pins B12, C13, E11, D11, B13, A13, B14, and A14, respectively.

Momentary push button switches SW5 and SW6, for applying a reset pulse and a global pulse, are connected via jumpers JP15 and JP16 to I/Os K11 and L15, respectively. Again, all labeling is clearly shown on the silkscreen.

The LCD also has associated jumpers for its data, namely JP41, JP42, JP43, and JP44, located on the top left side of the board. These are connected to I/O pins E2, E3, F5, and F6, respectively. The LCD control signals Enable, R/W, and RS are provided from I/O pins D3, E5, and D1 via jumpers JP47, JP45, and JP46, respectively.

4.4.4 Analog Circuitry Provided on the Board

A variety of analog inputs and outputs are provided on the Fusion Evaluation Board to show what Fusion can do as a single-chip solution. These components are detailed below and in Table 2, page 9, enumerating all possible connectivity. As with all other components, the FPGA pins may be disconnected from these components to allow the board to be used for other functions.

A potentiometer (R50) is provided on the board for simple user variation of analog input. This input is fed to the AV0 pad.

A multicolor LED, U1, is provided and has three individual color components that can be controlled by a set of AG pins (AG6 – Blue, AG7 – Orange, AG8 – Green). By using the analog outputs, PWM control as well as individual switch control can be effected. The multicolor LED is enabled with a p-channel MOSFET (Q5), where pad AG3 is connected to the gate of the MOSFET.

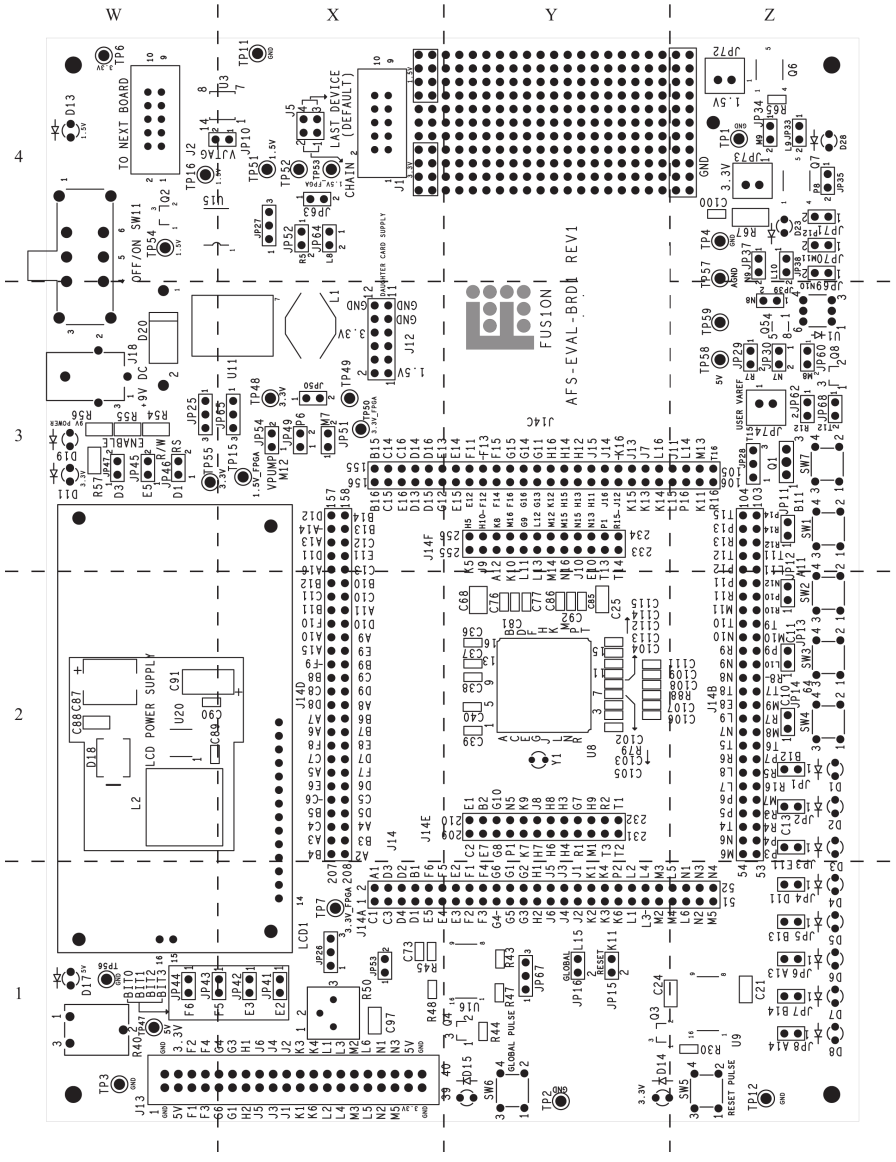
4.4.4.1 Motor Control

The Fusion Starter Kit board provides connections to two n-channel MOSFETs, Q6 and Q7, that are used to control current fed via the 1.5 V supply and the 3.3 V supply to an externally connected fan. Fans can be connected to the shrouded headers, JP72 and JP73, mounted on the board. An RC network is connected across each of these shrouded headers to filter out the back-EMF pulse that will occur when suddenly switching on or off a motor winding. Current is being measured via the AV and AC pads in each case by monitoring the voltage drop across a 0.1 Ω resistor (R62 for 1.5 V and R66 for 3.3 V) in each case. The AV and AC pads are tolerant to ±12 V DC; however, the voltage spike from a motor winding

being switched off will be much greater than this, so an RC “snubber” network is required to dampen such a voltage pulse and prevent it from reaching the FPGA inputs. Failure to apply an RC circuit across a motor when measuring the current through the field winding via direct connection to the FPGA will almost certainly result in voltages outside the maximum tolerance range of the FPGA’s analog inputs, which may result in catastrophic failure of the FPGA.

On the Fusion Evaluation Board, the n-channel MOSFETs are connected to a positive voltage supply. Because they are driven by the AG pads, their operation is inverse to normal. When AG pads on the FPGA are active, they float down or up to 0 V. When inactive they are tristated and switch off an n-channel MOSFET that is connected to the positive supply rail when activated. Normally, n-channel MOSFETs use the AG gate-drivers when the n-channel MOSFET is connected to a negative voltage supply. In this case, activating the AG gate-driver pad to 0 V will switch on the n-channel MOSFET.

Figure 2 • **Fusion Evaluation Board Top Silkscreen**



The following table lists jumper function listings and silkscreen grid locations.

Table 2 • **Jumper Function Listings and Silkscreen Grid Locations**

Jumper	Starter Kit Function	Notes	Grid Location
JP1	Disconnects green LED D1	Pin 1 to LED, pin 2 to FPGA B12	Z2
JP2	Disconnects green LED D2	Pin 1 to LED, pin 2 to FPGA C13	Z2
JP3	Disconnects green LED D3	Pin 1 to LED, pin 2 to FPGA E11	Z2
JP4	Disconnects green LED D4	Pin 1 to LED, pin 2 to FPGA D11	Z1
JP5	Disconnects green LED D5	Pin 1 to LED, pin 2 to FPGA B13	Z1
JP6	Disconnects green LED D6	Pin 1 to LED, pin 2 to FPGA A13	Z1
JP7	Disconnects green LED D7	Pin 1 to LED, pin 2 to FPGA B14	Z1
JP8	Disconnects green LED D8	Pin 1 to LED, pin 2 to FPGA A14	Z1
JP9	– No such jumper –	–	–
JP10	Enables VJTAG downstream to next board	Pin 1 to VJTAG of FPGA, pin 2 to programming header J2 pin 6 for next board	W4 and X4
JP11	Disconnects SW1	Pin 1 to switch, pin 2 to FPGA B11	Z3
JP12	Disconnects SW2	Pin 1 to switch, pin 2 to FPGA A11	Z2
JP13	Disconnects SW3	Pin 1 to switch, pin 2 to FPGA C11	Z2
JP14	Disconnects SW4	Pin 1 to switch, pin 2 to FPGA C10	Z2
JP15	Disconnects one-shot pulse initiated by SW5	Pin 1 to U9 pin 13, pin 2 to FPGA K11	Y1
JP16	Disconnects one-shot pulse initiated by SW6	Pin 1 to U16 pin 13, pin 2 to FPGA L15	Y1
JP17	– No such jumper –	–	–
JP18	– No such jumper –	–	–
JP19	– No such jumper –	–	–
JP20	– No such jumper –	–	–
JP21	– No such jumper –	–	–
JP22	– No such jumper –	–	–
JP23	– No such jumper –	–	–
JP24	– No such jumper –	–	–
JP25	Selects value of VMV1	Pin 1 is 1.5V_FPGA, pin 2 is VMV1, pin 3 is 3.3V_FPGA	W3
JP26	Selects value of VMV0	Pin 1 is 1.5V_FPGA, pin 2 is VMV0, pin 3 is 3.3V_FPGA	X1
JP27	VJTAG voltage selection	Pin 1 is 1.5 V, pin 2 is VJTAG, pin 3 is 3.3 V	X4
JP28	Determines whether 1.5 V is internally generated or externally generated	Pin 1 is 1.5V_INT, pin 2 is 1.5 V, pin 3 is 1.5V_EXT	Z3
JP29	Disconnects AV3	Pin 1 is TP58 (5.0 V), pin 2 is AV3_FLT (filtered to R7)	Z3
JP30	Disconnects AC3	Pin 1 is TP59, pin 2 is AC3_FLT (filtered to N7)	Z3

Table 2 • Jumper Function Listings and Silkscreen Grid Locations *(continued)*

Jumper	Starter Kit Function	Notes	Grid Location
JP31	– No such jumper –	–	–
JP32	– No such jumper –	–	–
JP33	Disconnects AV4	Pin 1 is 1.5 V, pin 2 is AV4_FLT (filtered to L9)	Z4
JP34	Disconnects AC4	Pin 1 is JP72 pin 1 for external 1.5 V fan, pin 2 is AC4_FLT (filtered to M9)	Z4
JP35	Disconnects AG4	Pin 1 is gate of n-channel MOSFET Q6 for 1.5 V fan, pin 2 is AG4 (P8)	Z4
JP36	– No such jumper –	–	–
JP37	Disconnects AV5	Pin 1 is 3.3 V, pin 2 is AV5_FLT (filtered to N9)	Z4
JP38	Disconnects AC5	Pin 1 is JP73 pin 1 for external 1.5 V fan, pin 2 is AC5_FLT (filtered to L10)	Z4
JP39	Disconnects AG5	Pin 1 is gate of n-channel MOSFET Q7 for 3.3 V fan, pin 2 is AG5 (N8)	Z3
JP40	– No such jumper –	–	–
JP41	Disconnects LCD data Bit3	Pin 1 is MDL14 – Bit3, pin 2 is FPGA E2	X1
JP42	Disconnects LCD data Bit2	Pin 1 is MDL13 – Bit2, pin 2 is FPGA E3	X1
JP43	Disconnects LCD data Bit1	Pin 1 is MDL12 – Bit1, pin 2 is FPGA F5	W1
JP44	Disconnects LCD data Bit0	Pin 1 is MDL11 – Bit0, pin 2 is FPGA F6	W1
JP45	Disconnects LCD control R/W	Pin 1 is MDL5 – R/W, pin 2 is FPGA E5	W3
JP46	Disconnects LCD control RS	Pin 1 is MDL4 – RS, pin 2 is FPGA D1	W3
JP47	Disconnects LCD control ENABLE	Pin 1 is MDL6 – ENABLE, pin 2 is FPGA D3	W3
JP48	– No such jumper –	–	–
JP49	Disconnects AV1	Pin 1 is TP48 (3.3 V), pin 2 is AV1_FLT (filtered to P6)	X3
JP50	Disconnects TP48 and TP49	Allows ammeter to be connected between TP48 and TP49 to measure 3.3V_FPGA current	X3
JP51	Disconnects AC1	Pin 1 is TP59, pin 2 is AC1_FLT (filtered to M7)	X3
JP52	Disconnects AV2	Pin 1 is TP51 (1.5V), pin 2 is AV2_FLT (filtered to R5)	X4
JP53	Disconnects AV0 from potentiometer R50	Pin 1 is center of R50 potentiometer, pin 2 is AV0_FLT (filtered to M6)	X1
JP54	Disconnects 3.3V_FPGA from VPUMP	Pin 1 is VPUMP (M12), pin 2 is 3.3V_FPGA	X3
JP55	– No such jumper –	–	–
JP56	– No such jumper –	–	–
JP57	– No such jumper –	–	–
JP58	– No such jumper –	–	–
JP59	– No such jumper –	–	–

Table 2 • **Jumper Function Listings and Silkscreen Grid Locations *(continued)***

Jumper	Starter Kit Function	Notes	Grid Location
JP60	Disconnects AG3 from multicolor LED	Pin 1 is gate of p-channel MOSFET Q5, pin 2 is AG3 (M8)	Z3
JP61	– No such jumper –	–	–
JP62	Disconnects AT9	Pin 1 is base-collector of temperature diode, pin 2 is AT9 (R12)	Z3
JP63	Disconnects TP51 and TP52	Allows ammeter to be connected between TP51 and TP52 to measure 1.5V_FPGA current	X4
JP64	Disconnects AC2	Pin 1 is TP53, pin 2 is AC2_FLT (filtered to L8)	X4
JP65	Selects value of VCCPLB	Pin 1 is 1.5V_FPGA, pin 2 is VCCPLB (B15), pin 3 is GND	X3
JP66	– No such jumper –	–	–
JP67	Selects value of VCCPLA	Pin 1 is 1.5V_FPGA, pin 2 is VCCPLA (B2), pin 3 is GND	Y1
JP68	Disconnects ARTN4	Pin 1 is emitter of temperature diode, pin 2 is ARTN4 (T12)	Z3
JP69	Disconnects AG6 from Blue	Pin 1 is tricolor LED U1 pin 1 (blue), pin 2 is AG6 (N10)	Z3 and Z4
JP70	Disconnects AG7 from Orange	Pin 1 is tricolor LED U1 pin 2 (orange), pin 2 is AG7 (M11)	Z4
JP71	Disconnects AG8 from Green	Pin 1 is tricolor LED U1 pin 3 (green), pin 2 is AG8 (P12)	Z4
JP72	Shrouded header for 1.5 V fan	Pin 1 is 1.5 V, pin 2 is drain of n-channel MOSFET Q6	Z4
JP73	Shrouded header for 3.3 V fan	Pin 1 is 3.3 V, pin 2 is drain of n-channel MOSFET Q7	Z4
JP74	Shrouded header for user-supplied VAREF	Pin 1 is VAREF (T15), pin 2 is GND	Z3

4.4.4.2 Test Points

All test points on the board are fitted with small test loops. These test points are labeled on the silkscreen as TP1, TP2, etc. All such test points are also labeled on the silkscreen with the voltage expected to be observed at that test point. Voltages will be one of 5.0 V, 3.3 V, 1.5 V, or GND. When measuring the voltage at a test point with a digital voltage multimeter (DVM) the ground lead should be connected to a test point labeled GND and the voltage lead should be connected to the voltage to be tested. All voltage labels on the board are relative to a 0 V ground reference or GND.

4.4.4.3 Prototyping Area

The prototyping area on the right side of the board has the bottom two rows of pins connected to ground, labeled as GND on the silkscreen and enclosed in a box, providing 16 holes connected to 0 V. The top two rows of pins are connected to various power supply rails internally in the board. They are grouped into rectangles of eight pins from left to right as follows: 3.3 V to the left and 1.5 V to the right, giving eight holes for each voltage level and six unconnected holes in the middle. All other holes in the prototyping area are unconnected and may be used to hold various discrete components, as needed for experimentation.

On the reverse side of the board there is an area labeled U5, which is a TQ100 pattern with some surrounding pads. This area may be used to solder a TQ100 part and then connect that part by adding

discrete wires to the pads and connecting them to desired pins on the board. The main purpose of this is to allow a previously programmed TQ100 device to be used to provide more system capability.

4.4.4.4 Layering on Board

The complete board design and manufacturing files are included on the Starter Kit CD. The board file is in Allegro format, which will allow an end user to create the appropriate Gerbers and other board views as needed. Pictures of the layers of the board are included in Appendix: Signal Layers, page 92. For your convenience, high-resolution PDFs of these layers are also provided on the Starter Kit CD.

The board is fabricated with six copper layers. The layers are arranged as follows from top to bottom:

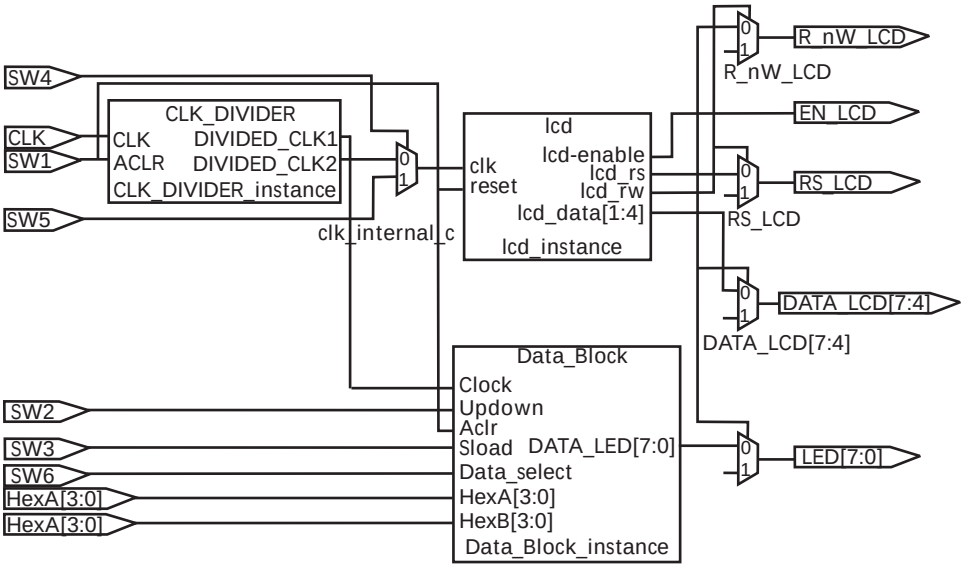
- Layer 1 – Top Signal Layer
- Layer 2 – Ground Plane (split into separate digital ground and analog ground joined at a single point)
- Layer 3 – Signal Layer 3
- Layer 4 – Signal Layer 4
- Layer 5 – Power Plane
- Layer 6 – Bottom Signal Layer

See the diagrams in Appendix: Signal Layers, page 92.

5 Description of Test Design

This is a description of the test design provided with the Fusion Starter Kit. The design contains a data generator block for LEDs, a clock divider, and an LCD block. A block diagram of the design is shown in the following figure.

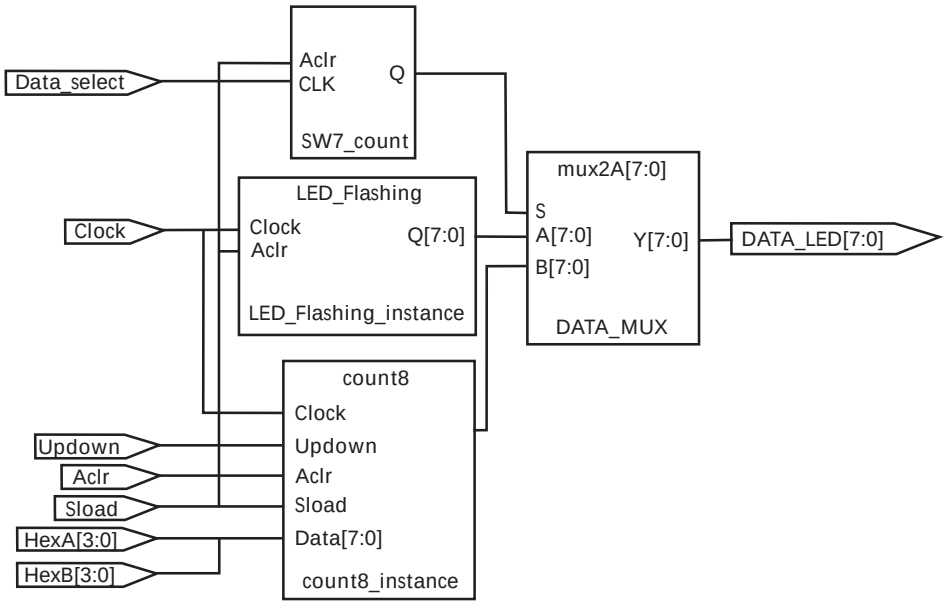
Figure 3 • **Design Block Diagram**



The clock divider divides the 40 MHz oscillator clock and sends the divided clock to the LCD module and the counter. The data generator (Data_Block) generates an 8-bit up/down counter and 8-bit flashing signal. The data generator output is displayed on the Fusion Evaluation Board LEDs. You can switch between the data using the SW6 signal. The counter has a synchronous load and an asynchronous clear.

A block diagram of Data_Block is shown in the following figure.

Figure 4 • **Data Block Diagram**



A message is generated and displayed on the Evaluation Board LCD. A state machine controls the LCD module.

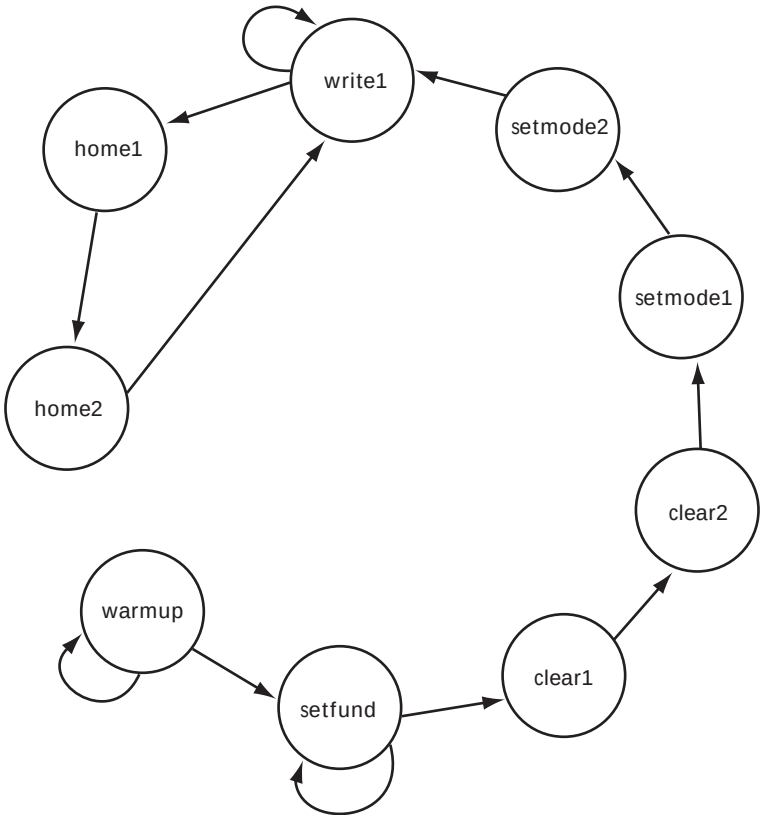
The following table gives a list of active switches on the board and the functions they perform.

Table 3 • **Switches**

Action	Results
Press SW1	Asynchronous clear for the whole design
Press SW2	Up/down control for the 8-bit counter. Press and hold SW2 for down count.
Press SW3	Synchronous load for the 8-bit counter. Press SW3 to load from the hex switches.
Press SW4	Switches between manual clock (SW5) and 40 MHz oscillator clock.
Press SW5	Manual clock (very useful for simulation)
Press SW6	Select for Data_Block. Allows switching LED output between the counter and flashing data.
Change hex switch setting (U13 and U14)	Changes the loaded data for the 8-bit counter.

The state diagram is shown in the following figure.

Figure 5 • **LCD State Diagram**



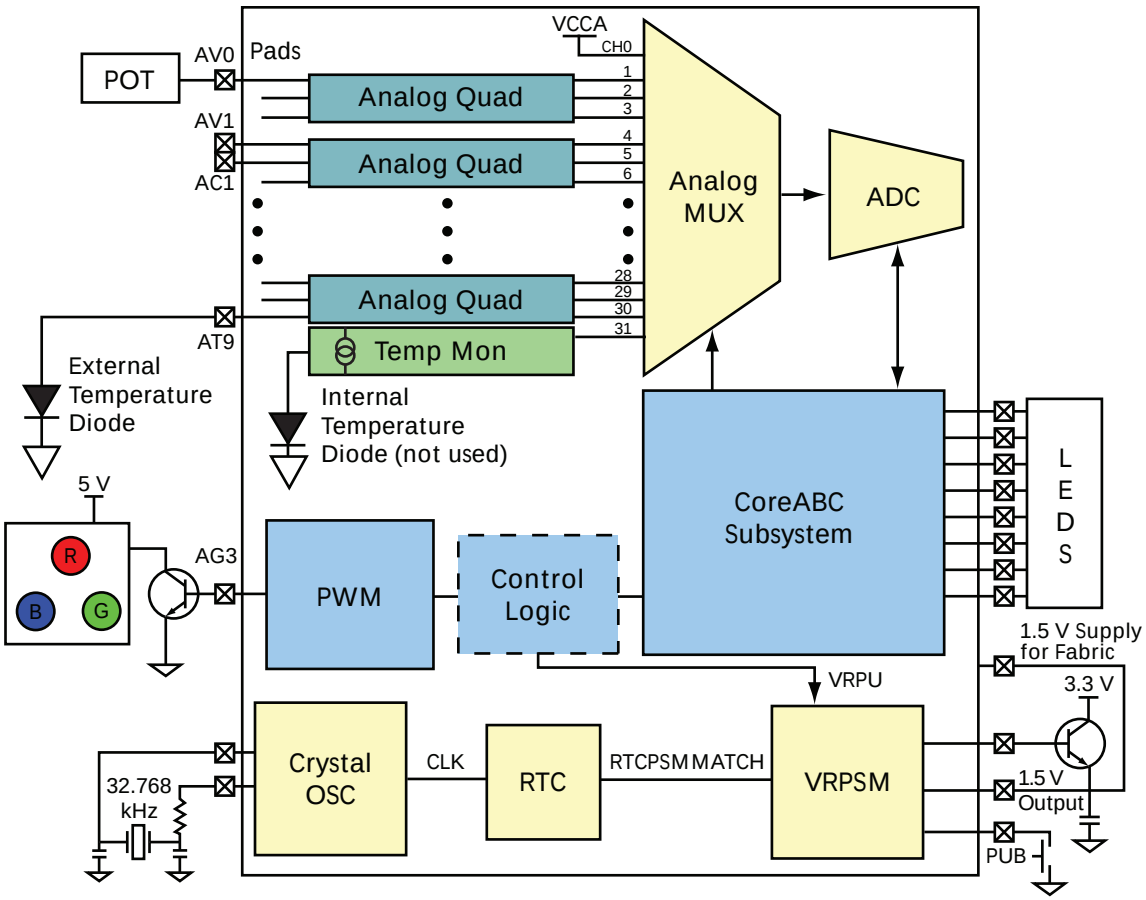
6 Demo Design Tutorial

This section demonstrates two possible implementations of the tutorial design. The first example is based on the Microsemi CoreABC (a flexible and fully programmable AMBA (Advanced Microcontroller Bus Architecture) Peripheral Bus Controller) and CoreAI intellectual property (IP) cores, which are freely available through the Microsemi CoreConsole IP Deployment Platform (IDP). The second example (SmartDesign Demonstration, page 38) implements the design in RTL with component macros generated from the Microsemi SmartGen core generator.

6.1 CoreABC Design Description

This demo design was created for the Microsemi Fusion Starter Kit. The 5 V, 3.3 V, and 1.5 V on-board power supplies are used in this design. Multiple analog input channels are utilized to sample the voltage and current provided to different loads. The design also samples the temperature through an on-board temperature sensor. Single-color LEDs are used to demonstrate the voltage threshold flags, and the tricolor LED is used to indicate different temperature levels with different colors.

Figure 6 • **CoreABC Demo Design Block Diagram**



6.1.1 Functionality Description

The following peripherals and functionality are exercised in the demo design:

6.1.1.1 Voltage Monitor

The demo design uses analog channel AV0 (pin M6) to monitor the voltage output from potentiometer R50. By changing the potentiometer, one can see the illumination status of LEDs D5–D8 change as the voltage output from the potentiometer changes. For details, refer to Table 4, page 16.

When the potentiometer is set to a different voltage level, the tricolor LED (U1) will blink at a different rate, from AV0 < 1.5 V, the slowest speed (1 Hz), to AV0 > 4.5 V, the fastest speed (always on).

6.1.1.2 Current Monitor

The following AV and AC pairs are used to monitor the voltage and current of various power supplies. For more details, refer to CoreABC Design Implementation, page 18.

- AV2 and AC2—AFS600 1.5 V power supply
- AV4 and AC4—1.5 V power supply for external load on board
- AV5 and AC5—3.3 V power supply for external load on board

Additionally, AV1 and AC1 can be used to monitor the 3.3 V AFS600 power supply current, and AV3 and AC3 can be used to monitor 5 V power supply current to the tricolor LED (U1).

6.1.1.3 Temperature Monitor

Channel AT9 is used in conjunction with an external temperature sensor to monitor the temperature of the Starter Kit environment. The tricolor LED (U1) will illuminate with different colors based on the temperature level detected.

- When temperature AT9 > 20°C, the LED illuminates blue.
- When temperature AT9 > 30°C, the LED illuminates green.
- When temperature AT9 > 40°C, the LED illuminates red.
- When temperature AT9 > 50°C, the LED illuminates white.

6.1.1.4 Sleep Mode Demonstration

The Real-Time Counter (RTC) is used in this demo to generate a power-on instruction (RTCPSMMATCH) to the Fusion internal voltage regulator. A 2-bit counter built into the control logic of the design generates a power-off instruction (VRPU) so the voltage regulator can be turned off from the Fusion fabric. With the RTC and the counter, one can test the Sleep Mode and wake-up of the Fusion device.

6.1.1.5 LCD

The LCD will show “Microsemi FUS1ON COREABC DEMO” after power-up.

The following table lists the different functionalities of the potentiometer, LEDs, and switches on the Fusion Starter Kit board for the demo design.

Table 4 • **Functionality of the Potentiometer, LEDs and Switches on the Fusion Evaluation Board**

On-Board Device	Jumper #	Pin #	Channel Name	Functionality
LED D5	JP5	B13	AV0	When AV0 > 1.5 V, D5 illuminated
LED D6	JP6	A13	AV0	When AV0 > 2.5 V, D6 illuminated
LED D7	JP7	B14	AV0	When AV0 > 3.3 V, D7 illuminated
LED D8	JP8	A14	AV0	When AV0 > 4.5 V, D8 illuminated
Potentiometer R50	JP53	M6	AV0	Turning the potentiometer drives AV0 with an analog voltage 0–5 V
Switch SW7	N/A	R15	N/A	Connects to the PUB pad directly. When depressed, the PUB pad is grounded to power-up the voltage regulator.
Switch SW6	JP16	L15	N/A	Inverted and connects to the active-low RESET signals of the counters, CoreABC Subsystem, and PLL.

Table 4 • **Functionality of the Potentiometer, LEDs and Switches on the Fusion Evaluation Board**

On-Board Device	Jumper #	Pin #	Channel Name	Functionality
Switch SW5	JP17	K11	N/A	Connects to the clock input of the 2-bit counter generating the power-off instruction. When depressed, a clock pulse is generated.
Switch SW4	JP14	C10	N/A	When depressed, the AFS600 core current is displayed on the LCD.
Switch SW3	JP13	C11	N/A	When depressed, the AFS600 core voltage is displayed on the LCD.
Switch SW2	JP12	A11	N/A	When depressed, the current temperature is displayed on the LCD.
Switch SW1	JP11	B11	N/A	When depressed, the potentiometer output voltage is displayed on the LCD.
Tricolor LED U1	JP69	AG6	AT9	When temperature AT9 > 20°C, the LED illuminates blue.
Tricolor LED U1	JP70	AG7	AT9	When temperature AT9 > 30°C, the LED illuminates green.
Tricolor LED U1	JP71	AG8	AT9	When temperature AT9 > 40°C, the LED illuminates red.

6.1.2 Demonstration Instructions

There are several special jumpers and pins on the Starter Kit that need attention. Select the appropriate jumper settings for the user design. The following table lists the basic functions of the jumpers.

Table 5 • **Special Jumper/Pin Settings and Their Functionality**

JP #/Pin #	Function	JP Setting	Value
JP25	VMV1	1–2	1.5 V
		2–3	3.3 V[1]
JP26	VMV0	1–2	1.5 V
		2–3	3.3 V[1]
JP27	VJTAG	1–2	1.5 V
		2–3	3.3 V[1]
JP28	PTEM	1–2	1.5 V_INT[1]
		2–3	1.5 V_EXT
Pin M15	TRSTB	Floating	JTAG operations
		Grounded	Allows voltage regulator power-down

1. Required for the Fusion Starter Kit Demo Design.

6.1.2.1 Exercising the Demo Design

To exercise the demo design:

1. Power on the Starter Kit using the power switch.
2. Turn on the fabric by pushing SW7 (this is only required if the TRSTB pin is grounded).
3. Test the voltage monitor by turning the potentiometer to observe whether D5–D8 turn on and off and whether the tricolor LED blinks at different rates.

4. Turn on Sleep Mode by turning off the fabric:
   - Press SW6 once to reset the system.
   - Press SW5 four times to generate a power-down signal.
5. Wake up the system via the RTC (at a preset time), or by pushing SW7.
6. Test the temperature indicator by warming the temperature diode (Q8) with a finger tip and then checking that the tricolor LED changes from blue to green to red (depending upon the initial room temperature, it may already be blue).
7. Press SW1 to show the potentiometer output voltage on the LCD.
8. Press SW2 to show the temperature sensed by Q8 on the LCD.
9. Press SW3 to show the AFS600 core voltage on the LCD.
10. Press SW4 to show the AFS600 core current on the LCD.

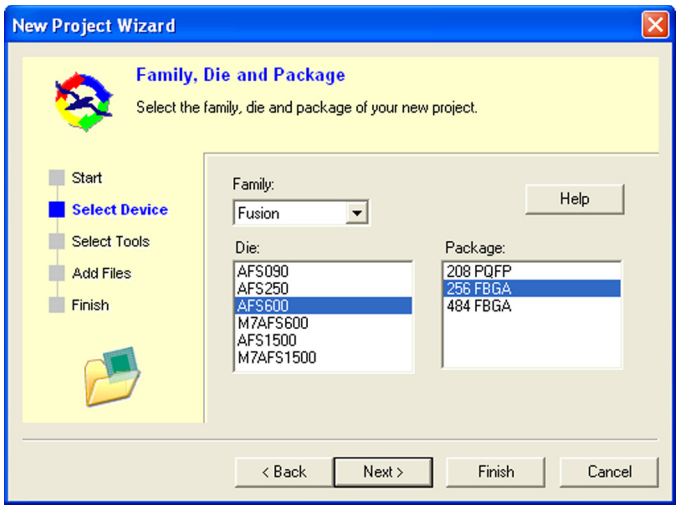
6.1.3 CoreABC Design Implementation

To implement the above functionalities, an integrated CoreConsole and Microsemi Libero Integrated Design Environment (IDE) project will need to be created with the configuration outlined in this chapter. For more details on creating the integrated CoreConsole and Microsemi Libero IDE project, see the *CoreConsole User Guide* and the *Libero IDE User Guide*.

6.1.3.1 Step 1 – Create an Integrated CoreConsole and Microsemi Libero IDE Project

Create a new Microsemi Libero IDE project by selecting **Fusion AFS600-FG256** and using CoreConsole and the SmartGen Macro Builder to generate the different functional macros; then instantiate them in the top-level design.

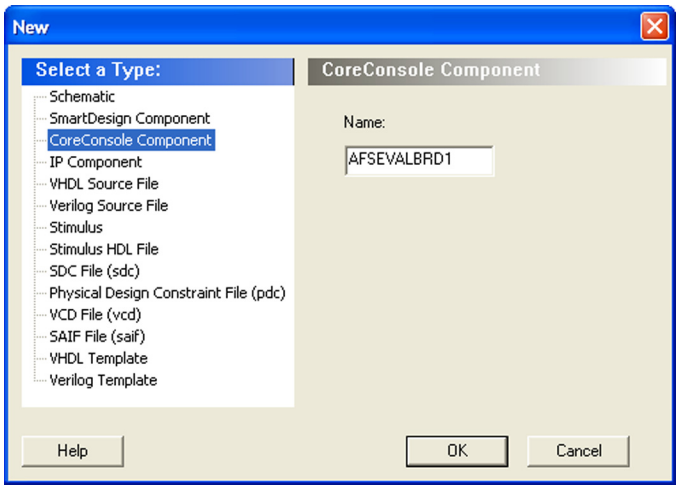
Figure 7 • **Microsemi Libero IDE New Project Wizard Device Selection**



6.1.3.2 Step 2 – Create a CoreConsole Project within Microsemi Libero IDE

From the Microsemi Libero IDE Project Flow, click the **CoreConsole Design Entry Tools** button to generate a new CoreConsole component with the name **AFSEVALBRD1**, as shown in the following figure. The end result of the CoreConsole component will yield the CoreABC Subsystem shown in Figure 6, page 15.

Figure 8 • **CoreConsole Component Creation Wizard**



6.1.3.2.1 Step 2.1 – CoreABC Instantiation and Configuration

From CoreConsole, instantiate and configure an instance of CoreABC through the **Parameters** tab shown in Table 6, page 19, Figure 9, page 21, and Figure 10, page 22. From the **Program** tab, copy and paste the source code provided in the *CoreABC_Source.txt* file included with the sample Libero IDE projects. CoreABC is the central controller in this application and is responsible for interfacing to the Analog Block (AB) and processing the results, as well as interfacing to the LCD.

Table 6 • **CoreABC Configuration Parameters**

Configuration Parameter Name		Value
Size Settings	APB Address Bus Width	10
	APB Data Bus Width	16
	Number of APB Slots	4
	Maximum Number of Instructions	512
	Z Register Size (bits)	14
	Number of I/O Inputs	4
	Number of I/O Flags	4
	Number of I/O Outputs	4
	Stack Size	32
Memory and Interrupt	Instruction Store	Soft (FPGA RAM)
	Internal Data/Stack Memory	Enabled
	ALU Operations from Memory	Enabled
	APB Indirect Addressing	Enabled
	Supported Data Sources	Accumulator and Immediate
	Interrupt Support	Disabled
	ISR Address	N/A

Table 6 • **CoreABC Configuration Parameters *(continued)***

Configuration Parameter Name		Value
Optional Instructions	AND, BITCLR, BITTST	Enabled
	XOR, CMP	Disabled
	OR, BITSET	Enabled
	ADD, SUB, DEC, CMPLEQ	Enabled
	INC	Disabled
	SHL, ROL	Enabled
	SHR, ROR	Enabled
	CALL, RETURN, RETISR	Enabled
	PUSH, POP	Enabled
	APBWRT ACM	Enabled
	IOREAD	Disabled
	IOWRT	Enabled
Optional Multiply Instruction	MULT	Not Implemented
Other Settings	Initialization Width	11
	Instance ID	N/A
	Verbose Simulation Log	Enabled
FPGA Family		Fusion
Testbench		User

Figure 9 • **CoreABC Configuration Dialog Box—Parameters Tab**

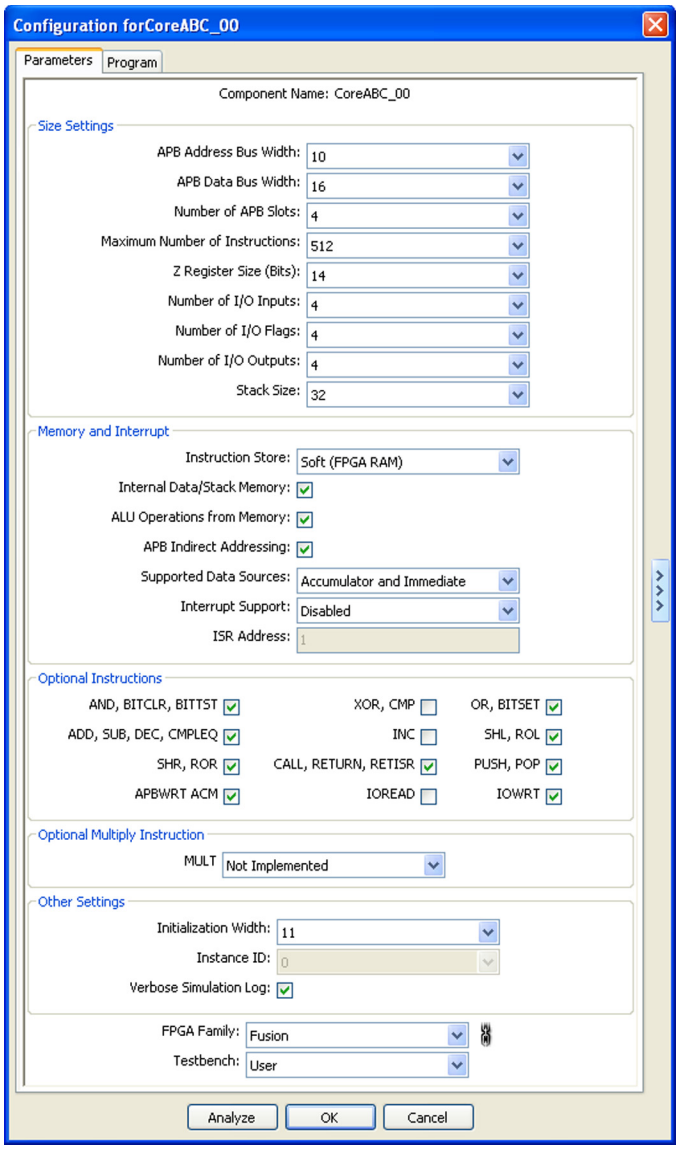
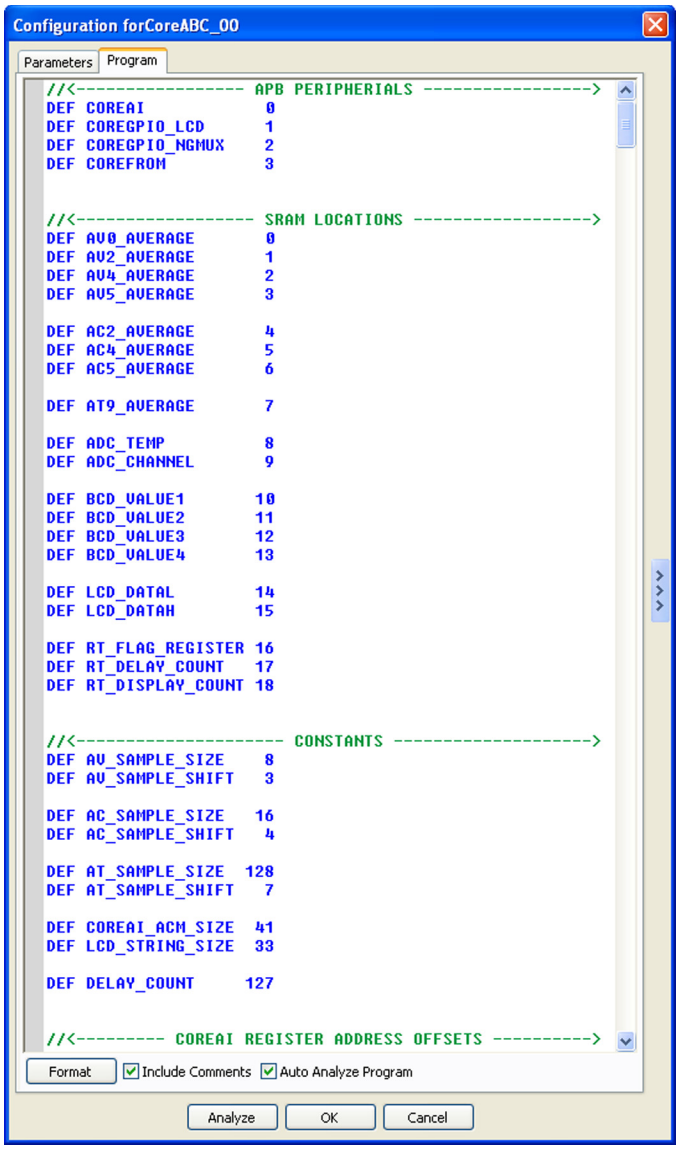


Figure 10 • **CoreABC Configuration Dialog Box—Program Tab**



6.1.3.2.2 Step 2.2 – CoreAI Instantiation and Configuration

From CoreConsole, instantiate and configure an instance of CoreAI as shown in Table 6, page 15 and Figure 11, page 25. CoreAI allows for the simple control of the Fusion analog peripherals via the industry-standard AMBA Advanced Peripheral Bus (APB) interface.

Table 7 • **CoreAI Configuration Parameters**

Configuration Parameter Name	Value
ACM Clock Divider	PCLK/4
Internal Temperature Monitor	Disabled
Interrupt Out Line	Disabled
Interrupt Output Polarity	N/A

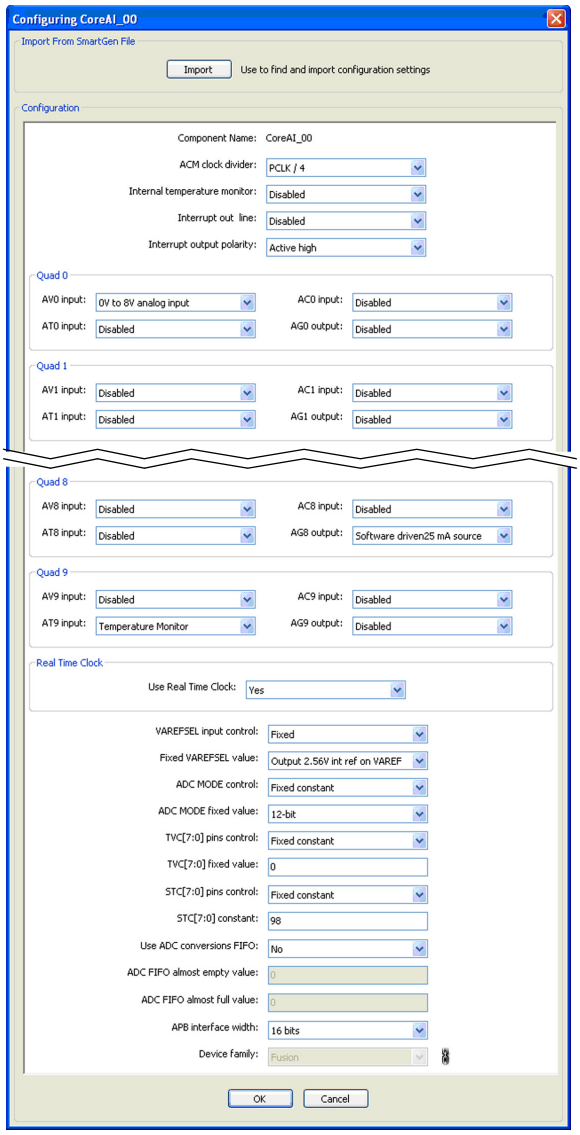
Table 7 • **CoreAI Configuration Parameters *(continued)***

Configuration Parameter Name		Value
Quad #0	AV0 Input	0 V to 8 V Analog Input
	AC0 Input	Disabled
	AT0 Input	Disabled
	AG0 Output	Disabled
Quad #1	AV1 Input	Disabled
	AC1 Input	Disabled
	AT1 Input	Disabled
	AG1 Output	Disabled
Quad #2	AV2 Input	0 V to 2 V Analog Input
	AC2 Input	Current Monitor
	AT2 Input	Disabled
	AG2 Output	Disabled
Quad #3	AV3 Input	Disabled
	AC3 Input	Disabled
	AT3 Input	Disabled
	AG3 Output	Hardware Driven 25 mA Source
Quad #4	AV4 Input	0 V to 2 V Analog Input
	AC4 Input	Current Monitor
	AT4 Input	Disabled
	AG4 Output	Software Driven 25 mA Source
Quad #5	AV5 Input	0 V to 4 V Analog Input
	AC5 Input	Current Monitor
	AT5 Input	Disabled
	AG5 Output	Software Driven 25 mA Source
Quad #6	AV6 Input	Disabled
	AC6 Input	Disabled
	AT6 Input	Disabled
	AG6 Output	Software Driven 25 mA Source
Quad #7	AV7 Input	Disabled
	AC7 Input	Disabled
	AT7 Input	Disabled
	AG7 Output	Software Driven 25 mA Source
Quad #8	AV8 Input	Disabled
	AC8 Input	Disabled
	AT8 Input	Disabled
	AG8 Output	Software Driven 25 mA Source

Table 7 • **CoreAI Configuration Parameters *(continued)***

Configuration Parameter Name		Value
Quad #9	AV9 Input	Disabled
	AC9 Input	Disabled
	AT9 Input	Temperature Monitor
	AG9 Output	Disabled
Real-Time Clock	Use Real-Time Clock	Yes
VAREFSEL Input Control		Fixed
Fixed VAREFSEL Value		Output 2.56 V Internal Voltage on VAREF
ADC Mode		Fixed Constant
ADC Mode Fixed Value		12-Bit
TVC[7:0] Pins Control		Fixed Constant
TVC[7:0] Fixed Value		0
STC[7:0] Pins Control		Fixed Constant
STC[7:0] Constant Value		98
Use ADC Conversion FIFO		No
ADC FIFO Almost Empty Value		N/A
ADC FIFO Almost Full Value		N/A
APB Interface Width		16-Bit
Device Family		Fusion

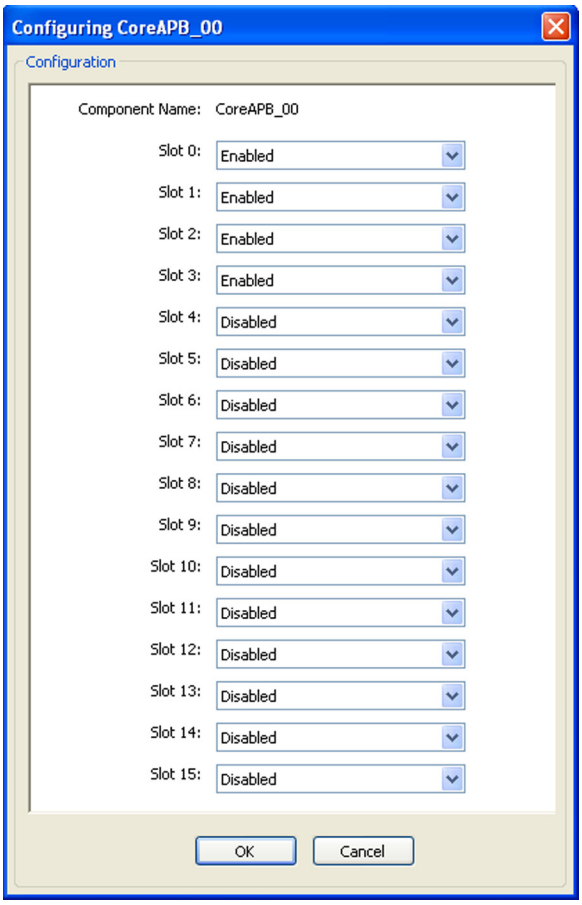
Figure 11 • **CoreAI Configuration Dialog Box**



6.1.3.2.3 Step 2.3 – CoreAPB Instantiation and Configuration

From CoreConsole, instantiate and configure an instance of CoreAPB, as shown in the following table. CoreAPB allows for communication between CoreABC and the various peripherals instantiated on the AMBA APB interface.

Figure 12 • **CoreAPB Configuration Dialog Box**



6.1.3.2.4 Step 2.4 – CoreGPIO and CoreFROM Instantiation

From CoreConsole, instantiate two CoreGPIO instances and one CoreFROM instance—no configuration of these instances is necessary. One of the two CoreGPIO instances is used to interface the control and data signals to the on-board LCD, and the other instance is used to allow runtime control of the NGMUX select line. The CoreFROM instance provides an AMBA APB interface to the embedded FROM (FlashROM) block within the Fusion device. The LCD default string is stored in the embedded FROM block.

6.1.3.2.5 Step 2.5 – Automatically Connecting Signals in CoreConsole

CoreConsole has the ability to automatically connect together standard interfaces for components. This is referred to as *Auto Stitching*. Many of the interfaces to standard components are well-defined and uniform, and permit unambiguous automatic connection. These include clock and reset lines, and AHB (Advanced High-Performance Bus) and APB connections.

First, perform a simple Auto Stitch and configure the dialog box, as shown in Figure 13, page 27. Taking careful note to set **APB:Slaves** correctly, as this defines the subsystem memory map, also make sure the **Top Level:Analog Pads** option is disabled, as the user will manually connect the necessary signals in a later step.

Next, perform an **Auto Stitch to Top Level** and configure the dialog box for the CoreABC instance, as shown in Figure 14, page 28. This quickly connects the component's signals to the top level of the subsystem without renaming the ports. The remainder of the signals will need to be manually connected, as the remaining ports require specific names in the top-level HDL file that will be used.

Figure 13 • **Auto Stitch Dialog Box**

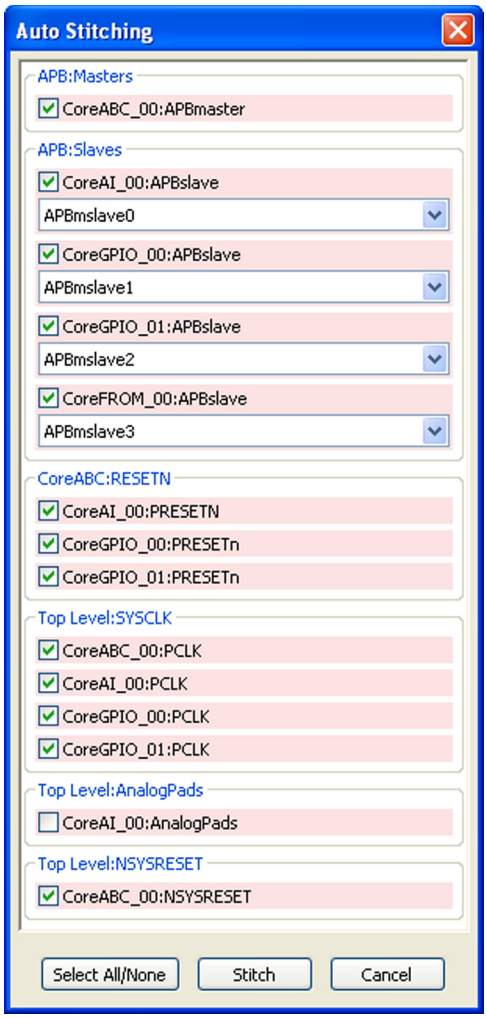
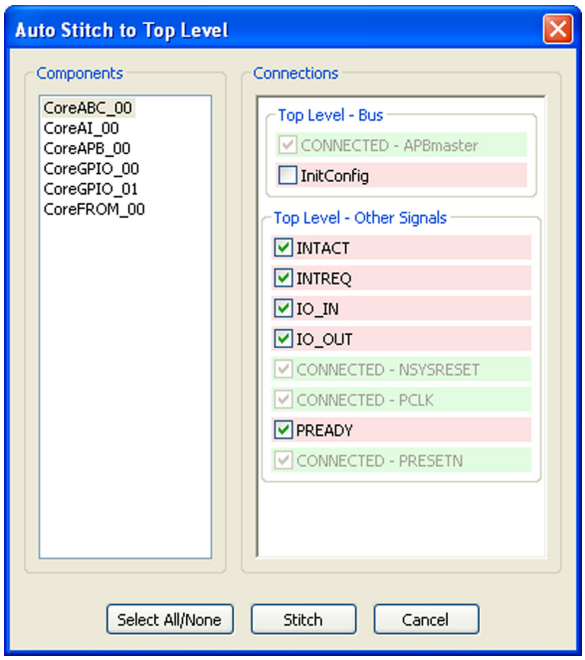


Figure 14 • **Auto Stitch to Top Level Dialog Box**



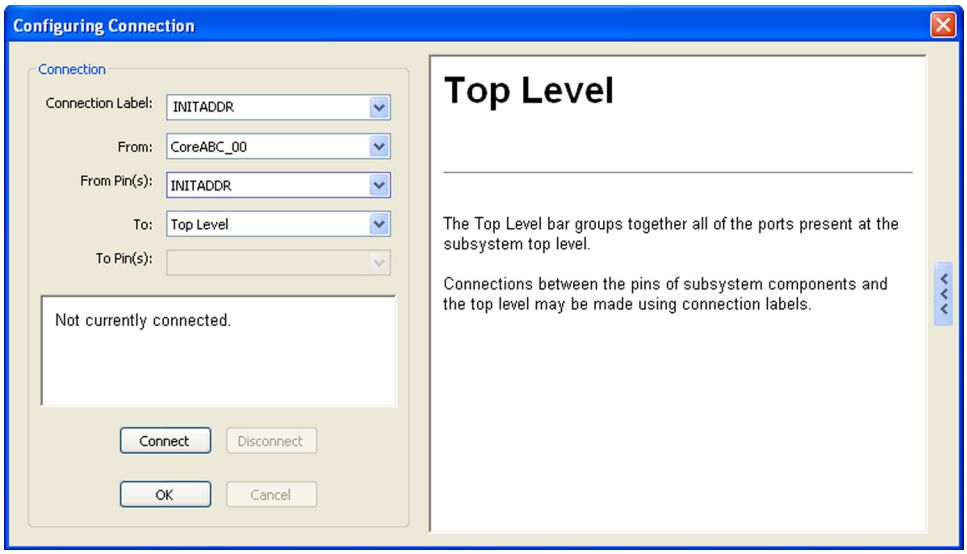
6.1.3.2.6 Step 2.6 – Manually Connecting Signals in CoreConsole

The remaining signals must be manually connected to the top level of the CoreABC subsystem with the exact name listed under the “Top Level Signal Name” heading in Table 8, page 29. To manually connect a signal in CoreConsole, perform the following steps from the **Configuring Connections** dialog box, as shown in Figure 15, page 29. Once all of the manual connections are established, the CoreConsole schematic should resemble the one shown in Figure 16, page 31.

To manually connect a signal CoreConsole:

1. Select the source component in the **From** list.
2. Select the source pin (or bus) in the **From Pin(s)** list (this can either be an input to or an output from the component).
3. A bus can be expanded by clicking the **+** sign to the left of the bus name.
4. Select the destination component or **Top Level** in the **To** list.
5. Select the destination pin in the **To Pin(s)** list (this can be either be an input, or an output from this component). This list only shows compatible pins. If the destination the user selects is **Top Level**, then **To Pin(s)** remains blank.
6. If connecting to a connection which does not already exist, enter a name for the **Connection Label**. If connecting to a previously existing connection, select the name from the **Connection Label** list.
   - If the **From** and **To** components and pins are compatible with the selected label, the **Connect** button becomes active.
   - If the **From** or **To** component or pins are not compatible with the selected label, a warning will display and the **Connect** button will be inactive.
   - If a bus connection is being made, **Connection Label** will be generated automatically.
7. After all selections are made and the connection is labeled, click the **Connect** button. The **Connect** and **OK** buttons remain unavailable until all selections and labels are correct. Only the **Connect** button establishes the connection. The **OK** button exits the dialog box but does not establish a connection.

Figure 15 • **Configuring Connection Dialog Box**



The following table lists the required component and top-level signal name.

Table 8 • **Required Component and Top-Level Signal Name**

Signal Location			
Component Name	**Bus Name**	**Signal Name**	**Top-Level Connection Label**
CoreABC_00	InitConfig	INITADDR	INITADDR
		INITDATA	INITDATA
		INITDATVAL	INITDATVAL
		INITDONE	INITDONE

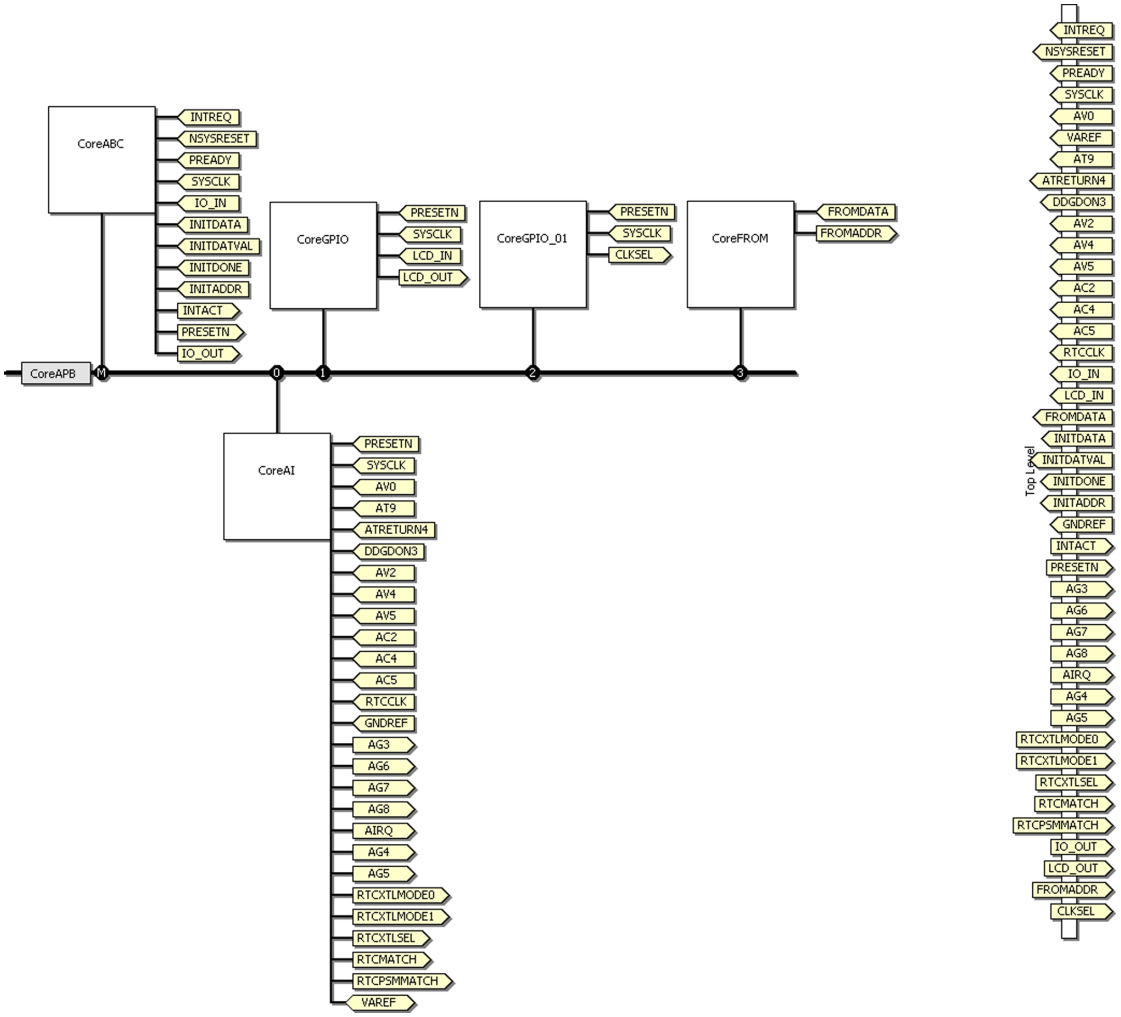
Table 8 • **Required Component and Top-Level Signal Name**

Signal Location			
Component Name	**Bus Name**	**Signal Name**	**Top-Level Connection Label**
CoreAI_00	AnalogPads	AV0	AV0
		AV2	AV2
		AC2	AC2
		AG3	AG3
		AV4	AV4
		AC4	AC4
		AG4	AG4
		AV5	AV5
		AC5	AC5
		AG5	AG5
		AG6	AG6
		AG7	AG7
		AG8	AG8
		AT9	AT9
		ATRETURN4	ATRETURN4
		VAREF	VAREF
		GNDREF	GNDREF
	DDGDON	DDGDON3	DDGDON3
	RTC	RTCCLK	RTCCLK
		RTCXTLMODE0	RTCXTLMODE0
		RTCXTLMODE1	RTCXTLMODE1
		RTCXTLSEL	RTCXTLSEL
		RTCMATCH	RTCMATCH
		RTCPSMMATCH	RTCPSMMATCH
		INTERRUPT	AIRQ
CoreGPIO_00		dataIn	LCD_IN
		dataOut	LCD_OUT
CoreGPIO_01		dataOut	CLKSEL

Table 8 • **Required Component and Top-Level Signal Name**

Signal Location			
Component Name	**Bus Name**	**Signal Name**	**Top-Level Connection Label**
CoreFROM		fromADDR	FROMADDR
		fromDATA	FROMDATA

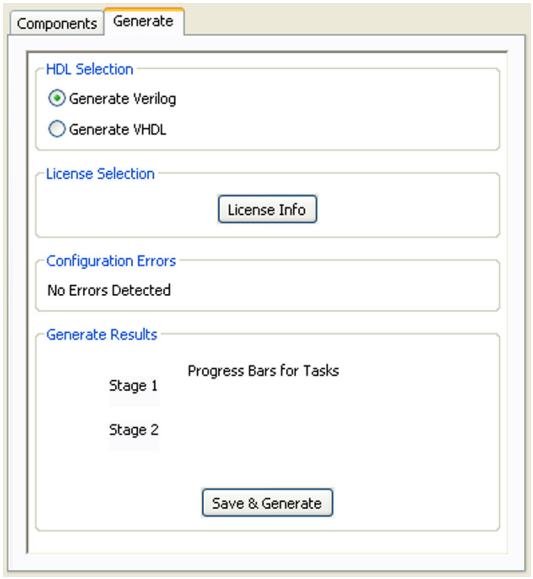
Figure 16 • **CoreABC Subsystem CoreConsole Schematic**



6.1.3.2.7 Step 2.7 – Saving and Generating the CoreConsole Design

The final step within CoreConsole is saving and generating HDL for Microsemi Libero IDE. Switch to the **Generate** tab and select either **Verilog** or **VHDL** as the desired language, then click the **Save & Generate** button. Once generation is completed, CoreConsole may be closed, and the AFSEVALBRD1 component will now be present and accessible within Microsemi Libero IDE.

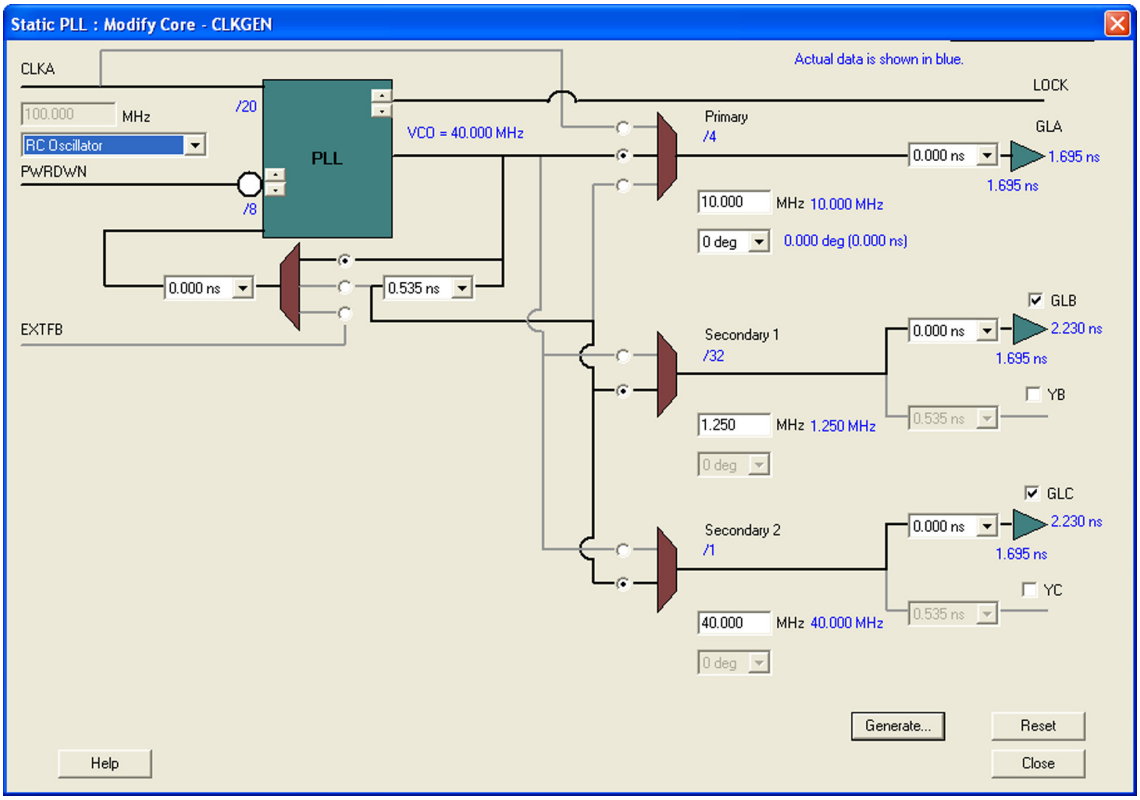
Figure 17 • **CoreConsole Generate Tab**



6.1.3.3 Step 3 – Generate the PLL Macro (CLKGEN)

In the SmartGen Cores Catalog, select **Static PLL** from the **Clock Conditioning/PLL** category, as shown in the following figure. Choose **RC Oscillator** as the input clock source. The PLL (CLKGEN) output clocks are 10 MHz, 1.25 MHz, and 40 MHz for GLA, GLB, and GLC, respectively. Once configured, click the **Generate** button and set the **Core Name** to **CLKGEN**.

Figure 18 • **Create the PLL Macro (CLKGEN)**



6.1.3.3.1 Step 4 – Generate the RAM Initialization Macro (INITBLK)

In the SmartGen Cores Catalog, select **Flash Memory System Builder** from the **Flash Memory System Builder** category, as shown in Figure 19, page 33. Select the **Initialization** client and click the **Add to System** button. Configure the client as shown in Figure 20, page 34. Once configured, click the **Generate** button and use the Core Name **INITBLK**.

Note: The full path to the Memory Contents File is *C:\Actel\AFSEVALBRD1\coreconsole\common\COREABC\software\CoreABC_00\RAMABC_0.mem* assuming the default location for the *Actelprj* directory.

Figure 19 • **Flash Memory System Builder Creation Dialog Box**

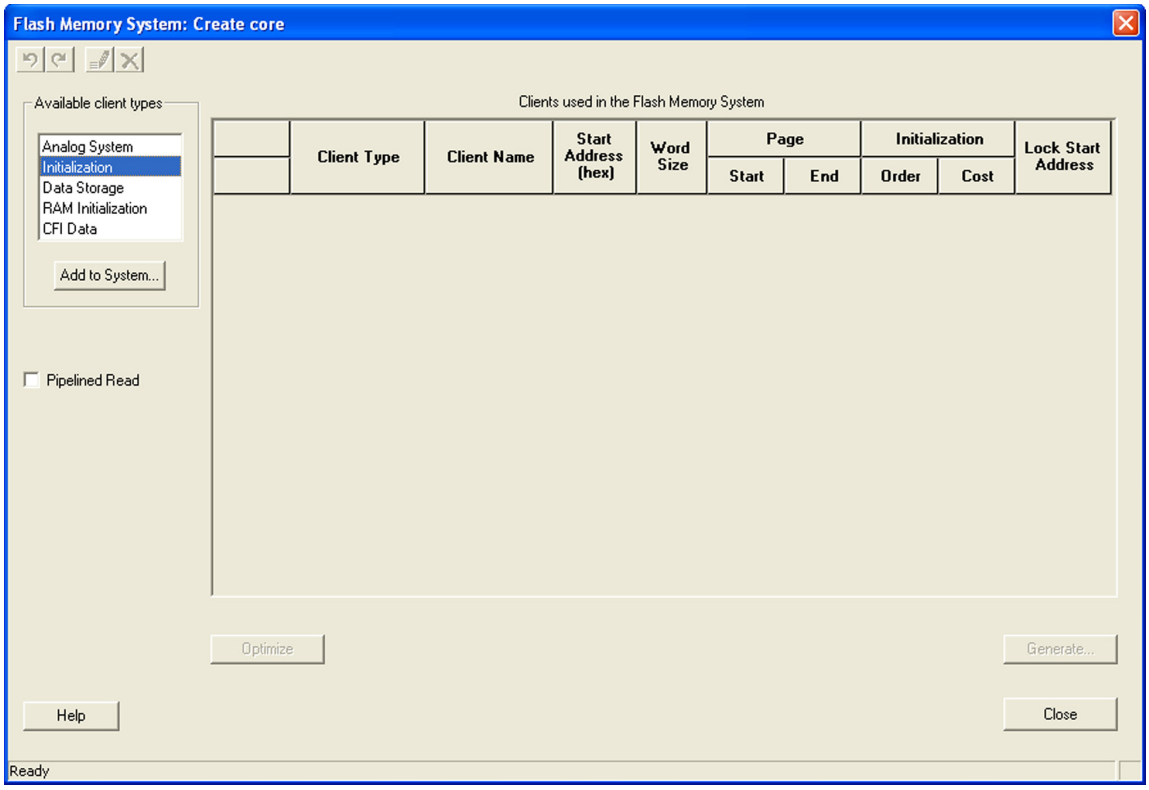
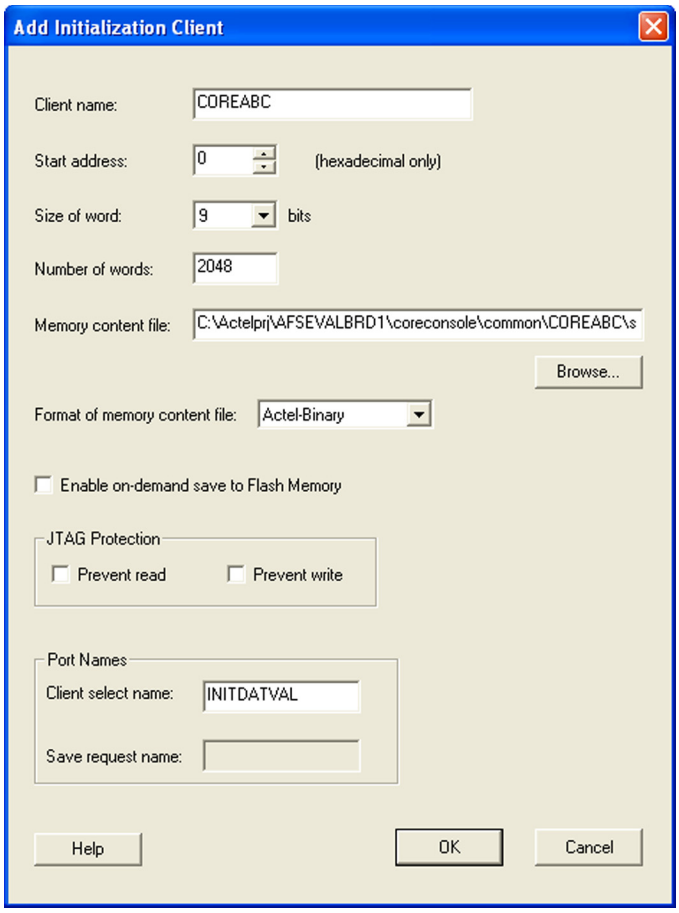


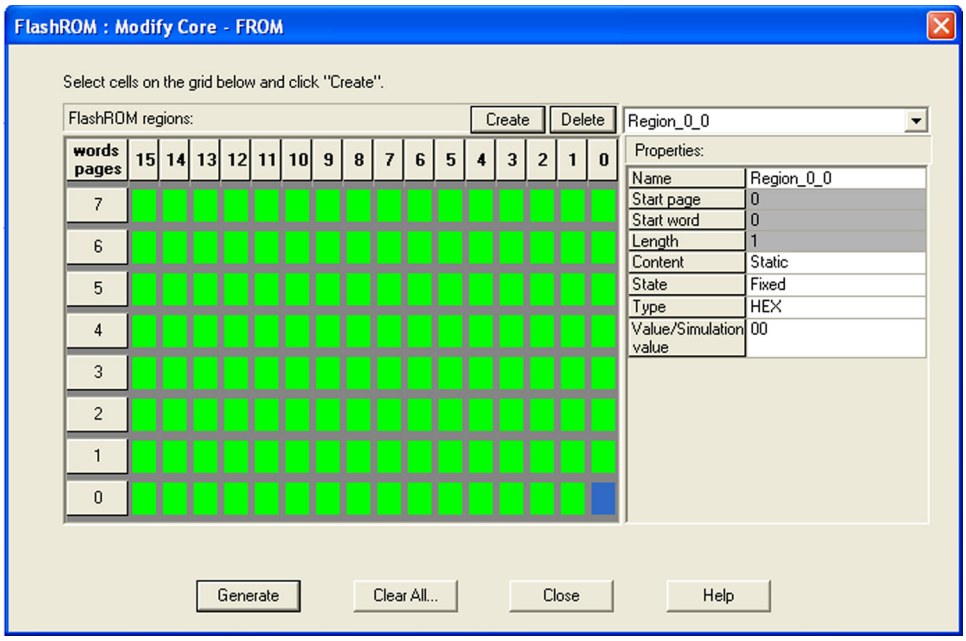
Figure 20 • **Initialization Client Configuration**



6.1.3.4 Step 5 – Import/Generate the FROM Macro

From the **File** menu in Microsemi Libero IDE, select **Import Files** and navigate to the provided *FROM.GEN* file. Once the FROM macro has been imported, regenerate the macro to ensure it is up to date.

Figure 21 • **FROM Macro Configuration**



6.1.3.5 Step 6 – Create Top-Level and Testbench

After generating the major function blocks, a top-level wrapper needs to be created, along with a testbench to simulate and verify the functionality of the design. For details on how to create the top-level wrapper and testbench, see the *Fusion Design Flow Tutorial*. A sample top-level wrapper and testbench (in both Verilog and VHDL) are provided in the sample Microsemi Libero IDE projects. The project files can be found in *AFS-EVAL-BRD1-COREABC.ZIP*.

6.1.3.6 Step 7 – Synthesis and Place-and-Route

After the functional simulation has completed, synthesis and place-and-route can be performed. Run simulation for each stage of the design.

Note: The instruction log for CoreABC will not be displayed during post-synthesis or post-layout simulations, even though it was displayed during pre-synthesis simulations.

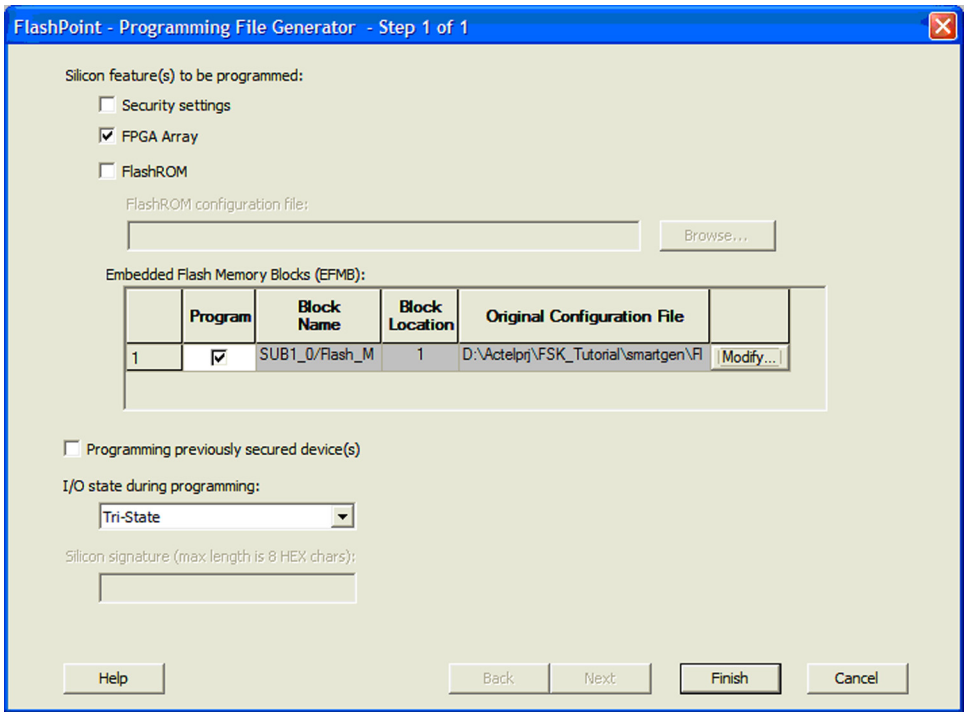
6.1.3.7 Step 8 – Generate a Programming File

Once the back-annotated simulation has completed, a PDB (or STAPL) file can be generated.

To generate a PDB Programming File:

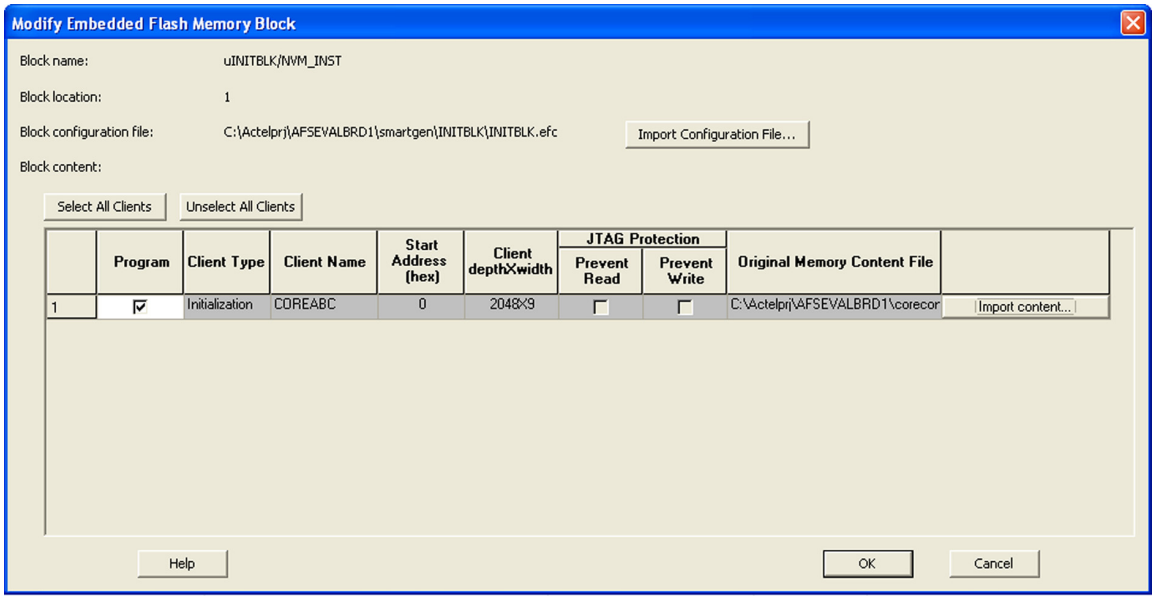
1. Click the **Programming File** icon in Designer. The dialog box shown in the following figure will appear.

Figure 22 • **Generating the Fusion Programming File**



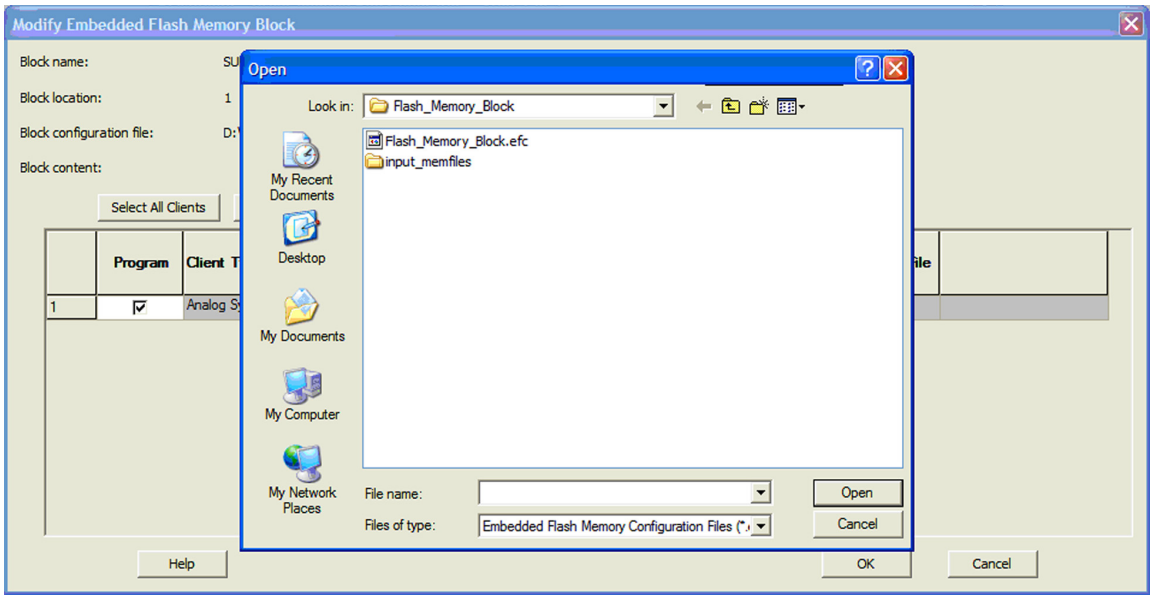
2. Enable FlashROM programming and load the FlashROM UFC configuration file located in the *<ProjectFolder>\smartgen\FROM* directory, as shown in the preceding figure. This will generate a PDB (or STAPL) file that will program the FlashROM and the FPGA.
3. Enable the programming of the embedded flash memory blocks by clicking the **Modify** button. The Modify Embedded Flash Memory Block dialog box appears, as shown in the following figure.

Figure 23 • **Flash Memory Block Configuration**



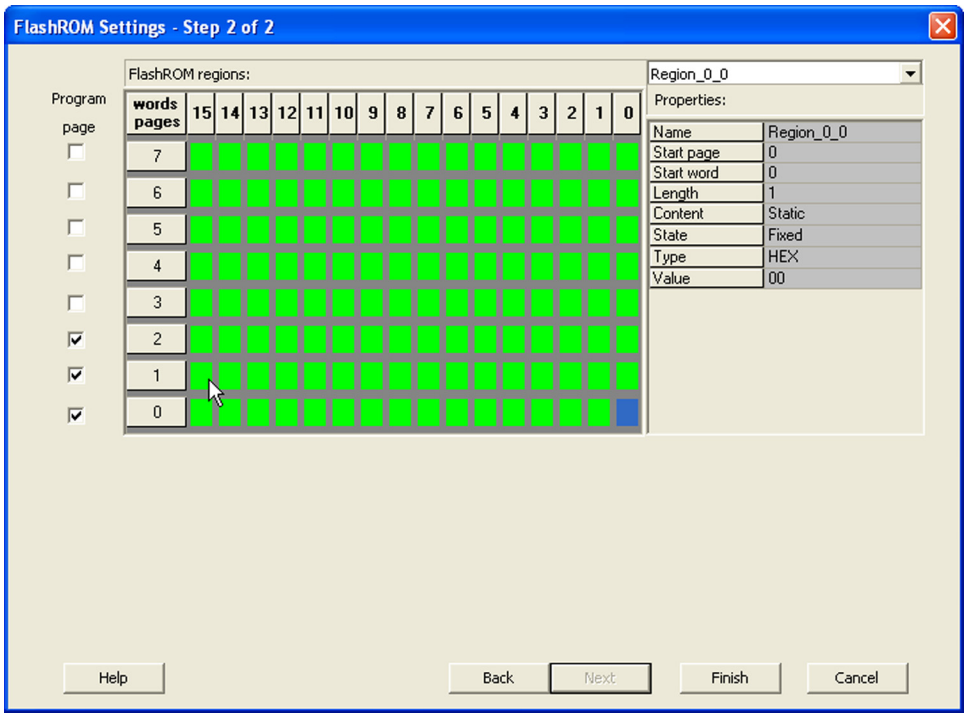
4. Click the **Import Configuration File** button and load the EFC file from the *<ProjectFolder>\smartgen\INITBLK* directory, as shown in the following figure. Click the **OK** button to return to the FlashPoint – Programming File Generator dialog box, and enable programming by selecting the check box in the **Program** column if it isn't already selected. Then click the **Next** button.

Figure 24 • **Loading the EFC File**



5. Enable the programming of FlashROM Pages 0 through 2 by selecting the check box in the **Program Page** column, as shown in the following figure. Click **Finish**. A PDB (or STAPL) file will be generated.

Figure 25 • **FlashROM Settings**



6.1.3.8 Step 9—Program the AFS600 on the Fusion Evaluation Board

Connect the FlashPro3 programmer to the Fusion Evaluation Board programming header (J1). Power up the board and follow the instructions in the *FlashPro for Software User Guide* to program the AFS600.

Up to this point, the user has created the Fusion Evaluation Board Demo Design based on CoreABC to demonstrate the following peripherals and functionality:

1. Analog System Block
   Voltage Monitor
   Current Monitor
   Temperature Monitor
   Gate Drivers
   Real-Time Counter
2. Embedded Flash Memory Block (for RAM initialization)
3. FlashROM (for constants storage)
4. Internal RC Oscillator
5. Crystal Oscillator
6. PLL
7. Fusion FPGA Fabric
8. GPIO
9. LCD

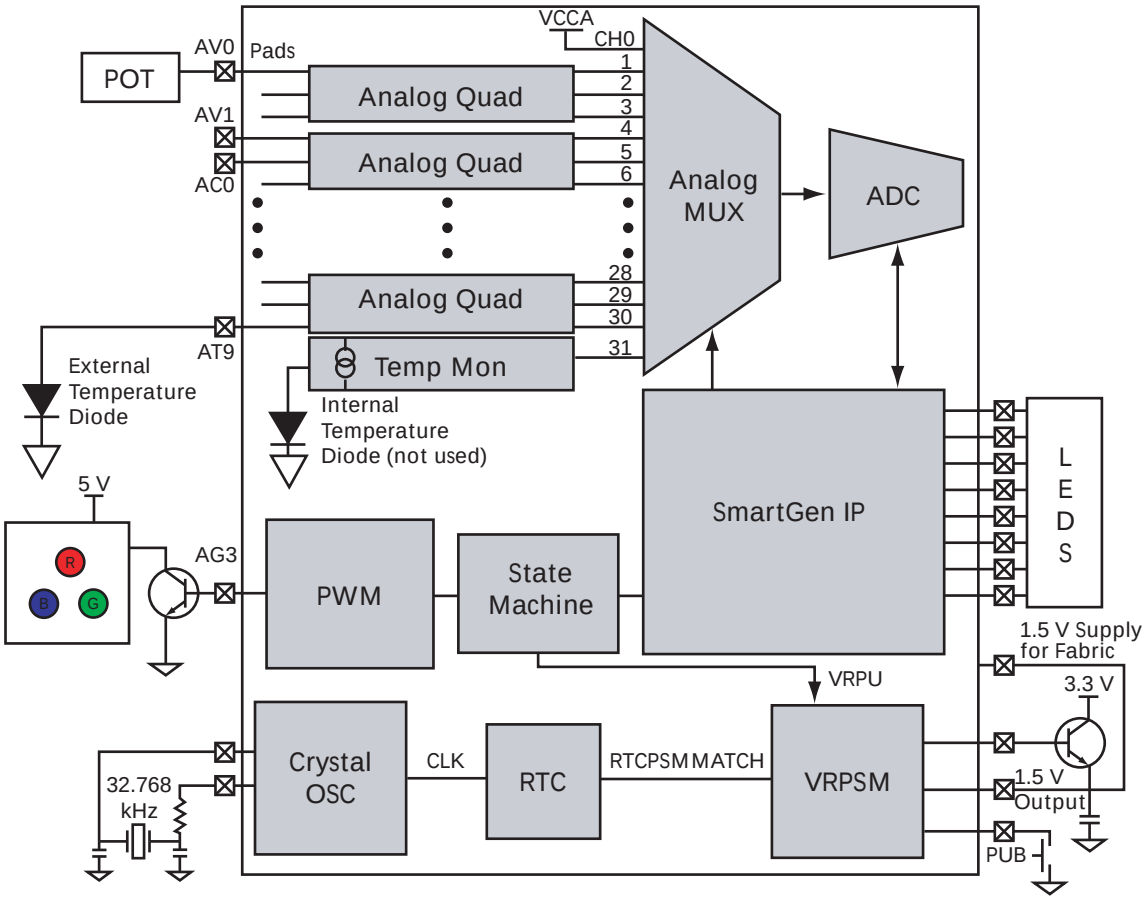
Once programming has completed, all demo design functionality on the board can be tested.

6.2 SmartDesign Demonstration

This demonstration design is created for the Microsemi Fusion Starter Kit. The 5 V, 3.3 V, and 1.5 V on-board power supplies are used in this design. Multiple analog input channels are utilized to sample the voltage and current provided to different loads. The design also samples the temperature through an on-board temperature sensor. Single-color LEDs are used to demonstrate the voltage threshold flags, and the tricolor LED is used to indicate different temperature levels with different colors.

The following figure shows the block diagram of functionality description.

Figure 26 • **Block Diagram Functionality Description**



The following peripherals and functionality are exercised in the demo design.

6.2.0.1 Voltage Monitor

The demo design uses analog channel AV0 (pin M6) to monitor the voltage output from potentiometer R50. By adjusting the potentiometer, one can see LEDs D5–D8 turning on or off as the voltage output from the potentiometer changes. For more information, see Table 9, page 40.

When the potentiometer is set to a different voltage level, the tricolor LED (U1) flashes at a different speed. The speed range varies from slowest (AV0 < 1.5 V [~1 Hz]) to fastest (AV0 > 4.5 V [always on]).

6.2.0.2 Current Monitor

Channels AV3 (pin R7) and AC3 (pin N7) are used to monitor the current flowing from the 5 V power supply to the tricolor LED (U1). The following AV and AC pairs are also used to monitor the voltage and current of other power supplies. For more information, see Implementation, page 41.

- AV1 and AC1 – AFS600 3.3 V power supply
- AV2 and AC2 – AFS600 1.5 V power supply
- AV4 and AC4 – 1.5 V power supply for extra load on board
- AV5 and AC5 – 3.3 V power supply for extra load on board

6.2.0.3 Temperature Monitor

Channel AT9 is used together with the external temperature sensor to monitor the temperature of the Starter Kit environment. The tricolor LED (U1) will light up with different colors based on the temperature level detected.

- When temperature AT > 20°C, the LED lights up blue.

- When temperature AT > 30°C, the LED lights up green.
- When temperature AT > 40°C, the LED lights up red.

6.2.0.4 Sleep Mode Demonstration

The real-time counter (RTC) is used in this demo to generate a power-on instruction (RTCPSMMATCH) to the Fusion internal voltage regulator. A 2-bit counter (CNT2) built into the logic design generates a power-off instruction (VRPU) so that the voltage regulator can be turned off from the Fusion fabric. With the RTC and CNT2, the user can test out the Sleep Mode of the Fusion device.

6.2.0.5 LCD

The LCD shows “Actel Fusion Starter Kit” after power-up. The following table lists the different functionalities of the potentiometer, LEDs, and switches on the Fusion Evaluation Board for the demo design.

Table 9 • **Functionality of the Potentiometer, LEDs, and Switches**

On-Board Device	Jumper #	Pin #	Channel Name	Functionality
LED D5	JP5	B13	AV0	When AV0 > 1.5 V, D5 lights up.
LED D6	JP6	A13	AV0	When AV0 > 2.5 V, D6 lights up.
LED D7	JP7	B14	AV0	When AV0 > 3.3 V, D7 lights up.
LED D8	JP8	A14	AV0	When AV0 > 4.5 V, D8 lights up.
Potentiometer R50	JP53	M6	AV0	Turning the potentiometer drives AV0 with analog voltage 0–5 V.
Switch SW7	N/A	R15	N/A	Connects to the PUB pad directly. When depressed, the PUB pad is grounded to power up the voltage regulator.
Switch SW6	JP16	L15	N/A	Connects to Aclr (active high) on the CNT2 (2-bit counter). When depressed, generates a '1' to reset the CNT.
Switch SW5	JP15	K11	N/A	Connects to CLK on the CNT2 (2-bit counter). When depressed, generates a clock pulse.
Switch SW4	JP11	B11	N/A	When depressed, shows the AFS600 core current on the LCD.
Switch SW3	JP11	B11	N/A	When depressed, shows the AFS600 core voltage on the LCD.
Switch SW2	JP11	B11	N/A	When depressed, shows the temperature sensed by the temperature sensor on the LCD.
Switch SW1	JP11	B11	N/A	When depressed, shows the potentiometer output voltage on the LCD.
Tricolor LED U1	JP69	AG6	AT	When temperature AT > 20°C, the LED lights up blue.
Tricolor LED U1	JP70	AG7	AT	When temperature AT > 30°C, the LED lights up green.
Tricolor LED U1	JP71	AG8	AT	When temperature AT > 40°C, the LED lights up red.

6.2.1 Demonstration Instructions

There are several special jumpers and pins on the Starter Kit that need to be paid attention. Select the appropriate jumper settings for your design. The following table lists the basic functions of these jumpers.

Table 10 • **Special Jumper/Pin Settings and Their Functionality**

JP / Pin #	Function	JP Setting	Value
JP25	VMV1	12	1.5 V
		23[1]	3.3 V[1]
JP26	VMV0	12	1.5 V
		23[1]	3.3 V[1]
JP27	VJTAG	12	1.5 V
		23[1]	3.3 V[1]
JP28	PTEM	12[1]	1.5V_INT[1]
		23	1.5V_EXT
Pin M15	TRSTB	Floating	JTAG Operations
		Grounded	Allows Power Down VR

1. Required for the demo design.

To exercise the demo design:

1. Power on using the Starter Kit power switch.
2. Turn the fabric on by pushing SW7.
3. Test the voltage monitor by turning the potentiometer to observe whether D5–D8 turn on and off and whether the tricolor LED blink speed changes.
4. If the ambient temperature is less than 20°C, the tricolor LED may not come on at all.
5. Turn on Sleep Mode by turning off the fabric with CNT2: Press SW6 once to reset, then press SW5 four times (clocking).
   - Generates 0–1–0 VRPU pulse
   - LEDs D1–D8 and the tricolor LED will be off

Note: The TRSTB pin (M15) needs to be grounded to demo Sleep mode.

6. Wake up the system via the RTC (at a preset time), or by pushing SW7 (hardwired power-up).
7. Test the temperature indicator by warming the temperature diode (Q8) with your fingers and checking that the tricolor LED goes from blue to green to red (depending on the room temperature, it may already be blue).
8. Press SW1 to show the potentiometer output voltage on the LCD.
9. Press SW2 to show the temperature sensed by Q8 on the LCD.
10. Press SW3 to show the AFS600 core voltage on the LCD.
11. Press SW4 to show the AFS600 core current on the LCD.

6.2.2 Implementation

To implement the above functionalities, create a Libero IDE project with the configuration described in the rest of this chapter. For information on how to create a Fusion Libero IDE project, see the *Fusion Design Flow Tutorial*.

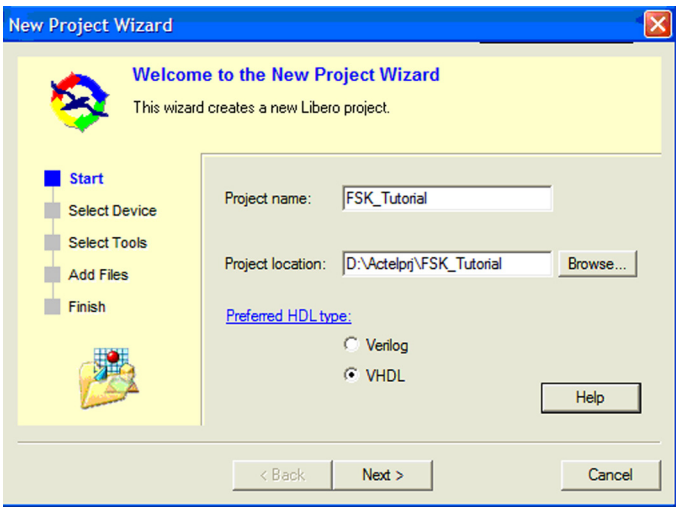
Before you can start the project you must download some design files from the Microsemi website.

1. Go to *http://www.Actel.com/documents/Fusion_StarterKit_DF.zip*. Download the zip file to your desktop.
2. Unzip and extract the files into the *Actelprj/sample/FSK_Tutorial* directory at the top-level.

6.2.2.1 Step 1 – Create Libero IDE Project

To create a new Libero IDE project (FSK_Tutorial), select **AFS600-FG256** and use the Libero IDE cores from the Catalog window to generate the different functional macros. Use SmartDesign to instantiate them in the top-level design.

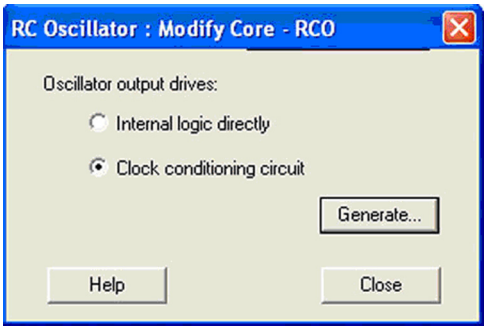
Figure 27 • **Create Libero IDE Project**



6.2.2.2 Step 2 – Generate RC Oscillator (RCO) from Libero IDE

From the Libero IDE cores folder, select **RC Oscillator** from the Fusion Peripherals category. The RC Oscillator (RCO) generates a fixed 100 MHz output clock. Configure the dialog box, as shown in the following figure. Click **Generate**, name your core *RCO,* and click **OK**.

Figure 28 • **RC Oscillator from Libero IDE**

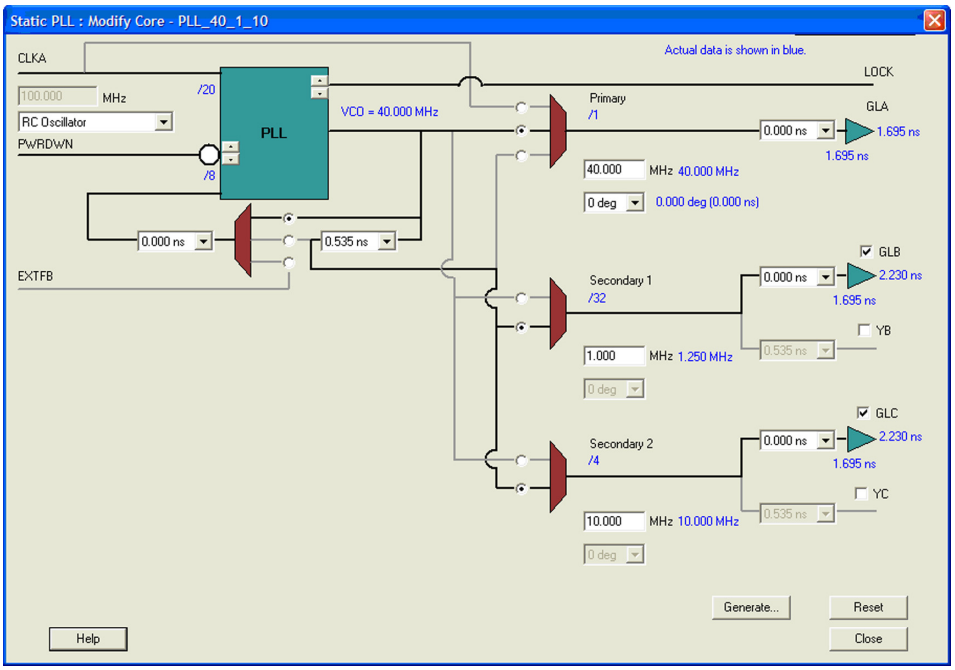


6.2.2.3 Step 3 – Generate PLL Macro (PLL_40_1_10) from Libero IDE

From the Libero IDE cores folder, select **Static PLL** from the Clock & Management category, as shown in the following figure.

Select **RC Oscillator** as the input clock source. The PLL (PLL_40_1_10) input clock is from RCO, and the output clocks are 40 MHz, 1 MHz, and 10 MHz. Click **Generate**, name your core *PLL_40_1_10,* and click **OK**.

Figure 29 • **Generate PLL Macro from Libero IDE**



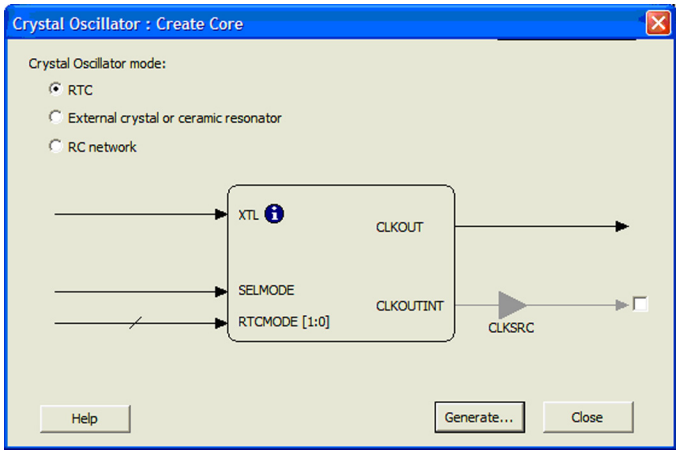
6.2.2.4 Step 4 – Generate No-Glitch Multiplexer (NGMUX) from Libero IDE

From the Libero IDE cores folder, select **MUX No-Glitch** from the Clock Management category. Accept the defaults. Click **Generate**, name your core *NG_MUX,* and click **OK**.

6.2.2.5 Step 5 – Generate Crystal Oscillator from Libero IDE

From the Libero IDE cores folder, select **Crystal Oscillator** from the Fusion Peripherals category. The crystal oscillator (XTALOSC) generates an output clock for the RTC. The on-board crystal oscillates at 32.768 kHz. The XTALOSC output clock is divided by 128 prior to driving the RTC, which makes the seventh bit of the 40-bit RTC register toggle at 1 Hz. Click **Generate**, name your core *XTALOSC,* and click **OK**.

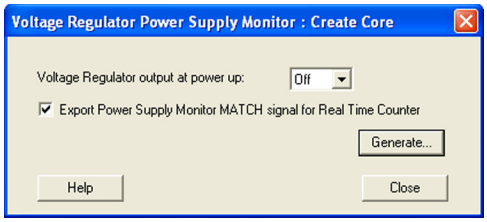
Figure 30 • **Generate Crystal Oscillator from Libero IDE**



6.2.2.6 Step 6 – Generate Voltage Regulator Power Supply Monitor from Libero IDE

From the Libero IDE cores folder, select **Voltage Regulator Power Supply Monitor** from the Fusion Peripherals category. Click **Generate**, name your core *VR_PSM,* and click **OK**.

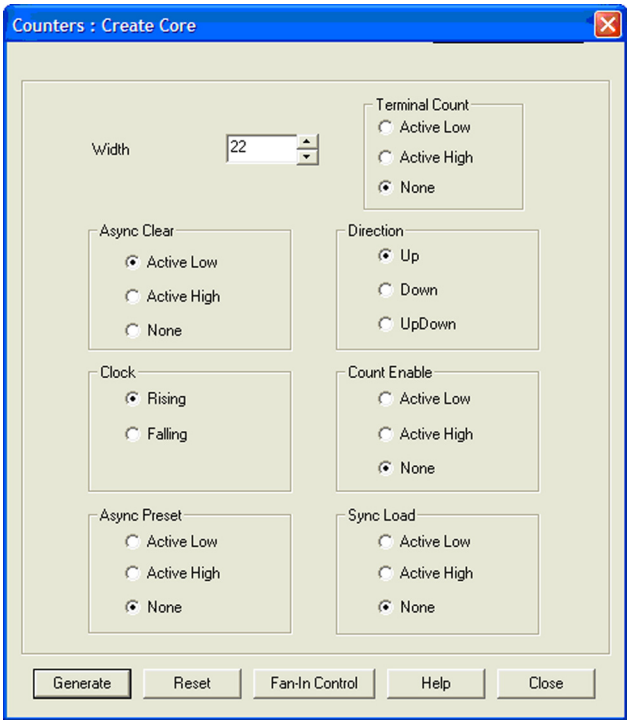
Figure 31 • **Generate Voltage Regulator Power Supply Monitor from Libero IDE**



6.2.2.7 Step 7 – Generate 22-Bit Counter from Libero IDE

From the Libero IDE cores folder, select **Counter** from the Basic category. Generate a 22-bit counter, as shown in the following figure to control the flashing rate of the tricolor LED based on the voltage level set by the potentiometer. Name your core *CNT22* and click **OK**.

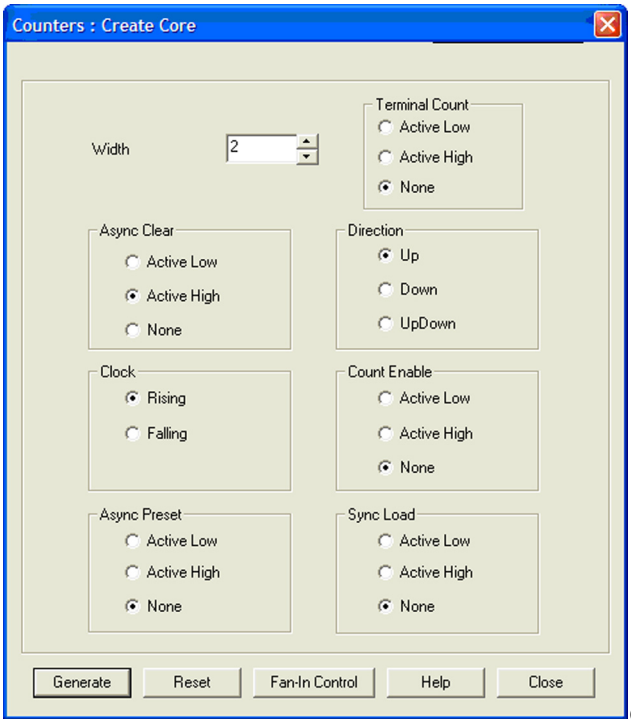
Figure 32 • **Generate 22-Bit Counter from Libero IDE**



6.2.2.8 Step 8 – Generate 2-Bit Counter from Libero IDE

From the Libero IDE cores folder, select **Counter** from the Basic category**.** Generate a 2-bit counter, as shown in the following figure, to control the internal voltage regulator. Name your core *CNT2* and click **OK**.

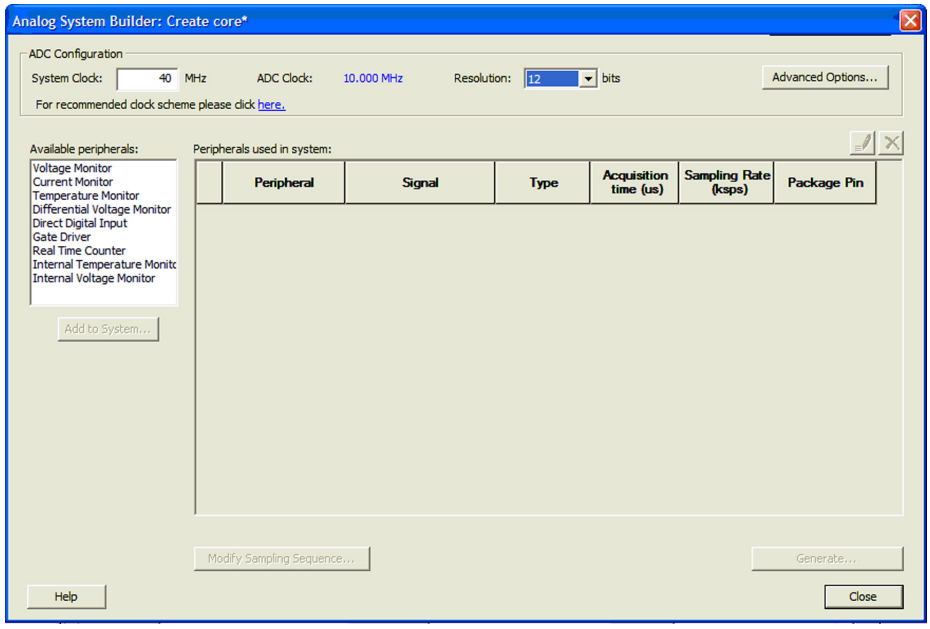
Figure 33 • **Generate 2-Bit Counter from Libero IDE**



6.2.2.9 Step 9 – Generate Analog System from Libero IDE

From the Libero IDE cores folder, select **Analog System Builder** from the Fusion Peripherals category.

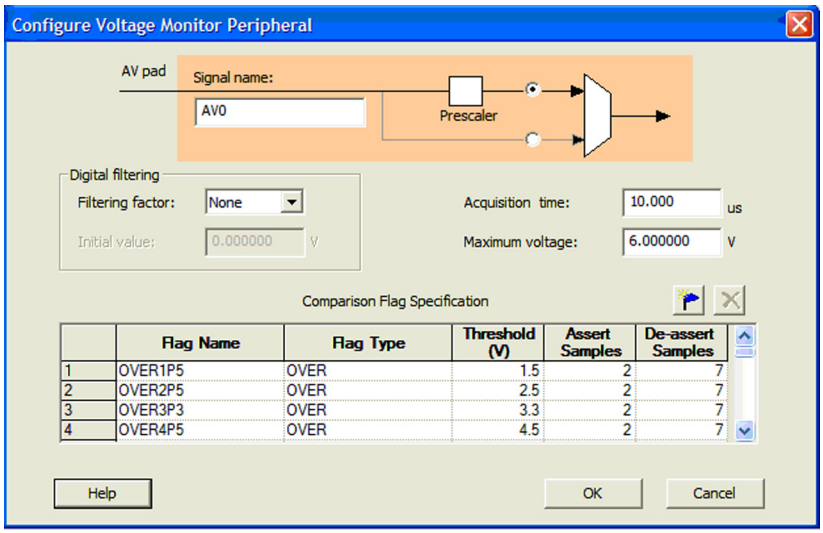
Figure 34 • **Generate Analog System from Libero IDE**



Set the **System Clock** to 40 MHz and the **Resolution** to 12 bits.

Follow the sequence shown in Figure 35, page 46 through Figure 41, page 51 to create the RTC and the voltage, current, and temperature monitors.

Figure 35 • **Voltage Monitor AV0**



The following table lists the LEDs connected to the AV0 flags.

Table 11 • **On-Board LED Setup for Voltage Monitor AV0**

LED	Flag
D8	OVER4P5
D7	OVER3P3
D6	OVER2P5
D5	OVER1P5

AV0 connects to a potentiometer with a maximum output of 5 V. The user can turn the potentiometer either way and see LEDs D5–D8 turn on and off to indicate the voltage range. Set AV0 to pin M6.

Figure 36 • **Current Monitor AC1 and Voltage Monitor AV1**

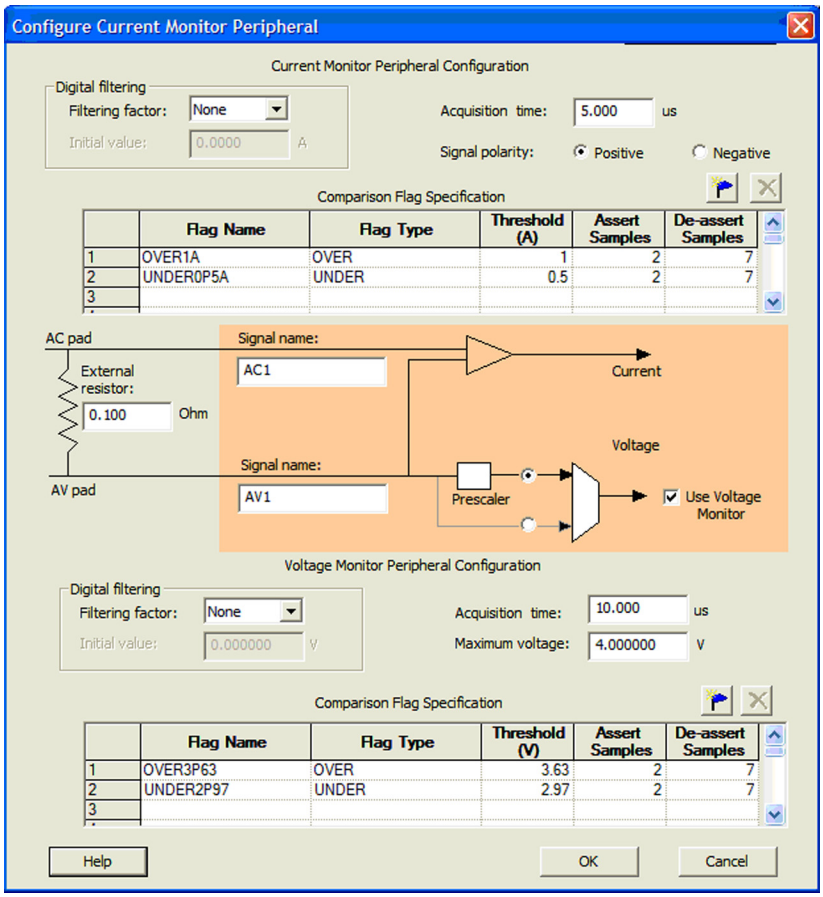


Figure 37 • **Current Monitor AC2 and Voltage Monitor AV2**

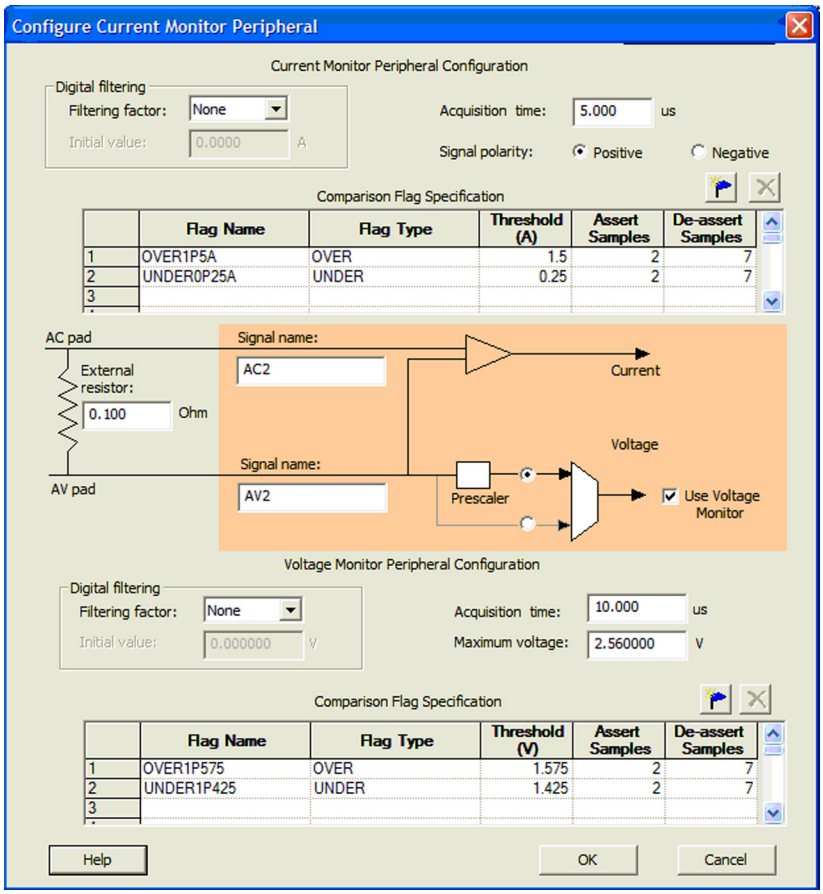
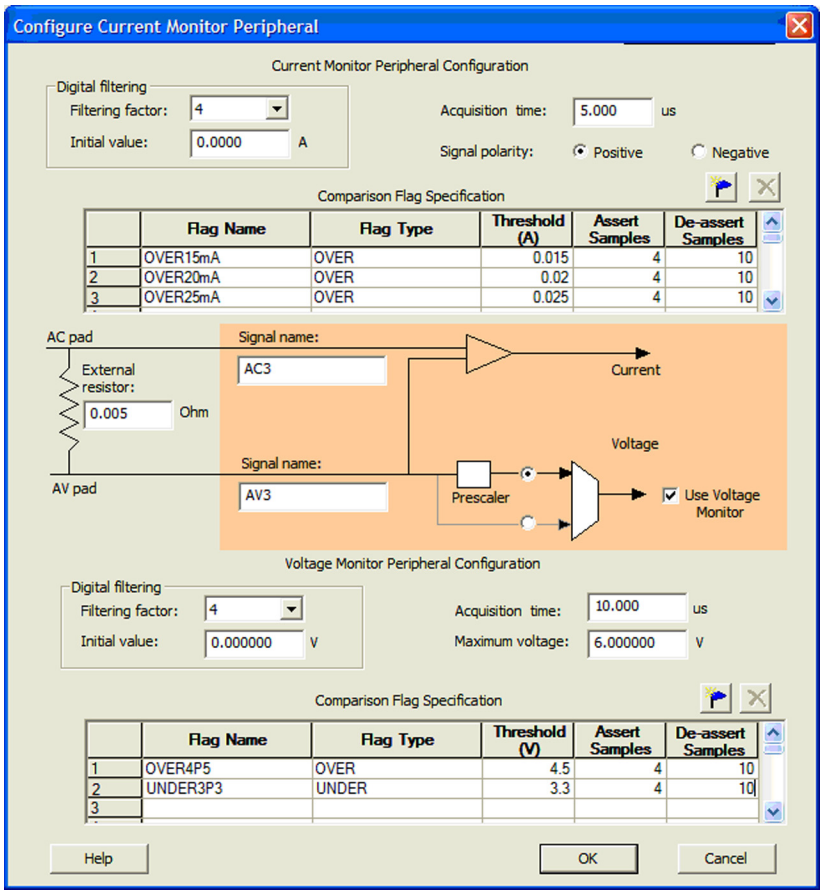


Figure 38 • **Current Monitor AC3 and Voltage Monitor AV3**



Follow the example shown in the preceding figure to set the following current monitor flags:

- OVER15mA
- OVER20mA
- OVER25mA

Figure 39 • **Current Monitor AC4 and Voltage Monitor AV4**

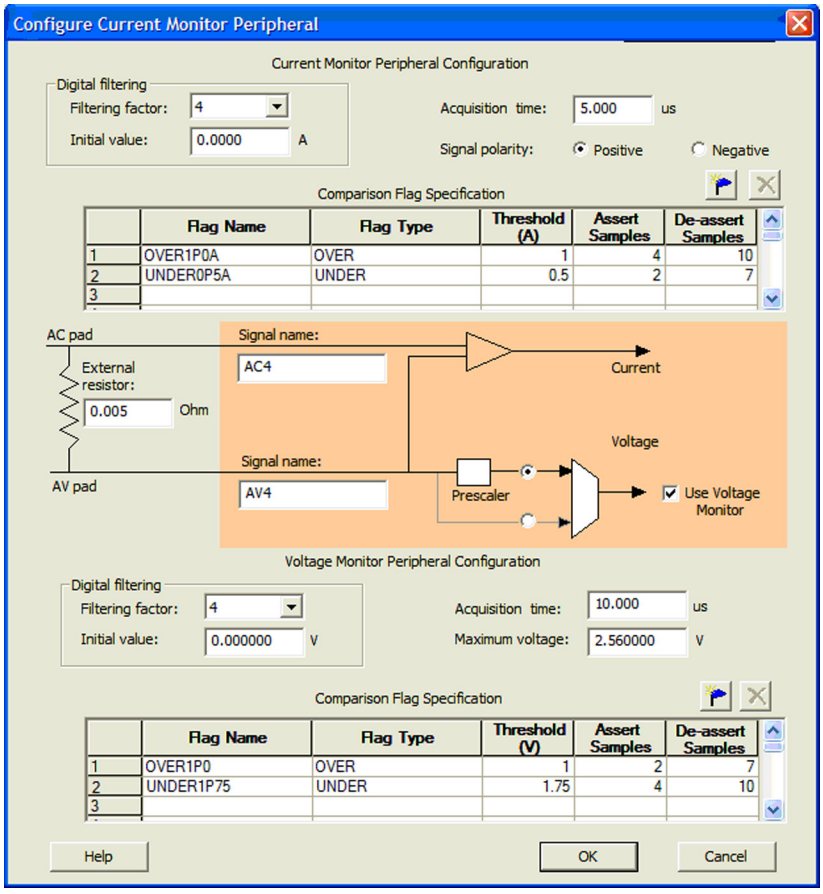


Figure 40 • **Current Monitor AC5 and Voltage Monitor AV5**

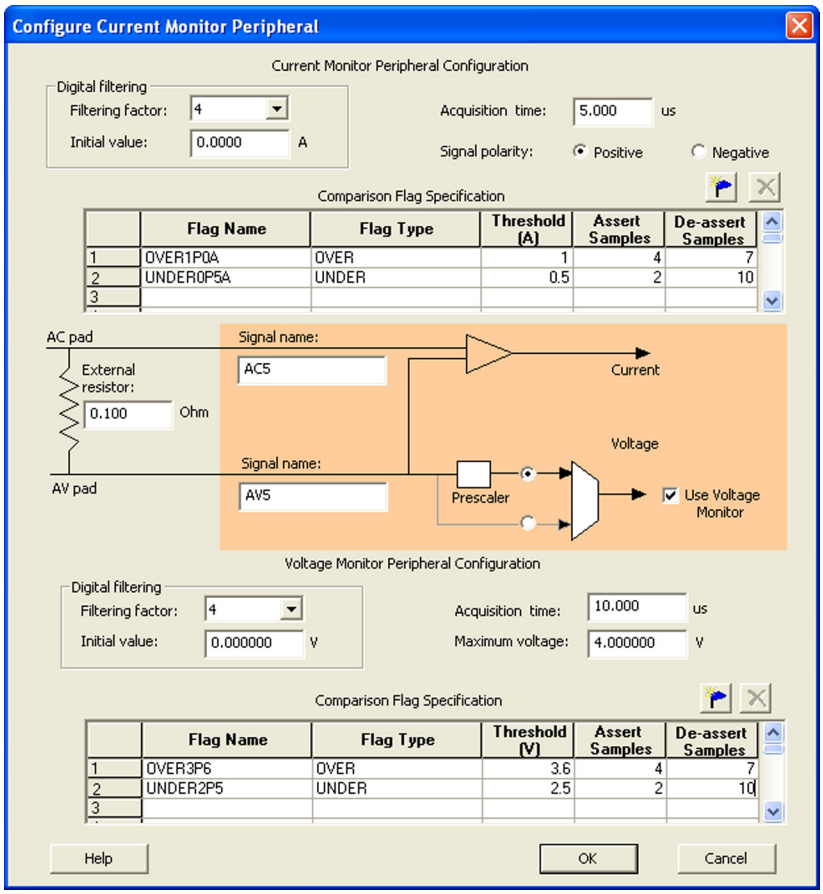
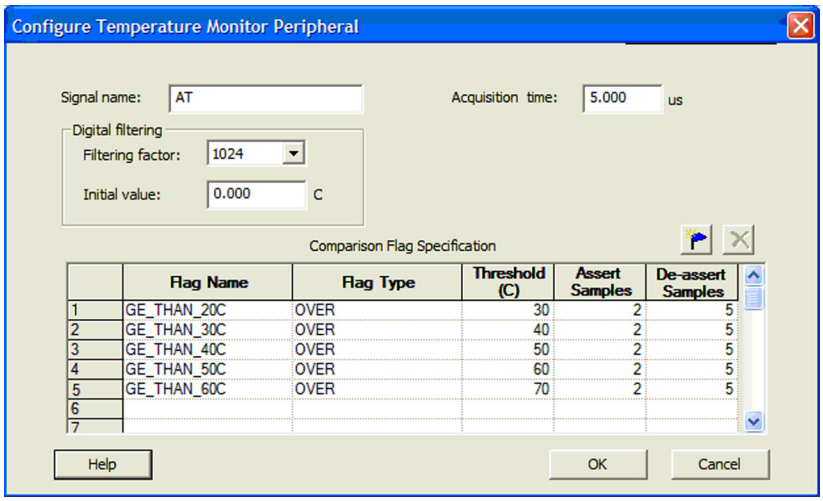


Figure 41 • **Temperature Monitor AT**



For the temperature monitor, calibration is required. In this demo design, a 10°C offset is added into the threshold value for calibration. Follow the example shown in the preceding figure to set the following temperature monitor flags:

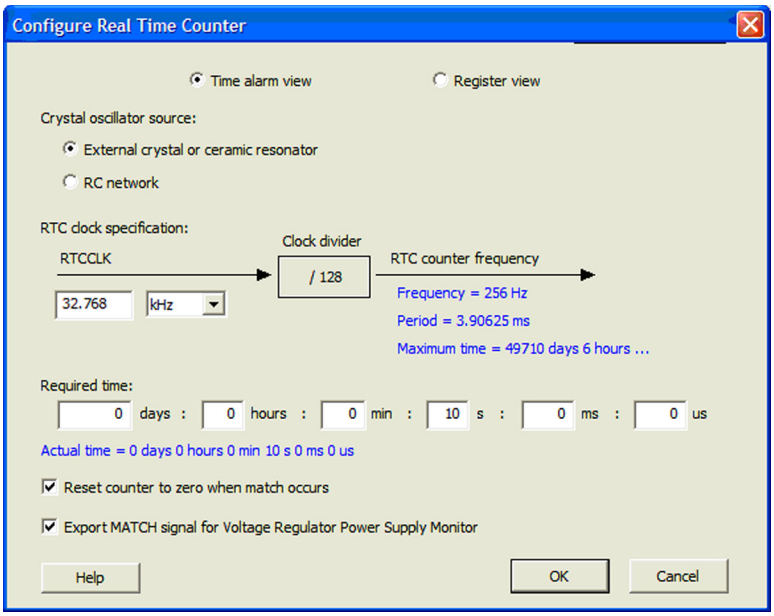
- GE_THAN_20C
- GE_THAN_30C
- GE_THAN_40C
- GE_THAN_50C
- GE_THAN_60C

The following table lists the colors emitted by the tricolor LED for each temperature range.

Table 12 • **On-Board Tricolor LED Setup for Temperature Monitor AT**

Temperature	LED Color
>20°C	Blue
>30°C	Green
>40°C	Red

Figure 42 • **Real-Time Counter**



With a 32.768 kHz crystal oscillator input clock, set the RTC match value to 10 seconds. In the demo design, the RTC starts counting as soon as the 3.3 V power supply is available and resets itself back to 0 when the match value is hit. Therefore, if the Fusion device is put into Sleep Mode while the RTC count is at 3 seconds, the device will wake itself up after another 8 seconds unless it is woken up by grounding the PUB pad, or pressing SW7.

6.2.2.9.1 Gate Drivers

Follow the sequence shown in Figure 43, page 53 through Figure 48, page 55 to create the gate drivers for the voltage, current, and temperature monitors.

Figure 43 • **Gate Driver – Step 1**

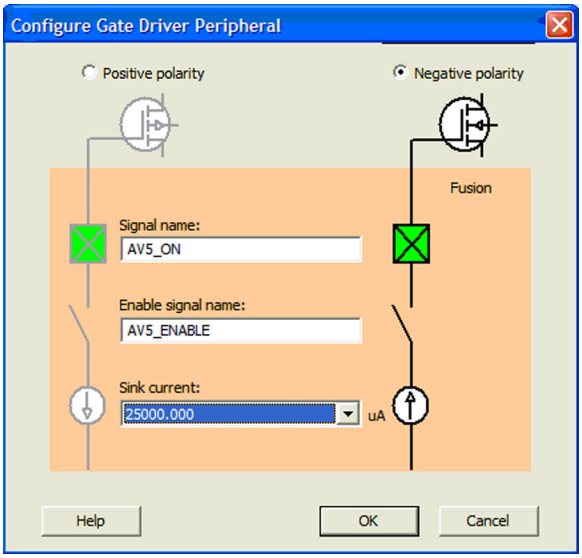


Figure 44 • **Gate Driver – Step 2**

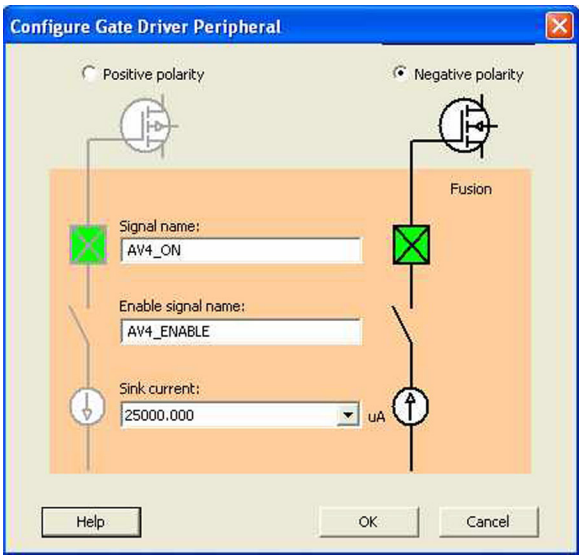


Figure 45 • **Gate Driver – Step 3**

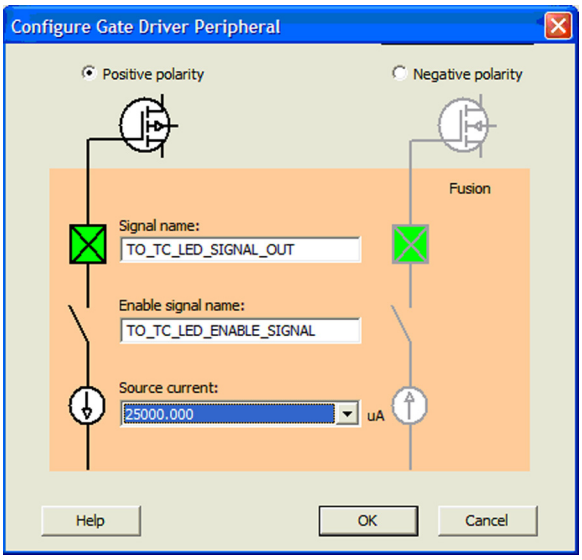


Figure 46 • **Gate Driver – Step 4**

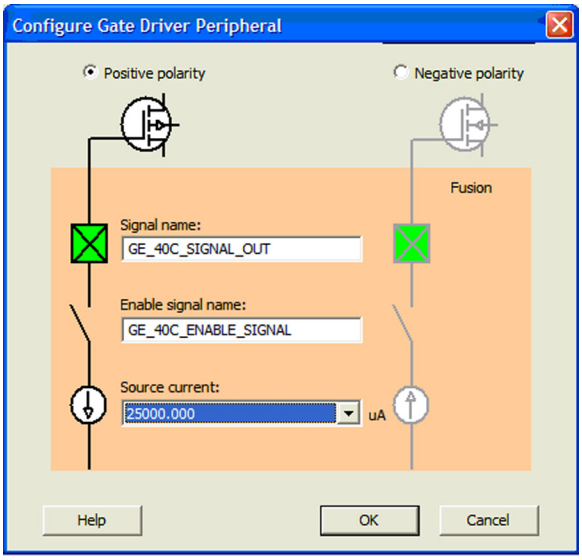


Figure 47 • **Gate Driver – Step 5**

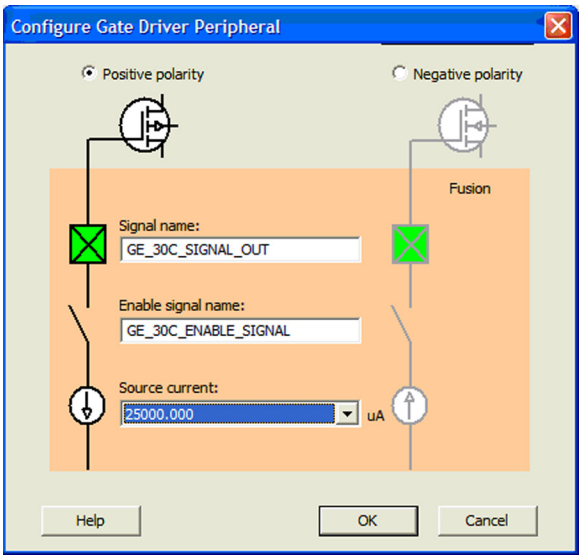
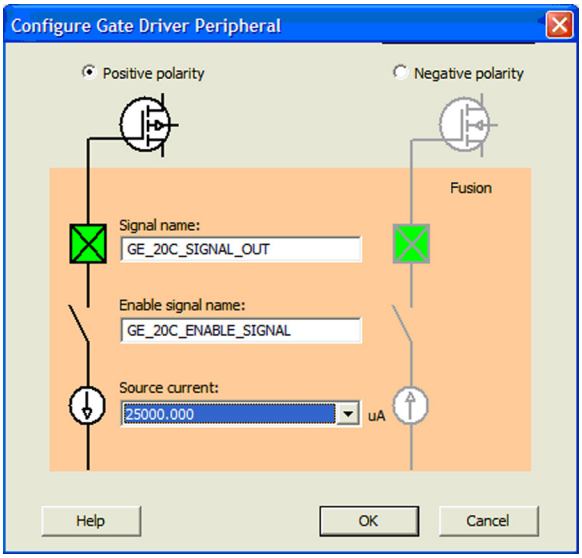
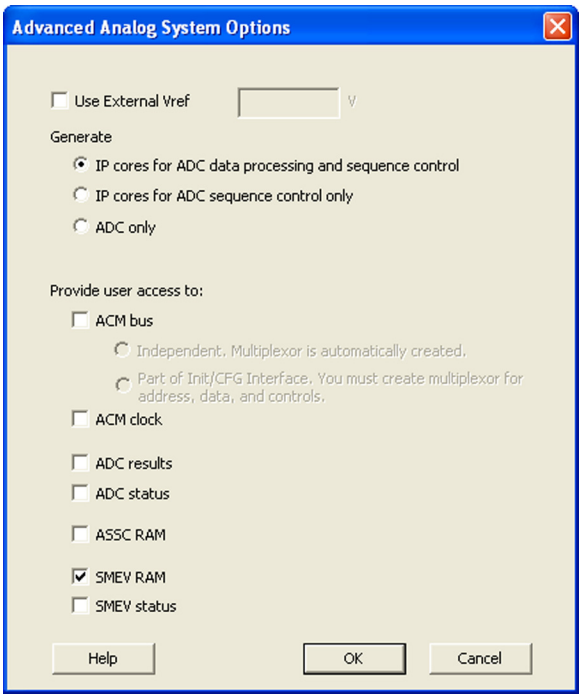


Figure 48 • **Gate Driver – Step 6**



Click the **Advanced Options** button. This opens the Advanced Analog System Options dialog box.

Figure 49 • **Advanced Analog System Options Dialog Box**



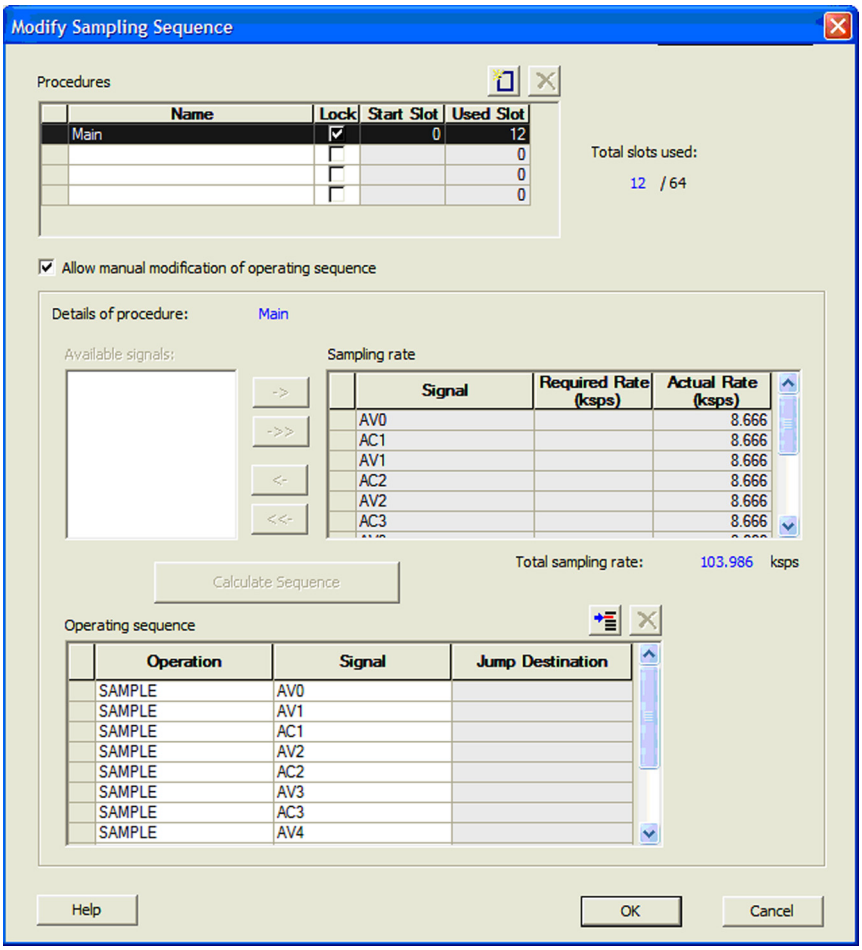
In the **Provide users access to** section, select **SMEV RAM** and clear all other options.

6.2.2.9.2 ADC Sample Sequence

Click the **Modify Sampling Sequence** button in the ASB to invoke the ADC Sampling Sequence window. Set up the ADC sample sequence, as shown in the following figure.

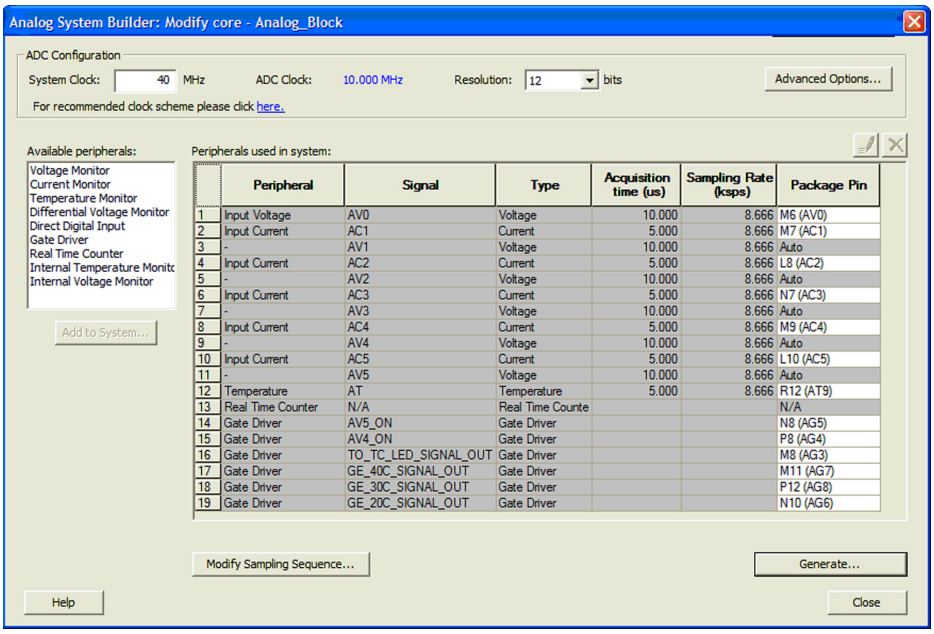
Click the **->>** button to select all available signals, and then click **Calculate Sequence**. Select the **Allow manual modification of operating sequence** option. Adjust the sample sequence manually from the **Operating sequence** section. Make sure the last operation is **SAMPLE_JUMP** back to the **Main** procedure.

Figure 50 • **ADC Sample Sequence**



Select the package pin number for each peripheral under the Package Pin column to match the following figure. Generate the analog system by clicking the **Generate** button. Set the macro to **Analog_Block**.

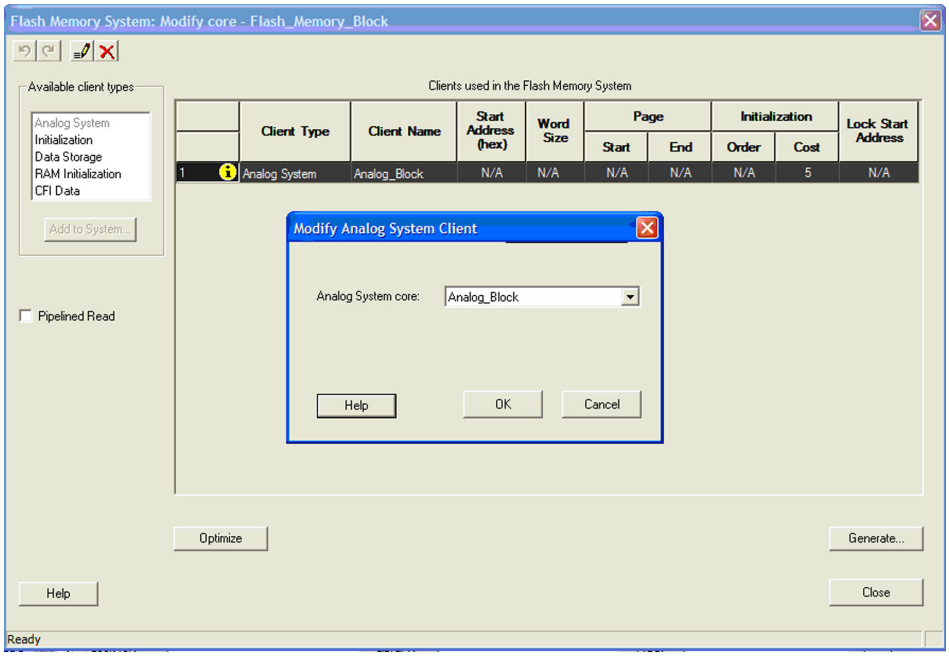
Figure 51 • **Package Pin Number and Peripheral**



6.2.2.10 Step 10 – Generate Flash Memory Block from Libero IDE

From the Libero IDE cores folder, select **Flash Memory System Builder** from the Fusion Peripherals category. Double-click **Analog System** and select **Analog_Block** from the Analog System core, then click **OK**. Click the **Generate** button to generate the Flash Memory Block, and set the core name to **Flash_Memory_Block**.

Figure 52 • **Generate Flash Memory Block from Libero IDE**



6.2.2.11 Step 11 – Create Other HDL Macros

This tutorial also utilizes the on-board LCD and DIP switches; thus corresponding LCD controller and switch debounce HDL macros are created. From the **File** menu, choose **Import files**, set the file type to **HDL Source Files**, and import the following HDL files from the sample project:

- LCD_controller.vhd
- LCD_interface.vhd
- formatter.vhd
- BCD_digit.vhd
- debounce.vhd

6.2.2.12 Step 12 – Create Top Level

After generating the major functional blocks, create the top level for the demo design.

Users can manually code the HDL top level for Fusion designs to instantiate and connect multiple macros together. Or, since Libero IDE v8.0, users can use SmartDesign to easily instantiate and connect different macros in a user-friendly GUI. This will be the base of the top level for Fusion designs.

In this tutorial, SmartDesign is used for top-level creation. For more details on how to use SmartDesign, see the *Libero IDE User Guide*.

1. Invoke SmartDesign from the Project Flow window, and name the SmartDesign Component **SUB1**.
2. Drag and drop all the cores you've just created into the SmartDesign Canvas window.
   Analog_Block
   Flash_Memory_Block
   NG_MUX
   PLL_40_1_10
   RCO
   VR_PSM
   XTALOSC
3. Click the **Save** button under the menu. The hierarchy will be refreshed.
4. Right-click the **canvas window** and choose **Auto Connect**. Some dedicated connections are done for users automatically.
5. Select the **Connectivity Grid** and finish all the rest of connections as specified in SUB1 Connections, page 98.
6. There are multiple threshold flags coming out of the Analog Block. Users can select and promote different flags to the top level. To simplify the connection and leave more flexibility to users, this tutorial only promotes some of the flags.
7. Click the **Save** button to capture all the connectivity.
8. From the **File** menu, select **Import files**, and import *SUB2.vhd* from the sample project.
9. The SUB2 entity also includes logic to read the ADC result from the SMEV RAM.
10. Create a SmartDesign component, **FSK_tutorial**.
11. Drag and drop the **SUB1** and **SUB2** components onto the canvas.
12. Make all the connections in the Connectivity Grid, as specified in FSK_Tutorial Connections, page 100.
13. Click the **Save** button to capture the connectivity.
14. Right-click the **canvas window** and select **Generate**. `FSK_tutorial.vhd` is generated.

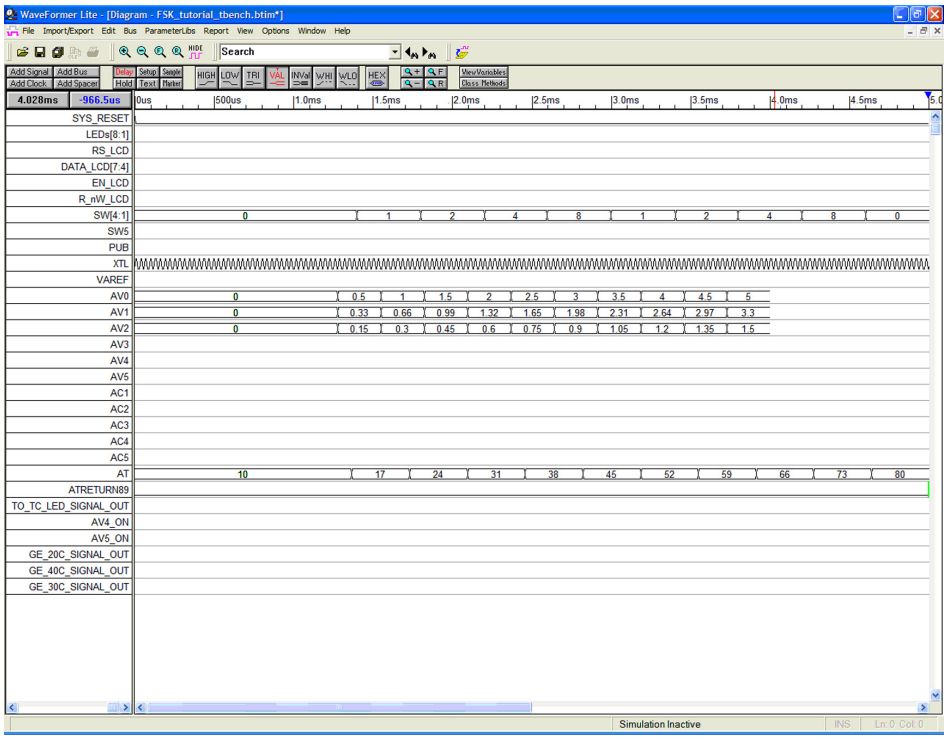
6.2.2.13 Step 13 – Create Testbench

After creating the top level, generate a testbench to simulate and verify the functionality of the design. In the Hierarchy window, select **FSK_tutorial** as the root.

Copy *<sample_project>/FSK_Tutorial/Stimulus/FSK_tutorial_tbench.btim* to *<Your_projects_folder>/FSK_Tutorial/Stimulus/.*

Double-click the *FSK_tutorial_tbench.btim* file in the File window to open the stimulus file in WaveFormer Lite.

Figure 53 • **Create Testbench**



Export the timing diagram by selecting **Import/Export > Export Timing Diagram**, select the file type as **V**HDL w/ Top Level Test Bench and save the file as *FSK_tutorial_tbench.vhd*.

For more information, see *Creating Analog Test Benches for Fusion Designs*.

6.2.2.14 Step 14 – Run Pre-Synthesis Simulation

From the **File** menu, choose **Import Files**, set the file type to **Simulation Files** and import the *wave.do* file from the sample project files.

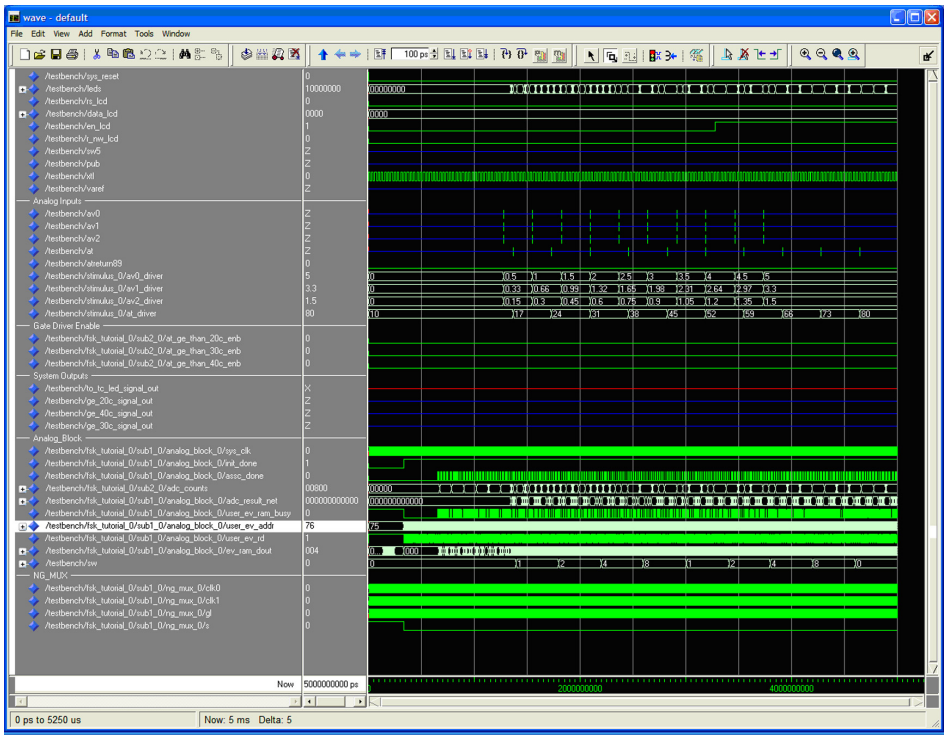
From the **Project** menu, choose **Settings**, click the **Simulation** tab, and select **Include Do file**.

In the Hierarchy window, right-click the top-level **FSK_tutorial** and choose **Organize Stimulus**. Add *FSK_tutorial_tbench.vhd*.

From the **Project** folder, choose **Settings**. Click the **Simulation** tab and enter **4ms** as the simulation run time.

In the Hierarchy window, right-click the top-level **FSK_tutorial** and choose **Run Pre-Synthesis Simulation**.

Figure 54 • **Run Pre-Synthesis Simulation**



6.2.2.15 Step 15 – Run Synthesis and Place-and-Route

After the functional simulation is done, you can proceed to synthesize and place-and-route the design. After Synthesis is done, run post-synthesis simulation. Include the *post-syn-wave.do* file in the simulation options to view appropriate waveforms for the post-synthesis results.

From the Libero IDE **File** menu, choose **Import Files**, set the file type to **Physical Design Constraint File**, and import the *FSK_tutorial.pdc* file from the sample project files.

In the Hierarchy window, right-click the top-level **FSK_tutorial** and select **Organize Designer Constraint Files**. Remove *FSK_tutorial_sdc.sdc* and add *FSK_tutorial.pdc*.

Click the **Place & Route** button from the Project Flow window. This will open Designer. If the Device Selection Wizard opens, accept all defaults and click **Finish**.

Click **Compile**, accept all defaults, and click **OK**. When the compile button turns green, compilation has been completed.

Click **Layout**, accept all defaults, and click **OK**. When the layout button turns green, layout has been completed.

Click **Back-Annotate** to generate back-annotation files. Once back-annotation is done, perform back-annotation simulation. Include the *post-layout-wave.do* file in the simulation options to view appropriate waveforms for the back-annotation results.

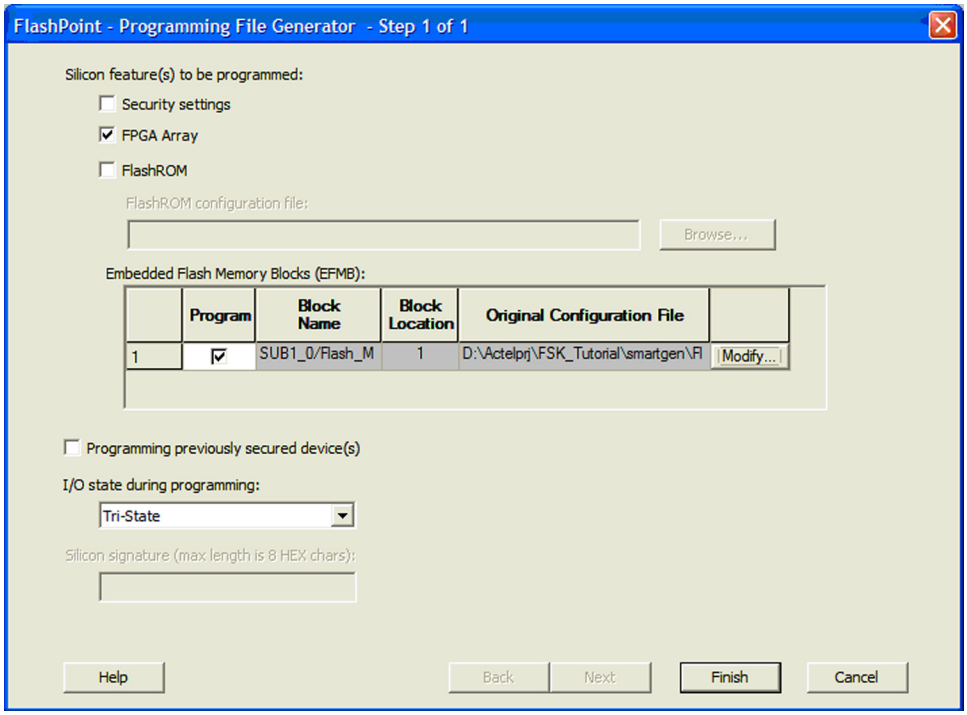
6.2.2.16 Step 16 – Generate Programming File

Once the back-annotation simulation is done, generate the STAPL programming file.

To generate the STAPL programming file:

1. Click the **Programming File** icon in Designer. The dialog shown in the following figure will appear.

Figure 55 • **Generating Fusion Programming File**

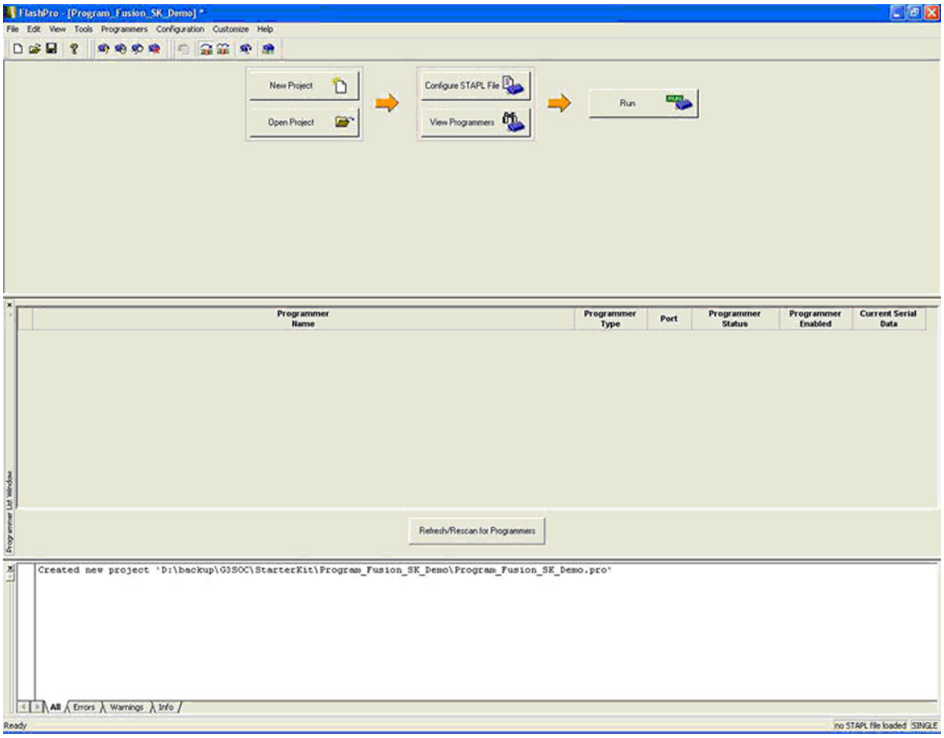


2. Select the **Program** check box.
3. Click **Modify** to open the Modify Embedded Flash Memory Block dialog box.
4. Click **Import Configuration File**, select the EFC file from *<project folder>\smartgen\Flash_Memory_Block*, and click **OK**.
5. Click **Finish** to generate a programming file with which to program the Flash Memory Block and the FPGA array.
6. Select both **Programming Data (**.pdb**)** and **STAPL (**.stapl**)** when generating the programming file.

6.2.2.17 Step 17 – Program the AFS600 on the Fusion Evaluation Board

Connect the FlashPro3 programmer to the Fusion Evaluation Board programming header. Power-up the board and follow the *FlashPro for Software User Guide* to program the AFS600.

Figure 56 • **Program the AFS600 on the Fusion Evaluation Board**



Up to this point, you have created the Fusion starter kit demo design to demonstrate the following peripherals and functionality:

1. Analog System Block: Voltage Monitor Current Monitor Temperature Monitor Gate Driver RTC
2. Embedded Flash Memory Block
3. RC Oscillator
4. Crystal Oscillator
5. PLL
6. Fusion FPGA Fabric
7. GPIO
8. LCD

Once programming is complete, you can test all demo design functionality on the board.

7 Test Procedures for Board Testing

This chapter defines the test procedure required to be carried out by the Microsemi-designated manufacturer's testing facility on the Fusion Evaluation Board with silkscreen labeling AFS-EVAL-BRD1. This testing is specific to the socketed version of the board. All steps in the following enumerated test procedure should be followed in sequence for testing the board. Deviations in the sequence are explained in the text.

7.1 Equipment Required

7.1.1 Microsemi Equipment Provided by Microsemi to Testing Facility

Microsemi will provide the following:

- This test procedure document
- FlashPro v4.1 software on a CD-ROM
- FlashPro3 programmer and programming cable for connecting to the AFS-EVAL-BRD1
- Pre-programmed AFS600-FG256 silicon. Ten devices will be provided for ten boards. The initial silicon will not be labeled as having been programmed. (This is just for the testing associated with the first manufacturing build.) Additional devices will be provided for testing further boards, and this change will be detailed in an update to the procedure.
- Power supply (+9 V, 2 A CUI) for the Fusion Evaluation Board, plus a mains cable for the power supply

7.1.2 Testing Facility Equipment to Be Available for Testing

The manufacturer's testing facility will provide the following equipment for testing of the board: Digital multimeter to measure voltages on the circuit board at the known test points

7.2 Test Procedure for the AFS-EVAL-BRD1

In this section, full test procedure for the boards is outlined. This procedure applies to socketed boards. For boards fitted with directly soldered parts, the procedure is the same except for fitting of the FPGA. In such cases, the reader should adjust the procedure accordingly and ignore references to fitting parts to sockets.

7.2.1 Initial Power-Up Procedure

This part of the procedure may be carried out independently and ahead of the other parts of the test procedure. Boards passing this procedure may be transferred to a passing set of boards.

To perform the initial power-up procedure:

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) in a test log.
2. Plug the +9 V power supply into the wall.
3. Take an AFS-EVAL-BRD1 that has an empty socket. Make sure switch SW11 is in the OFF position, (the switch should be moved to the left). This corresponds with the labeling of the silkscreen on the board.
4. Connect +9 V DC output of the CUI power supply to the J18 connector on the board. You should observe the red LED at the top right of the board, i.e., LED D19 should light indicating +9 V DC has been applied to the board.
5. Move the SW11 switch to the ON position, i.e., move the switch to the right. Observe that LEDs D13, D9, D10, D11, and D17 light up green on the board. All LEDs are on the top edge of the board (same edge as the red D19 power connector LED, which should remain lit).
6. Using a DVM, measure DC voltages using TP11 as ground:
7. TP6 and TP7 – should be 3.3 V (values ±0.2 V are acceptable). Values outside this range are a failure.
8. TP15 – should be 1.5 V (values ±0.1 V are acceptable)

TP8 – should be 1.8 V (values ±0.1 V are acceptable)

TP10 – should be 2.5 V (values ±0.2 V are acceptable)

TP47 – should be 5.0 V (values ±0.2 V are acceptable)

J14C pin 106 – should be 3.3 V (values ±0.2 V are acceptable). Note that jumper JP48 must be in place for this measurement, otherwise zero will be recorded.

9. That completes the initial power-up check. The board should now be switched off by moving SW11 to the OFF position (to the left).

7.2.2 Testing Board Functionality with AFS600-FG256 Silicon

To test board functionality:

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) in a test log.
2. Make sure switch SW11 is in the OFF position (i.e., to the left).
3. Apply power to the board by attaching the +9 V DC supply to J18. Only the red LED should be illuminated.
4. Undo the four screws holding the socket of U8 in place. Remove the lid of the socket.
5. Place a pre-programmed AFS600-FG256 FPGA part into the socket using the appropriate vacuum pen while observing anti-static precautions. Make sure that pin 1 of the FPGA is oriented correctly. (The Microsemi logo on the part should match the orientation of the Actel logo on the board just above the AFS-EVAL-BRD1 part number.) Take great care to make sure all pins are in correct alignment so that the FPGA is on a level plane parallel to the board.
6. Carefully replace the socket cover and screw down all four corners to appropriate tightness. It is recommended that you tighten opposite corners first so as to lessen rotational torque on the part.
7. Switch SW11 to the ON position (slide it to the right).
8. Validate that all five LEDs at the top of the board, including the red one, turn on: D17, D11, D10, D9, D13, and D19.
9. Validate that LEDs D8 through D1 all pulsate in either a counting pattern or a “center to outside swinging” pattern.
10. If no LEDs are visible, stop and switch off SW11. Rotate SW8 and SW9 clockwise to the 3.3 V selection. This is best described with the thicker arrow bar pointing upward. Switch the board back on. The LEDs should be visible. If very dim, stop, switch off the board and rotate the switches one quarter turn clockwise before switching the board back on. Continue if the LEDs are glowing. If unable to get a display on the LEDs, the board must be tagged as bad.
11. If it is a bad board, carefully remove the AFS600-FG256 silicon from the socket and set it aside in an electrostatic-safe area. Using another piece of pre-programmed silicon, repeat steps 4 to 8 above.
12. If still no response, mark the board as defective and re-use the silicon for other testing.
13. If there is a good response, then place the previous silicon in a “bad” tray to prevent it from being retested.
14. Validate that the patterns can be switched by pressing SW6 (Global pulse) on the left side of board. When the switch is pressed, the LED D15 should momentarily light. The pattern on LEDs D8 through D1 will change.
15. Validate that the message “Microsemi Fusion Starter Kit” continually cycles on the LCD. You may need to turn R40 clockwise to adjust contrast on the display until the message is dark enough to see.
16. If no message is observed, press buttons SW4 and SW3 simultaneously. This will usually reset the system after a few cycles of the counter.
17. Connect a FlashPro3 programmer to a PC USB port and observe that the power light illuminates. Ensure that the FlashPro v4.1 software is installed on the PC being used.
18. Connect the programming cable of the FlashPro3 programmer to the J1 shrouded and keyed header labeled FP3. The red line labeling pin 1 should be close to pin 1 on the header – no other orientation is possible.
19. On the PC, run the FlashPro v4.1 software and connect to the programmer. Select **Fusion** as the device family. Once the software has shown a connection, select **Analyze Chain** from the **File** menu.
    If an error message of incorrect VJTAG is reported, remove the jumper placed at J5 and place it instead at J12 across pins 11 and 12. It may safely be left there. Repeat the **Analyze Chain** command.

If a message appears indicating that an AFS600 part (depending on the device fitted to the board) has been detected, then the board has passed this test. Leave the silicon in place in the socket and move to the next step.

If a message of **11** or some other numeric indication appears, record the message in a test log and fail the board. Remove the silicon from the socket and place it in the safe silicon holding area.

This concludes the testing of the board. Switch SW11 to the OFF position and remove the power connector from J18.

8 Appendix: FG256 Package Connections for AFS600 Devices

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O. The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

IO Nomenclature = Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access – i.e., global pins

Where,

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank in a clockwise direction

x = P (Positive) or N (Negative) for differential pairs, or R (Regular – single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as LVPECL pair.

w = D (Differential Pair) or P (Pair) or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

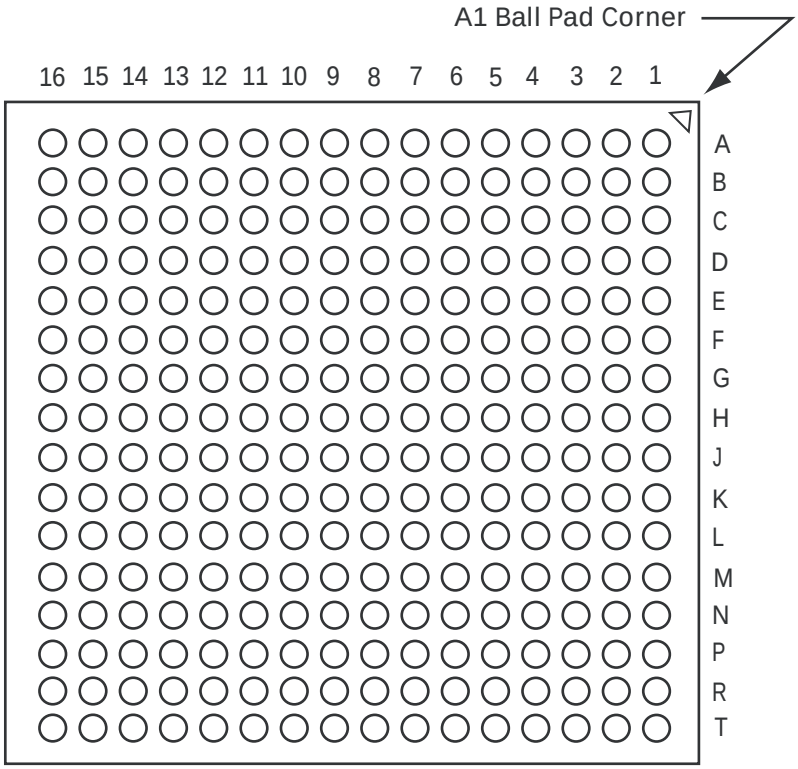
B = Bank

y = Bank number [0.7]. Bank number starting at 0 from the northwest I/O bank in a clockwise direction

Figure 57, page 68 and Table 13, page 68 are extracted from the Fusion datasheet and provide package connections for the AFS600 device. Pinouts for other devices in the Fusion family may be found in the *Fusion Family of Mixed-Signal Flash FPGAs* datasheet. This datasheet is included on the Fusion Starter Kit CD. However, the website should always be consulted for the most recent datasheet.

8.1 256-Pin FBGA (bottom view)

Figure 57 • **256-Pin FBGA**



Note: For package manufacturing and environmental information, visit the Resource Center at http://www.actel.com/products/rescenter/package/index.html.

The following table lists the pin connections for fusion starter kit board.

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board**

Pin Number	Pin Name	Starter Kit Function	Notes
A1	GND	GND	Tied to GND
A2	VCCIB0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
A3	GAA0/IO01NDB0V0	General I/O	Global
A4	GAA1/IO01PDB0V0	General I/O	Global
A5	GND	GND	Tied to GND
A6	IO10PDB0V1	General I/O	
A7	IO12PDB0V1	General I/O	
A8	IO12NDB0V1	General I/O	
A9	IO22NDB1V0	General I/O	
A10	IO22PDB1V0	General I/O	
A11	IO24NDB1V1	Pressing SW2 applies VMV1	Jumper JP12 can disconnect
A12	GND	GND	Tied to GND

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
A13	GBA0/IO28NDB1V1	Green LED D6	Jumper JP6 can disconnect
A14	IO29NDB1V1	Green LED D8	Jumper JP8 can disconnect
A15	VCCIB1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
A16	GND	GND	Tied to GND
B1	VCOMPLA	GND	Tied to GND
B2	VCCPLA	VCCPLA	Jumper JP67 ties to 1.5V_FPGA or GND
B3	IO00NDB0V0	General I/O	
B4	IO00PDB0V0	General I/O	
B5	GAB1/IO02PPB0V0	General I/O	Global
B6	IO10NDB0V1	General I/O	
B7	VCCIB0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
B8	IO18NDB1V0	General I/O	
B9	IO18PDB1V0	General I/O	
B10	VCCIB1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
B11	IO24PDB1V1	Pressing SW1 applies VMV1	Jumper JP11 can disconnect
B12	GBC0/IO26NPB1V1	Green LED D1	Jumper JP1 can disconnect
B13	GBA1/IO28PDB1V1	Green LED D5	Jumper JP5 can disconnect
B14	IO29PDB1V1	Green LED D7	Jumper JP7 can disconnect
B15	VCCPLB	VCCPLB	Jumper JP65 ties to 1.5V_FPGA or GND
B16	VCOMPLB	GND	Tied to GND
C1	VCCIB4	VMV4	Tied to 3.3V_FPGA
C2	GND	GND	Tied to GND
C3	VMV4	VMV4	Tied to 3.3V_FPGA
C4	VMV0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
C5	VCCIB0	VMV0	Jumper JP26 ties to 1.5V_FPGA or 3.3V_FPGA
C6	GAC1/IO03PDB0V0	General I/O	Global
C7	IO06NDB0V0	General I/O	
C8	IO16PDB1V0	General I/O	
C9	IO16NDB1V0	General I/O	
C10	IO25NDB1V1	Pressing SW4 applies VMV1	Jumper JP14 can disconnect

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
C11	IO25PDB1V1	Pressing SW3 applies VMV1	Jumper JP13 can disconnect
C12	VCCIB1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
C13	GBC1/IO26PPB1V1	Green LED D2	Jumper JP2 can disconnect
C14	VMV2	VMV2	Tied to 3.3V_FPGA
C15	GND	GND	Tied to GND
C16	VCCIB2	VMV2	Tied to 3.3V_FPGA
D1	IO84NDB4V0	LCD MDL4 – RS	Jumper JP46 can disconnect
D2	GAB2/IO84PDB4V0	General I/O	Global
D3	IO85NDB4V0	LCD MDL6 – ENABLE	Jumper JP47 can disconnect
D4	GAA2/IO85PDB4V0	General I/O	Global
D5	GAB0/IO02NPB0V0	General I/O	Global
D6	GAC0/IO03NDB0V0	General I/O	Global
D7	IO06PDB0V0	General I/O	
D8	IO14NDB0V1	General I/O	
D9	IO14PDB0V1	General I/O	
D10	IO23PDB1V1	General I/O	
D11	GBB0/IO27NDB1V1	Green LED D4	Jumper JP4 can disconnect
D12	VMV1	VMV1	Jumper JP25 ties to 1.5V_FPGA or 3.3V_FPGA
D13	GBA2/IO30PDB2V0	General I/O	Global
D14	IO30NDB2V0	General I/O	
D15	GBB2/IO31PDB2V0	General I/O	Global
D16	IO31NDB2V0	General I/O	
E1	GND	GND	Tied to GND
E2	IO81NDB4V0	LCD MDL14 – Bit3	Jumper JP41 can disconnect
E3	IO81PDB4V0	LCD MDL13 – Bit2	Jumper JP42 can disconnect
E4	VCCIB4	VMV4	Tied to 3.3V_FPGA
E5	IO83NPB4V0	LCD MDL5 – R/W	Jumper JP45 can disconnect
E6	IO04NPB0V0	General I/O	
E7	GND	GND	Tied to GND
E8	IO08PDB0V1	General I/O	
E9	IO20NDB1V0	General I/O	
E10	GND	GND	Tied to GND

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
E11	GBB1/IO27PDB1V1	Green LED D3	Jumper JP3 can disconnect
E12	IO33PSB2V0	General I/O	
E13	VCCIB2	VMV2	Tied to 3.3V_FPGA
E14	IO32NDB2V0	General I/O	
E15	GBC2/IO32PDB2V0	Global IO	
E16	GND	GND	Tied to GND
F1	IO79NDB4V0	J13 pin 5	J13 is 40-pin IP header
F2	IO79PDB4V0	J13 pin 6	J13 is 40-pin IP header
F3	IO76NDB4V0	J13 pin 7	J13 is 40-pin IP header
F4	IO76PDB4V0	J13 pin 8	J13 is 40-pin IP header
F5	IO82PSB4V0	LCD MDL12 – Bit1	Jumper JP43 can disconnect
F6	GAC2/IO83PPB4V0	LCD MDL11 – Bit0	Jumper JP44 can disconnect
F7	IO04PPB0V0	General I/O	
F8	IO08NDB0V1	General I/O	
F9	IO20PDB1V0	General I/O	
F10	IO23NDB1V1	General I/O	
F11	IO36NDB2V0	General I/O	
F12	IO36PDB2V0	General I/O	
F13	IO39NDB2V0	General I/O	
F14	GCA2/IO39PDB2V0	General I/O	Global
F15	GCB2/IO40PDB2V0	General I/O	Global
F16	IO40NDB2V0	General I/O	
G1	IO74NPB4V0	J13 pin 11	J13 is 40-pin IP header
G2	VCCIB4	VMV4	Tied to 3.3V_FPGA
G3	GFB2/IO74PPB4V0	J13 pin 12	J13 is 40-pin IP header
G4	GFA2/IO75PDB4V0	J13 pin 10	J13 is 40-pin IP header
G5	GND	GND	Tied to GND
G6	IO75NDB4V0	J13 pin 9	J13 is 40-pin IP header
G7	GND	GND	Tied to GND
G8	VCC	1.5V_FPGA	
G9	GND	GND	Tied to GND
G10	VCC	1.5V_FPGA	
G11	GCC0/IO43NDB2V0	General I/O	Global
G12	GND	GND	Tied to GND
G13	GCC1/IO43PDB2V0	General I/O	Global
G14	IO41NPB2V0	General I/O	

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
G15	VCCIB2	VMV2	Tied to 3.3V_FPGA
G16	GCC2/IO41PPB2V0	General I/O	Global
H1	GFC2/IO73PDB4V0	J13 pin 14	J13 is 40-pin IP header
H2	IO73NDB4V0	J13 pin 13	J13 is 40-pin IP header
H3	XTAL2	Pin 2 of crystal Y1	Y1 is 32.768 kHz
H4	XTAL1	Pin 1 of crystal Y1	Y1 is 32.768 kHz
H5	GNDOSC	GND	Tied to GND
H6	VCCOSC	3.3V_FPGA	
H7	VCC	1.5V_FPGA	
H8	GND	GND	Tied to GND
H9	VCC	1.5V_FPGA	
H10	GND	GND	Tied to GND
H11	IO47NDB2V0	General I/O	
H12	IO47PDB2V0	General I/O	
H13	GCA1/IO45PDB2V0	General I/O	Global
H14	GCA0/IO45NDB2V0	General I/O	Global
H15	GCB0/IO44NDB2V0	General I/O	Global
H16	GCB1/IO44PDB2V0	General I/O	Global
J1	GFA0/IO70NDB4V0	J13 pin 19	J13 is 40-pin IP header
J2	GFA1/IO70PDB4V0	J13 pin 20	J13 is 40-pin IP header
J3	GFB0/IO71NDB4V0	J13 pin 17	J13 is 40-pin IP header
J4	GFB1/IO71PDB4V0	J13 pin 18	J13 is 40-pin IP header
J5	GFC0/IO72NDB4V0	J13 pin 15	J13 is 40-pin IP header
J6	GFC1/IO72PDB4V0	J13 pin 16	J13 is 40-pin IP header
J7	GND	GND	Tied to GND
J8	VCC	1.5V_FPGA	
J9	GND	GND	Tied to GND
J10	VCC	1.5V_FPGA	
J11	IO56NPB2V0	General I/O	
J12	GDB0/IO53NPB2V0	General I/O	Global
J13	GDA1/IO54PDB2V0	General I/O	Global
J14	GDC1/IO52PPB2V0	General I/O	Global
J15	IO51NSB2V0	General I/O	
J16	GDC0/IO52NPB2V0	General I/O	Global
K1	IO67NPB4V0	J13 pin 21	J13 is 40-pin IP header
K2	VCCIB4	VMV4	Tied to 3.3V_FPGA
K3	IO67PPB4V0	J13 pin 22	J13 is 40-pin IP header

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
K4	IO65PDB4V0	J13 pin 24	J13 is 40-pin IP header
K5	GND	GND	Tied to GND
K6	IO65NDB4V0	J13 pin 23	J13 is 40-pin IP header
K7	VCC	1.5V_FPGA	
K8	GND	GND	Tied to GND
K9	VCC	1.5V_FPGA	
K10	GND	GND	Tied to GND
K11	GDC2/IO57PPB2V0	Pressing SW5 gives one-shot “global” pulse	Jumper JP15 can disconnect. Silkscreen labeled incorrectly as “reset”.
K12	GND	GND	Tied to GND
K13	GDA0/IO54NDB2V0	General I/O	Global
K14	GDA2/IO55PPB2V0	General I/O	Global
K15	VCCIB2	VMV2	Tied to 3.3V_FPGA
K16	GDB1/IO53PPB2V0	General I/O	Global
L1	GEC1/IO63PDB4V0	J13 pin 26	J13 is 40-pin IP header
L2	GEC0/IO63NDB4V0	J13 pin 25	J13 is 40-pin IP header
L3	GEB1/IO62PDB4V0	J13 pin 28	J13 is 40-pin IP header
L4	GEB0/IO62NDB4V0	J13 pin 27	J13 is 40-pin IP header
L5	IO60NDB4V0	J13 pin 31	J13 is 40-pin IP header
L6	GEC2/IO60PDB4V0	J13 pin 32	J13 is 40-pin IP header
L7	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins.
L8	AC2	Test point TP53 for 1.5 V FPGA current sense	Jumper JP64 can disconnect
L9	AV4	1.5 V of fan control circuit for current sense	Jumper JP33 can disconnect
L10	AC5	Current sense of 3.3 V fan circuit	Jumper JP38 can disconnect
L11	PTEM		
L12	TDO	TDO	To FlashPro3 header J1 pin 3 (if J5 is across pins 3 and 4 as last device) and as TDI to J2 pin 9
L13	VJTAG	VJTAG	Jumper JP27 allows setting to either 3.3 V or 1.5 V
L14	IO57NPB2V0		

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
L15	GDB2/IO56PPB2V0	Pressing SW6 gives one-shot “reset” pulse	Jumper JP16 can disconnect. Silkscreen labeled incorrectly as “global”.
L16	IO55NPB2V0	General I/O	
M1	GND	GND	Tied to GND
M2	GEA1/IO61PDB4V0	J13 pin 30	J13 is 40-pin IP header
M3	GEA0/IO61NDB4V0	J13 pin 29	J13 is 40-pin IP header
M4	VCCIB4	VMV4	Tied to 3.3V_FPGA
M5	IO58NPB4V0	J13 pin 35	J13 is 40-pin IP header
M6	AV0	Analog voltage from R50 potentiometer	Jumper JP53 can disconnect. Voltage varies from 0 V to 5 V.
M7	AC1	Test point TP50 for 3.3 V FPGA current sense	Jumper JP51 can disconnect
M8	AG3	Gate of p-channel MOSFET Q5 driving tricolor LED	Jumper JP60 can disconnect
M9	AC4	Current sense of 1.5 V fan circuit	Jumper JP34 can disconnect
M10	AC6	AC6	Unfiltered
M11	AG7	Active low for orange part of tricolor LED	Jumper JP70 can disconnect. AG7 should be set to 25 mA.
M12	VPUMP	3.3 V programming	Jumper JP54 connects the board supplied voltage otherwise provided by FlashPro3.
M13	VCCIB2	VMV2	Tied to 3.3V_FPGA
M14	TMS	TMS	From FlashPro3 header J1 pin 5
M15	TRST	TRST	From FlashPro3 header J1 pin 8
M16	GND	GND	Tied to GND
N1	GEB2/IO59PDB4V0	J13 pin 34	J13 is 40-pin IP header
N2	IO59NDB4V0	J13 pin 33	J13 is 40-pin IP header
N3	GEA2/IO58PPB4V0	J13 pin 36	J13 is 40-pin IP header
N4	VCC33PMP	3.3V_FPGA	
N5	VCC15A	1.5V_FPGA	
N6	AG0	AG0	Unfiltered
N7	AC3	Test point TP59 for current flow through multicolor LED	Jumper JP30 can disconnect

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
N8	AG5	Gate of n-channel MOSFET Q7 for 3.3 V fan control	Jumper JP39 can disconnect
N9	AV5	3.3 V of fan control circuit for current sense	Jumper JP37 can disconnect
N10	AG6	Active low for blue part of tricolor LED	Jumper JP69 can disconnect. AG6 should be set to 25 mA.
N11	AC8	AC8	Optional filtering available
N12	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins.
N13	VCC33A	3.3V_FPGA	
N14	VCCNVM	1.5V_FPGA	
N15	TCK	TCK	From FlashPro3 header J1 pin 1
N16	TDI	TDI	From FlashPro3 header J1 pin 9
P1	VCCNVM	1.5V_FPGA	
P2	GNDNVM	GND	Tied to GND
P3	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins.
P4	AC0	AC0	Unfiltered
P5	AG1	AG1	Unfiltered
P6	AV1	Test point TP48 for 3.3 V FPGA current sense	Jumper JP49 can disconnect
P7	AG2	AG2	Unfiltered
P8	AG4	Gate of n-channel MOSFET Q6 for 1.5 V fan control	Jumper JP35 can disconnect
P9	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins.
P10	AC7	AC7	Unfiltered
P11	AV8	AV8	Optional filtering available
P12	AG8	Active low for green part of tricolor LED	Jumper JP71 can disconnect. AG8 should be set to 25 mA.
P13	AV9	AV9	Optional filtering available
P14	ADCGNDREF	Tied to analog ground	

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
P15	PTBASE	Base of Q1 pass transistor for 1.5 V internal generation	Jumper JP28 selects 1.5 V internal (Q1 pass transistor) or 1.5 V external (U15 regulator).
P16	GNDNVM	GND	Tied to GND
R1	VCCIB4	VMV4	Tied to 3.3V_FPGA
R2	PCAP	PCAP	
R3	AT1	AT1	Unfiltered
R4	AT0	AT0	Unfiltered
R5	AV2	Test point TP51 for 1.5 V FPGA current sense	Jumper JP52 can disconnect
R6	AT2	AT2	Unfiltered
R7	AV3	Test point TP58 for current flow through multicolor LED	Jumper JP29 can disconnect
R8	AT5	AT5	Unfiltered
R9	AV6	AV6	Unfiltered
R10	AT7	AT7	Unfiltered
R11	AV7	AV7	Unfiltered
R12	AT9	Base-collector of Q8 temperature diode	Jumper JP62 can disconnect
R13	AG9	AG9	Unfiltered
R14	AC9	AC9	Optional filtering available
R15	PUB	SW7	Pressing SW7 momentarily takes R15 to GND.
R16	VCCIB2	VMV2	Tied to 3.3V_FPGA
T1	GND	GND	Tied to GND
T2	NCAP	NCAP	
T3	VCC33N	VCC33N	Available on header pin
T4	ATRTN0	ATRTN0	
T5	AT3	AT3	Unfiltered
T6	ATRTN1	ATRTN1	Unfiltered
T7	AT4	AT4	Unfiltered
T8	ATRTN2	ATRTN2	Unfiltered
T9	AT6	AT6	Unfiltered
T10	ATRTN3	ATRTN3	Unfiltered
T11	AT8	AT8	Unfiltered
T12	ATRTN4	Emitter of Q8 temperature diode	Jumper JP68 can disconnect

Table 13 • **AFS600-FG256 Pin Connections for Fusion Starter Kit Board *(continued)***

Pin Number	Pin Name	Starter Kit Function	Notes
T13	GNDA	GNDA	Analog ground is on a separate plane and joined to digital ground at regulator U15 ground pins.
T14	VCC33ACAP	VCC33ACAP	
T15	VAREF	User VAREF	Shrouded header JP74 can be used to supply User VAREF.
T16	GND	GND	Tied to GND

9 Appendix: Board Schematics

This section provides illustrations of the Fusion Evaluation Board.

9.1 Top-Level View

Figure 58, page 78 illustrates a view of the top of the Fusion Evaluation Board. Figure 59, page 79 and Figure 60, page 80 illustrate views of the bottom of the Fusion Evaluation Board.

Figure 58 • **Top View of Fusion Evaluation Board**

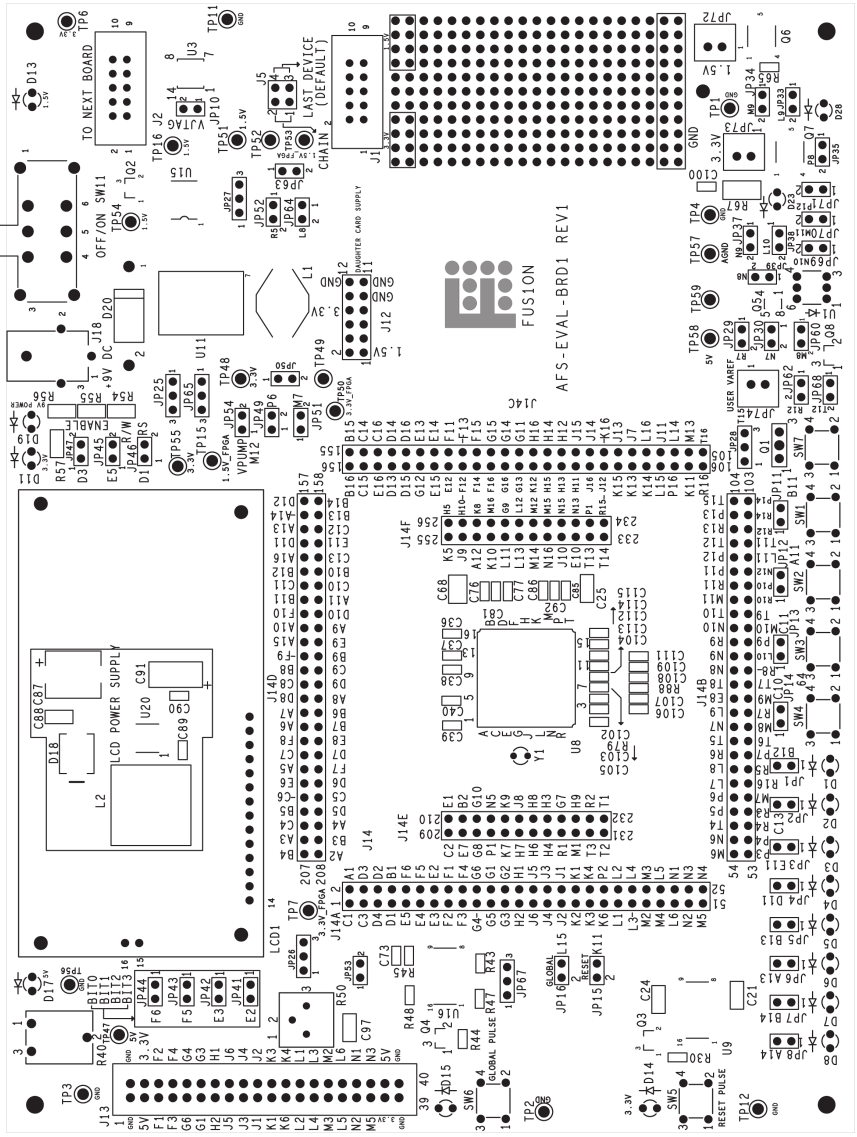


Figure 59 • **Bottom View of Fusion Evaluation Board (viewed from above)**

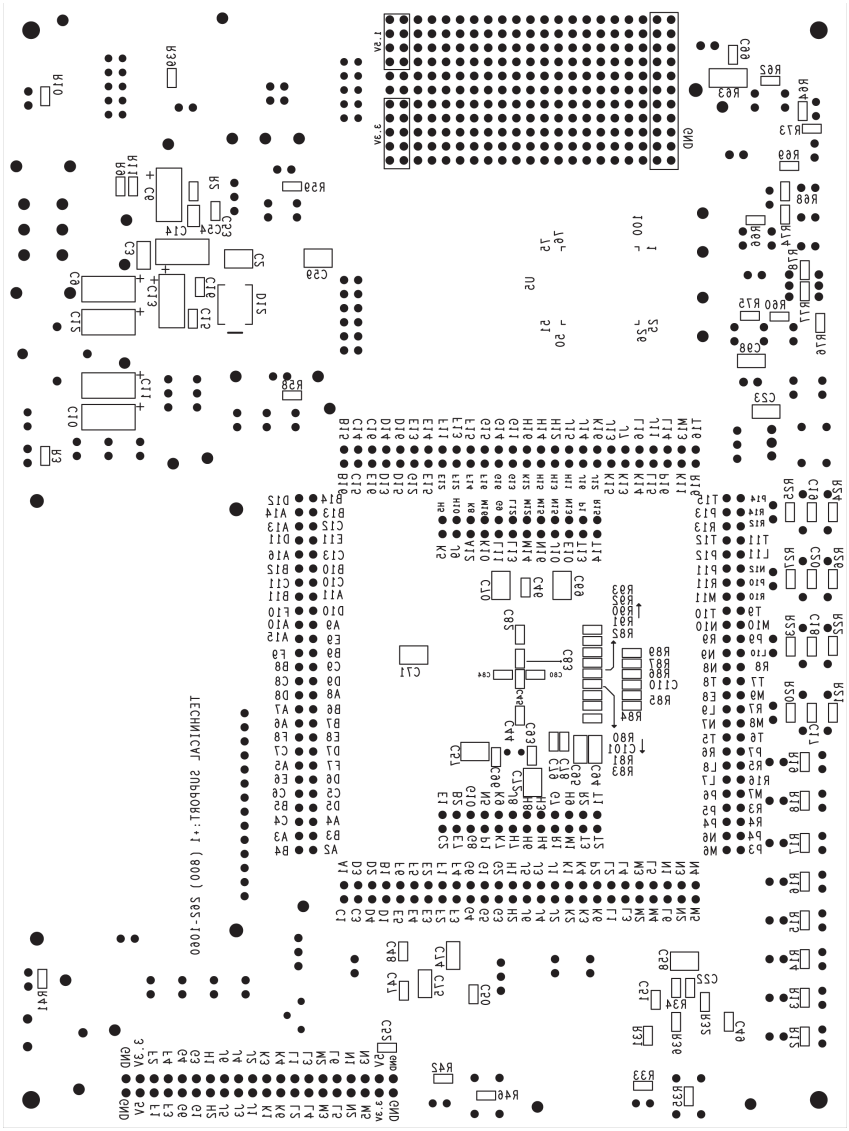
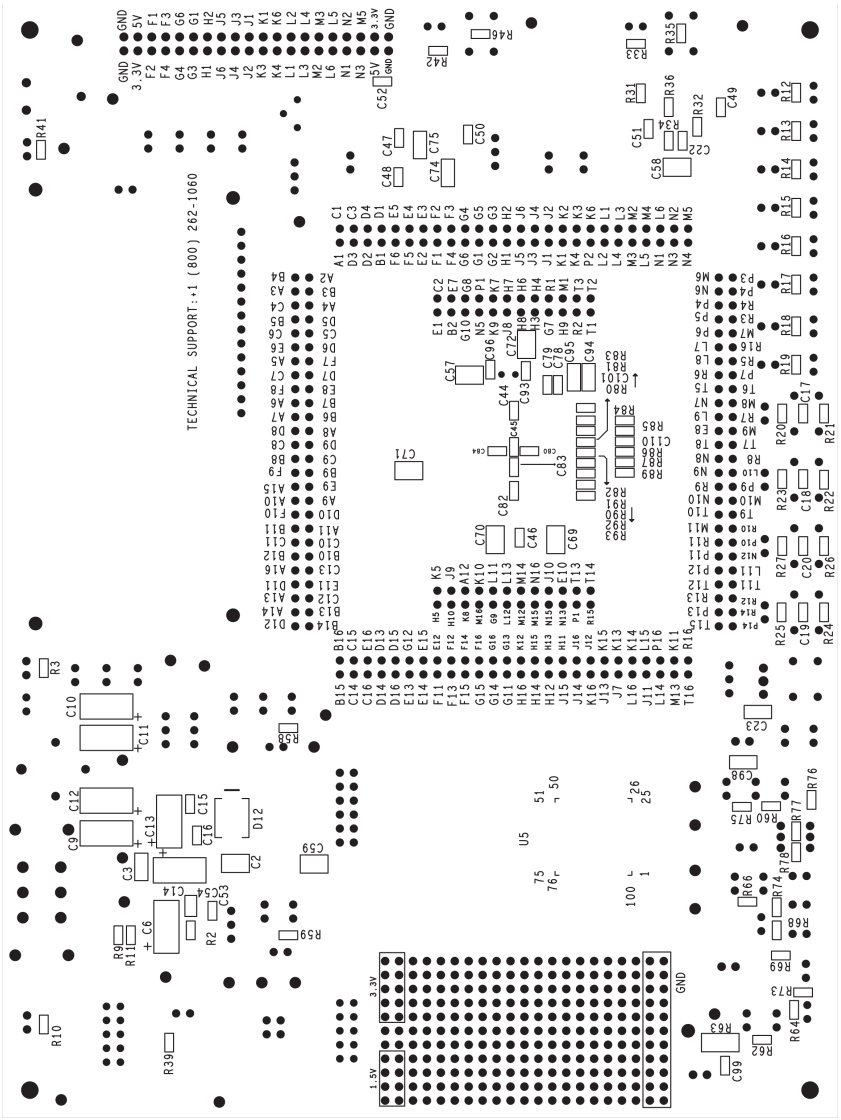


Figure 60 • **Bottom View of Fusion Evaluation Board (viewed from below)**



9.2 Fusion Schematics

The following illustrations shows the schematics of the Fusion Starter Kit board.

Figure 61 • **Power Supplies and Indication**

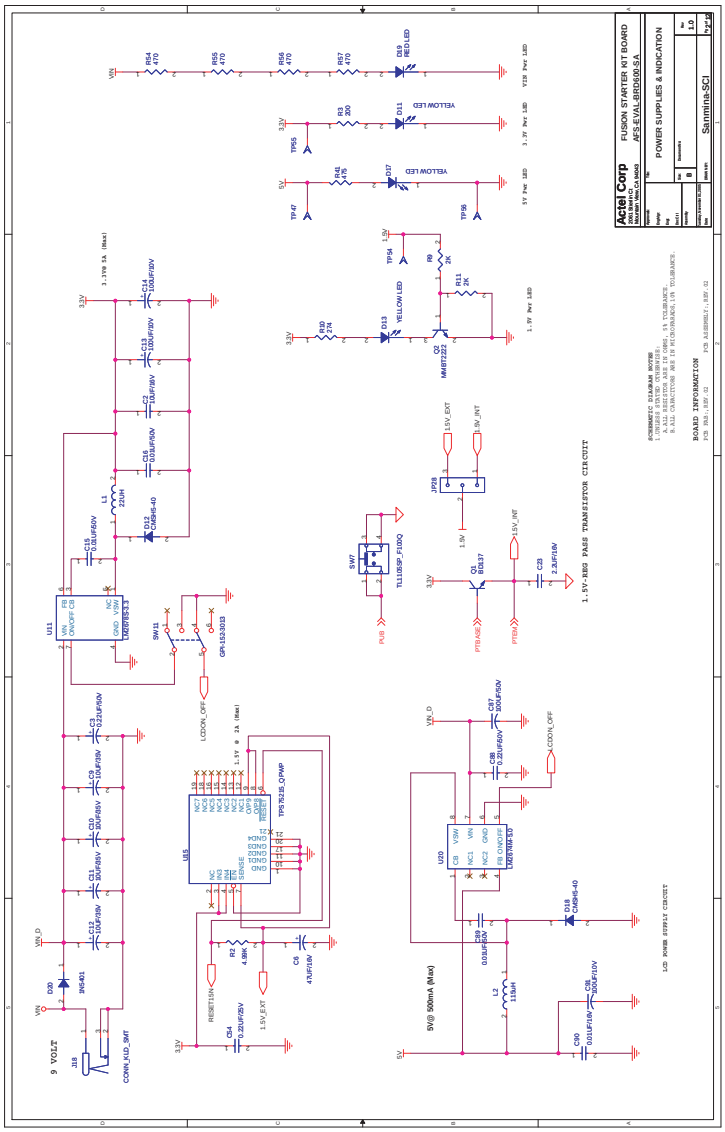


Figure 62 • **Bank 2 and Bank 4 I/O**

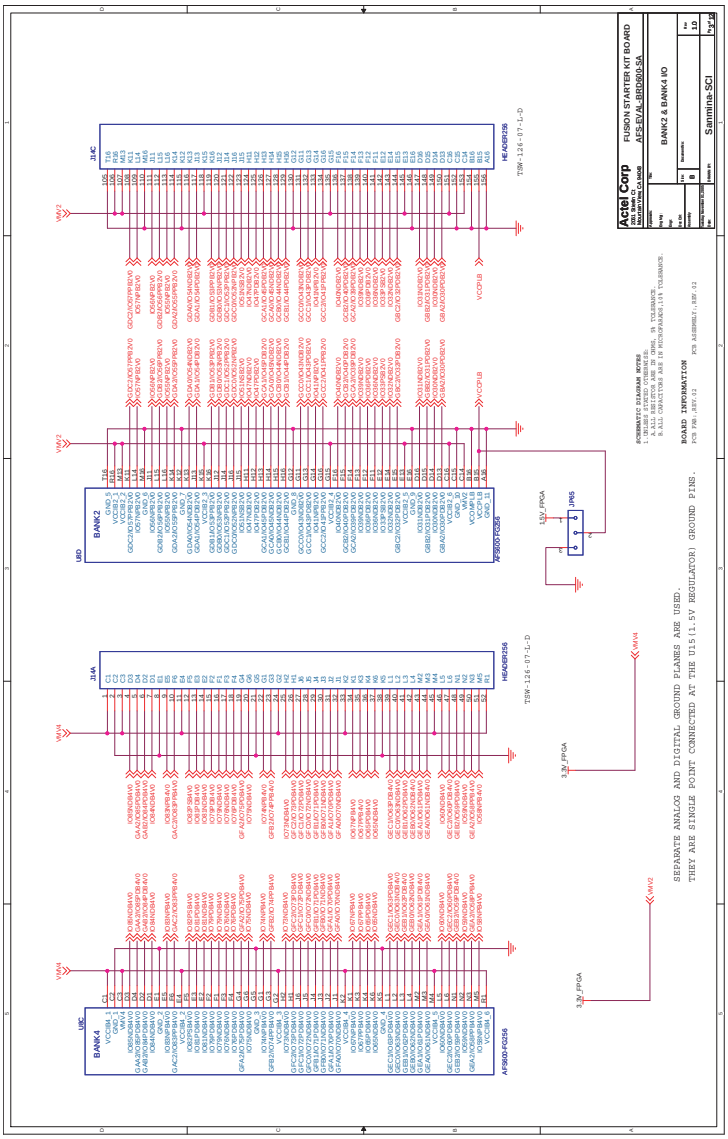


Figure 63 • **Bank 0, Bank 1, and Analog I/O**

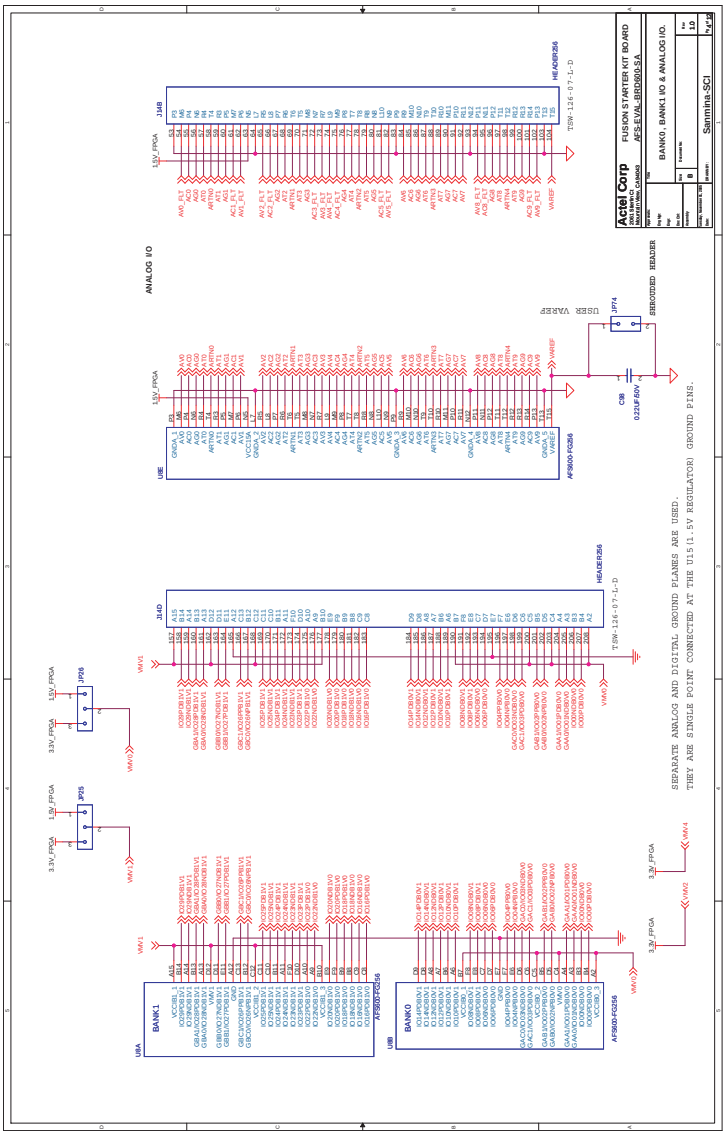


Figure 64 • **VCC, GND, and JTAG**

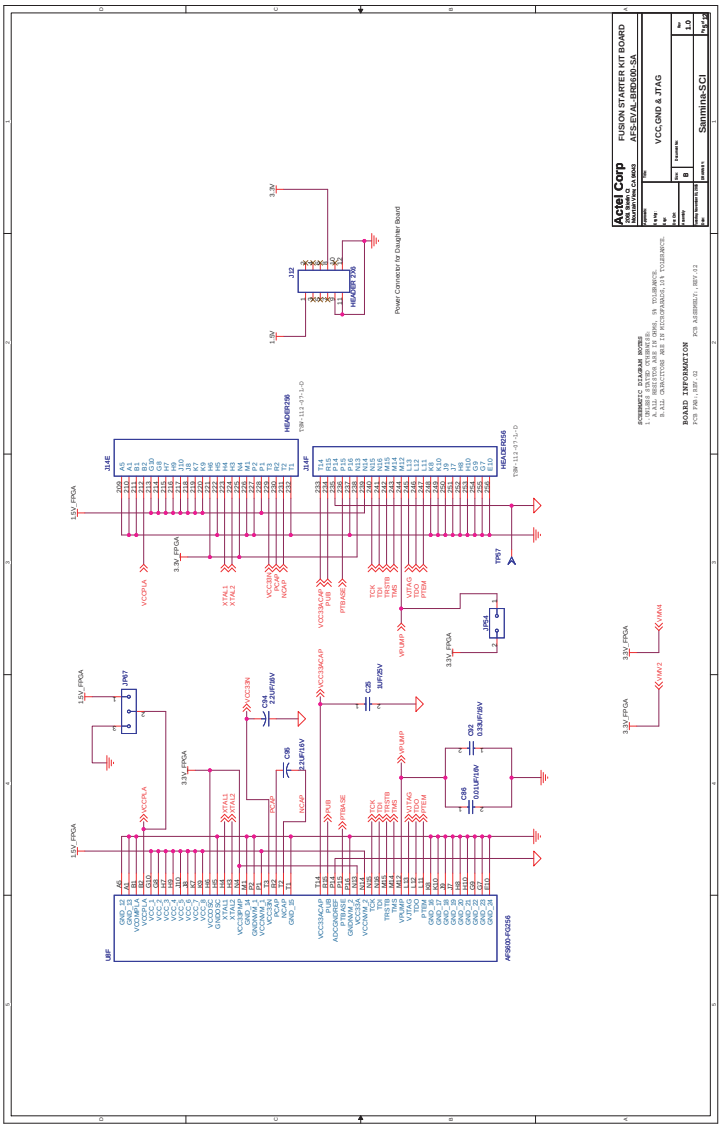


Figure 65 • **LED and LCD Module Interface**

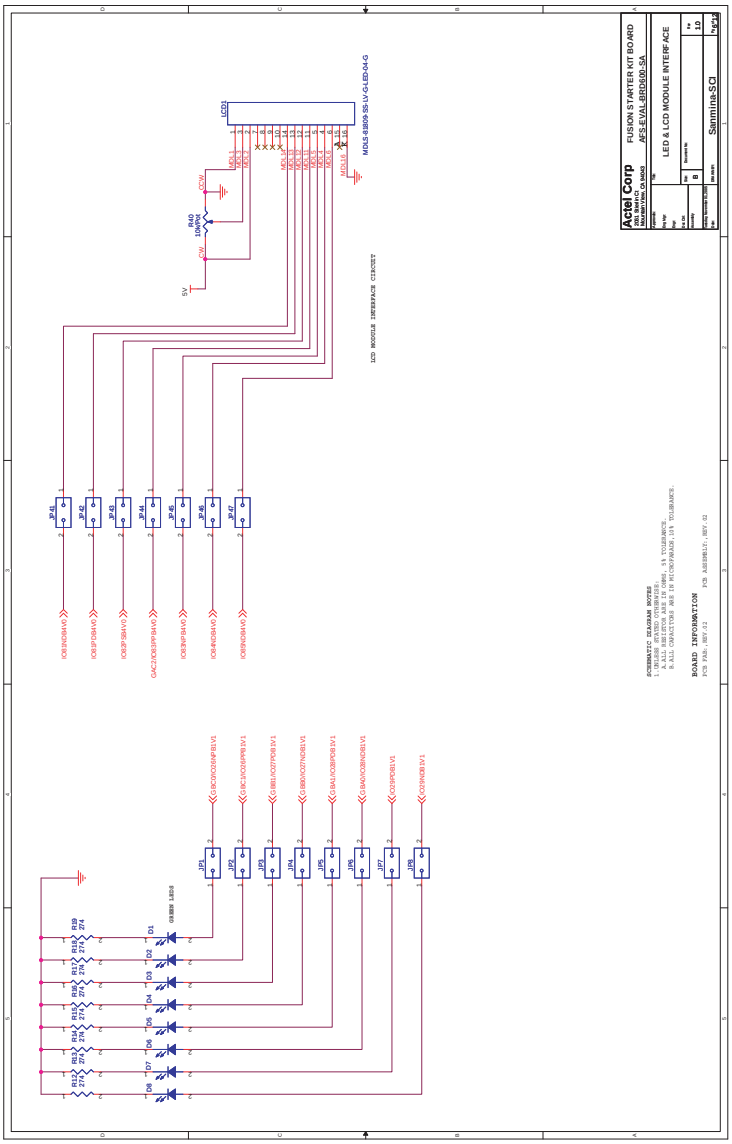


Figure 66 • **Push Button Interface and 40-Pin Header**

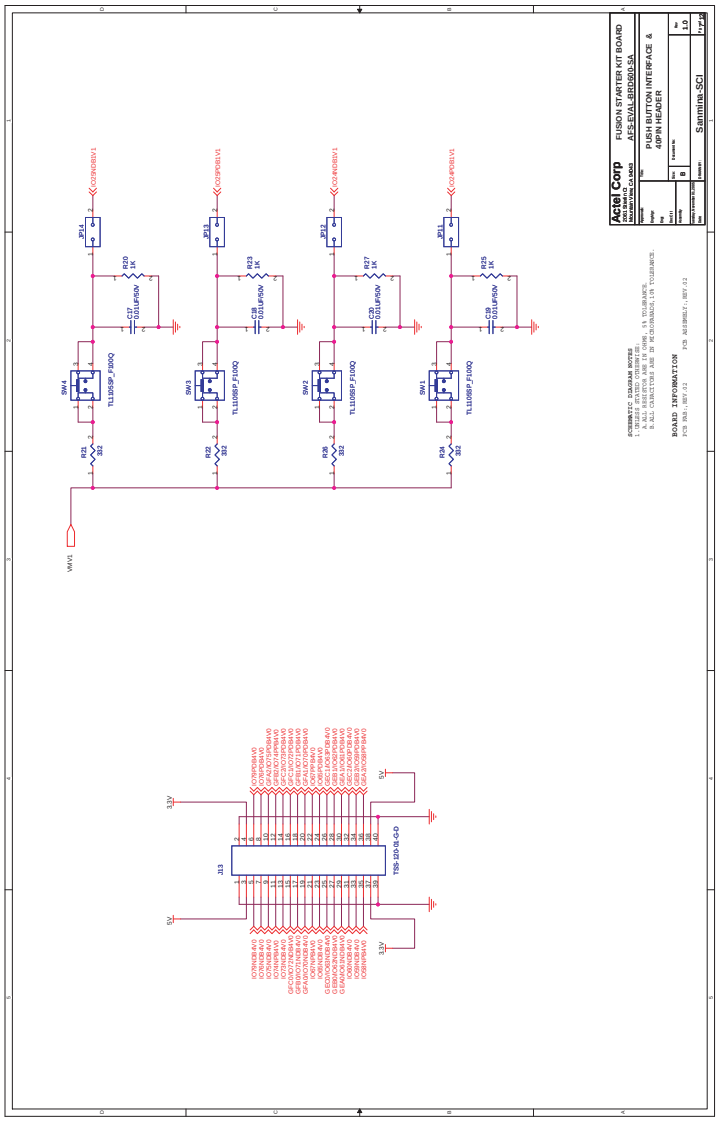


Figure 67 • **Pulse Generator for Reset and Global**

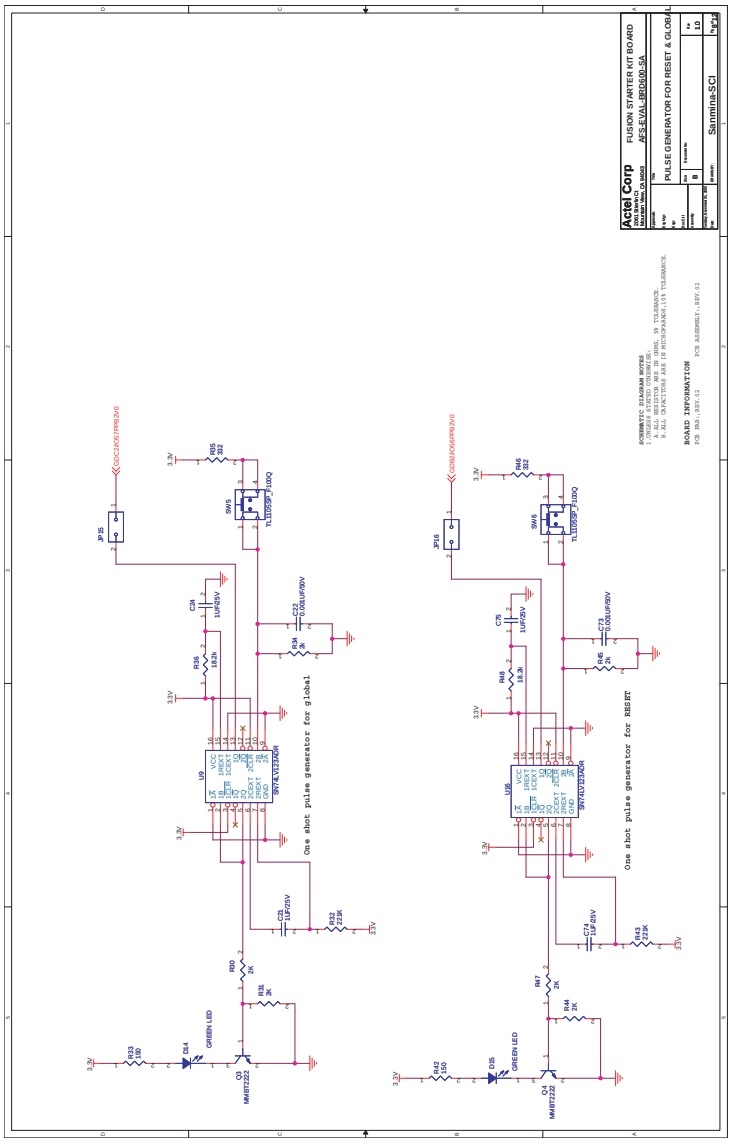


Figure 68 • **JTAG and JTAG Daisy Chain Connector**

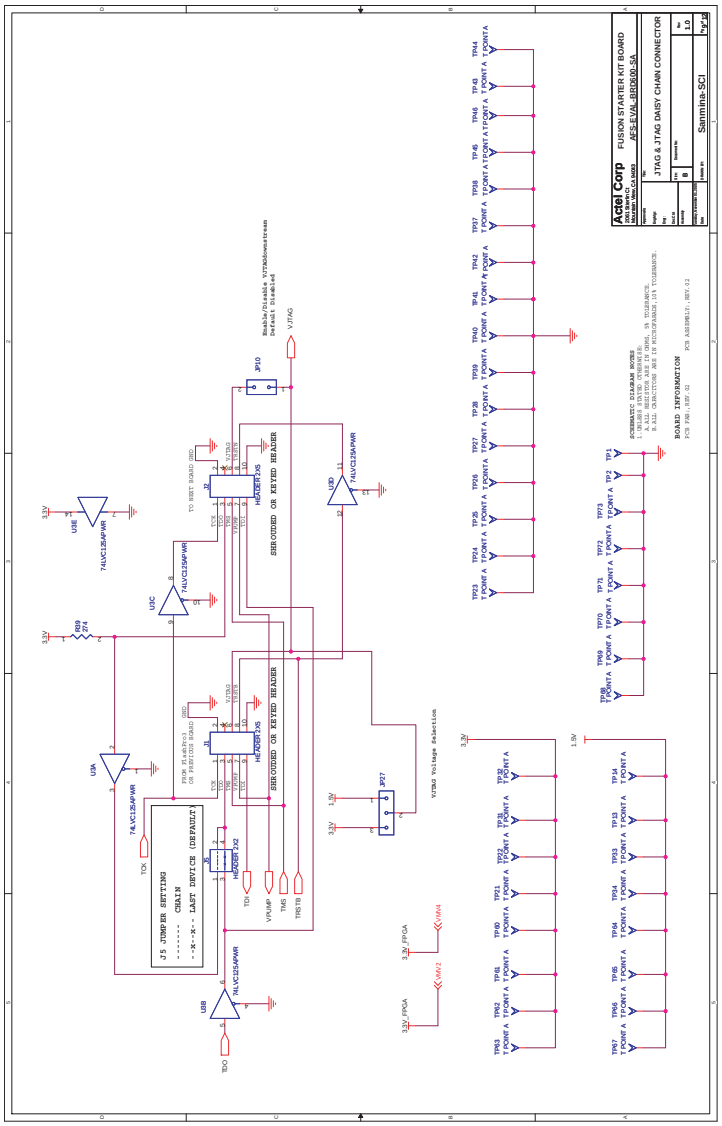


Figure 69 • **Decoupling Capacitors**

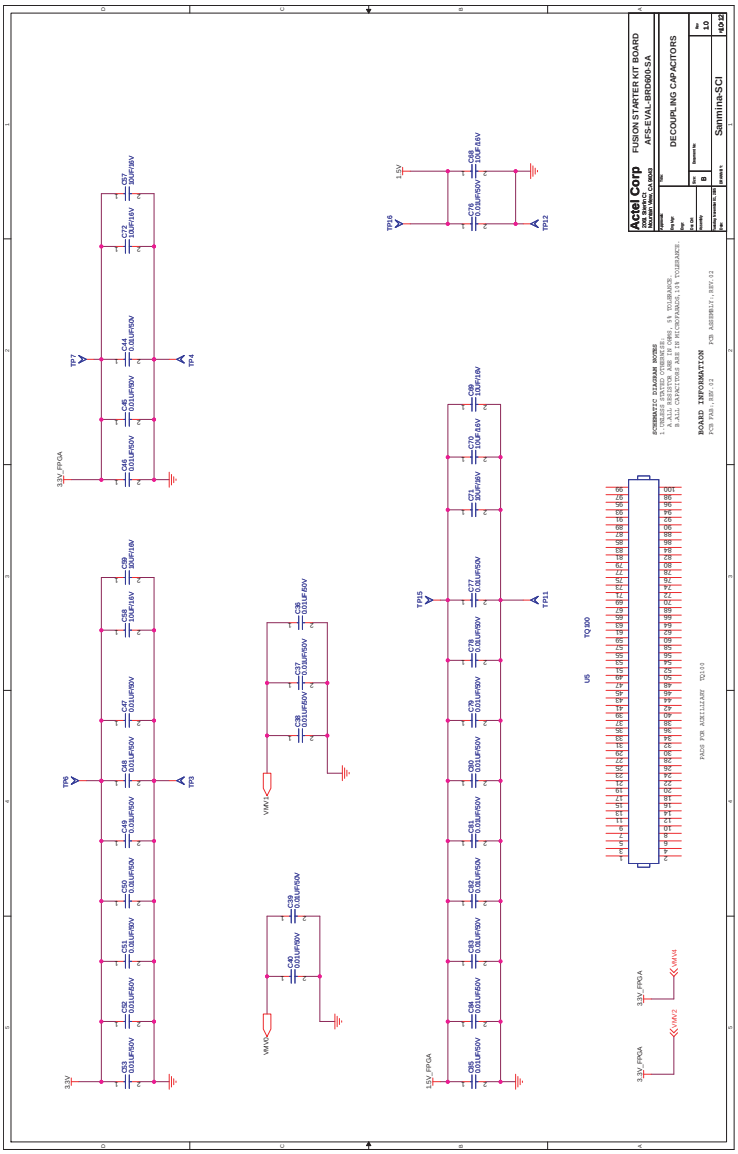


Figure 70 • **Crystal, 1.5 V and 3.3 V Current Sense, Temperature Diode, and Pot**

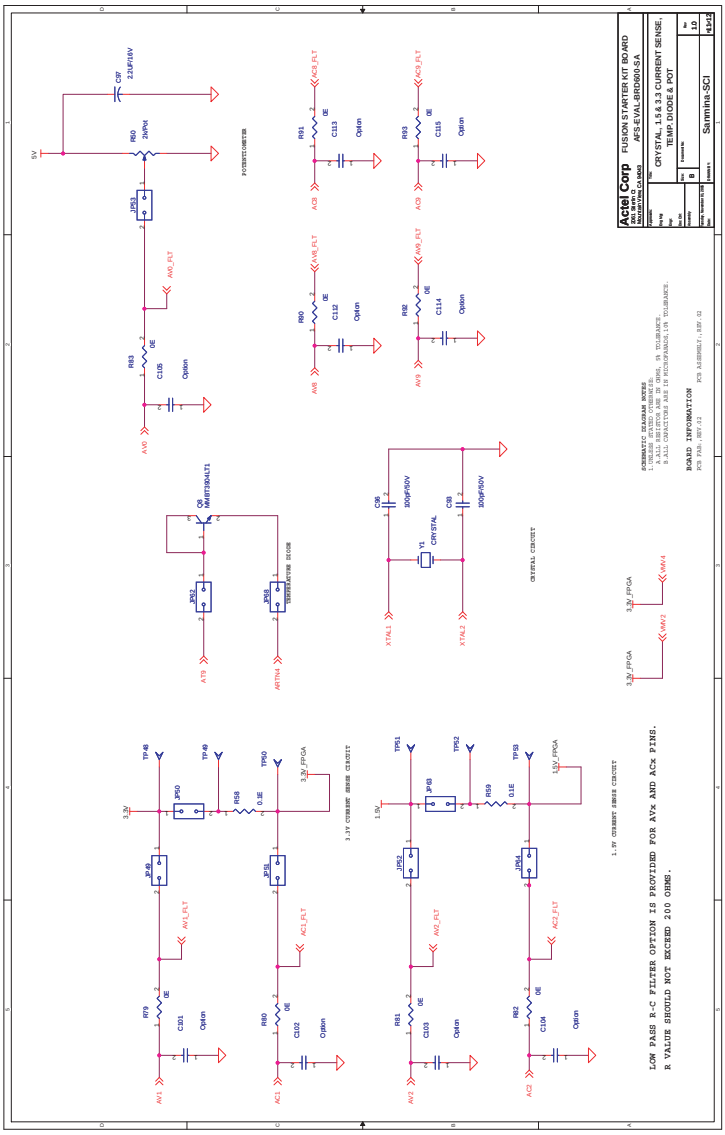
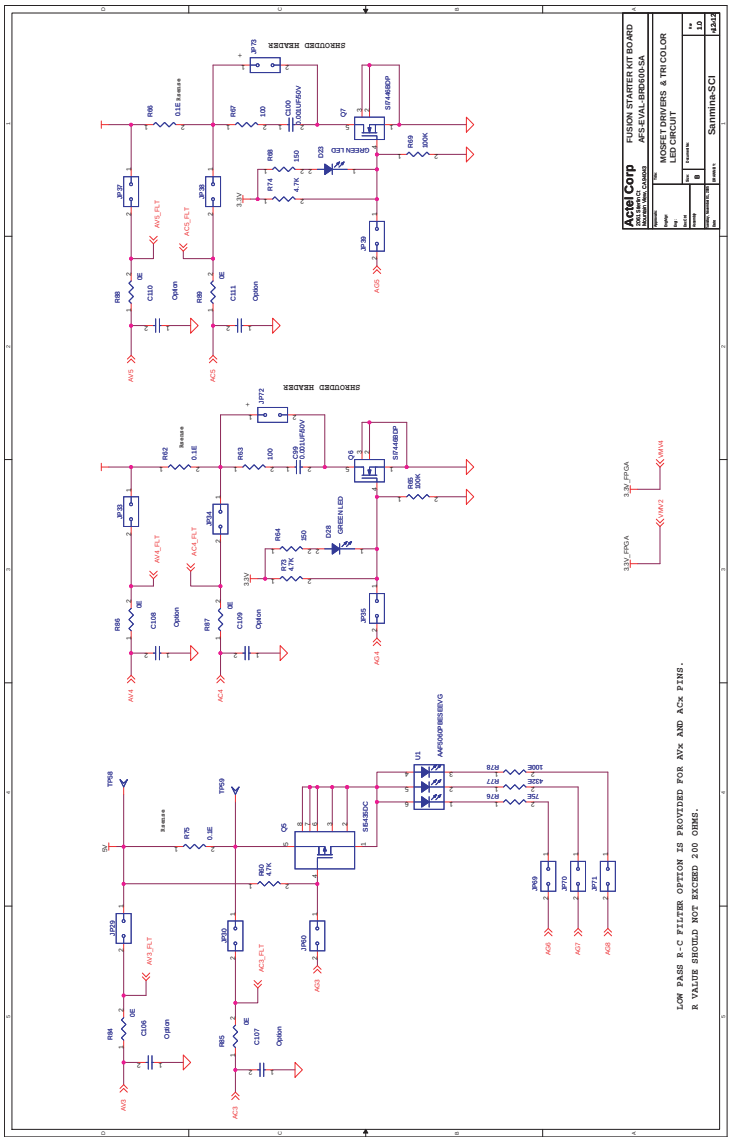


Figure 71 • **MOSFET Drivers and Tricolor LED Circuit**



10 Appendix: Signal Layers

The Fusion Evaluation Board is a six-layer board, with the following layers of copper:

Layer 1 – Top signal layer (see Figure 72, page 93)

Layer 2 – Ground plane

Layer 3 – Signal layer (see Figure 73, page 94)

Layer 4 – Signal layer (see Figure 74, page 95)

Layer 5 – Power plane

Layer 6 – Bottom signal layer (see Figure 75, page 96 and Figure 76, page 97)

10.1 Errata

The REV1 silkscreen does have some errors with regard to pin labeling on the silkscreen. The pin names shown in the following table do not match in the schematics and silkscreen for connector J14C.

Table 14 • **Actual Correspondence between Mismatched Pin Labels**

Schematics	Silkscreen
M16	P‘16
K12	J7
G12	K12
E16	G12
C15	E16
B16	C16
A16	B16

These pins are connected to a common ground, so this problem would not cause you to inadvertently use a wrong pin. This discrepancy is pointed out in case you are using the pins for general purposes and have concerns over the discrepancy.

Figure 72 • **Layer 1 – Top Signal Layer**

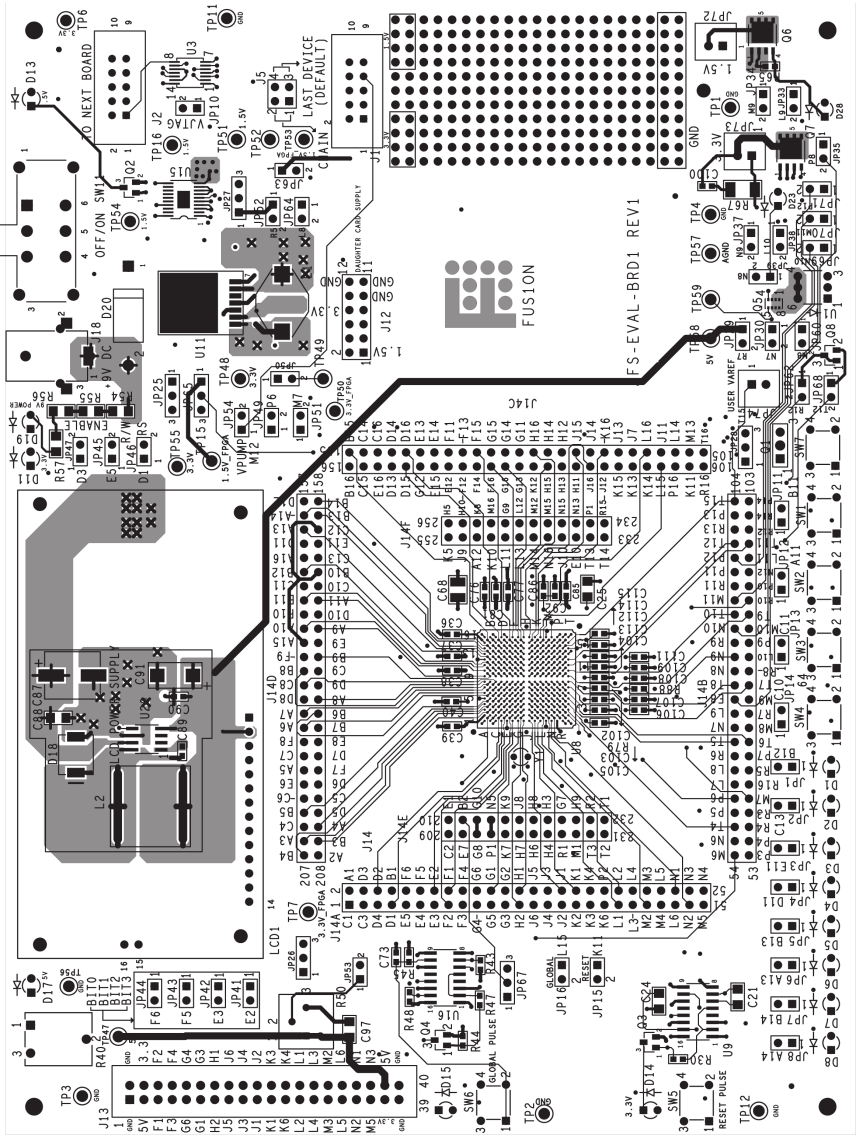


Figure 73 • **Layer 3 – Signal Layer**

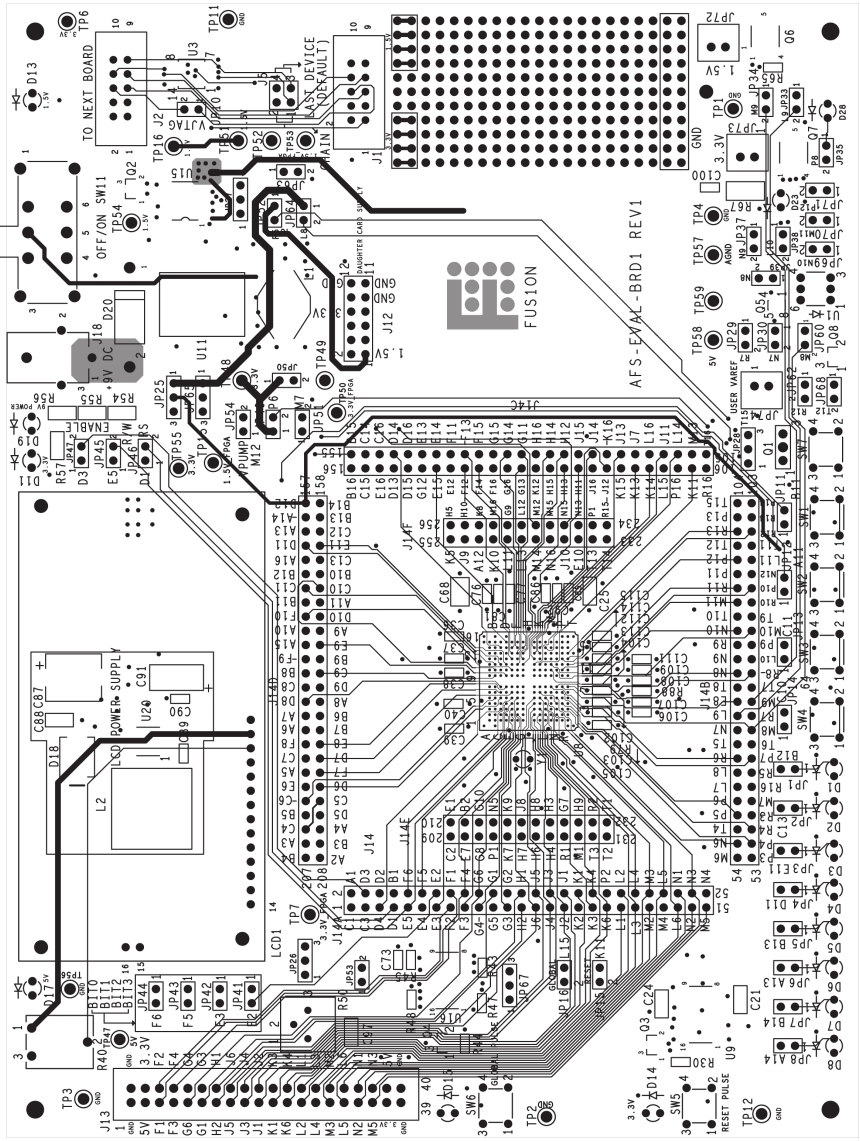


Figure 74 • **Layer 4 – Signal Layer**

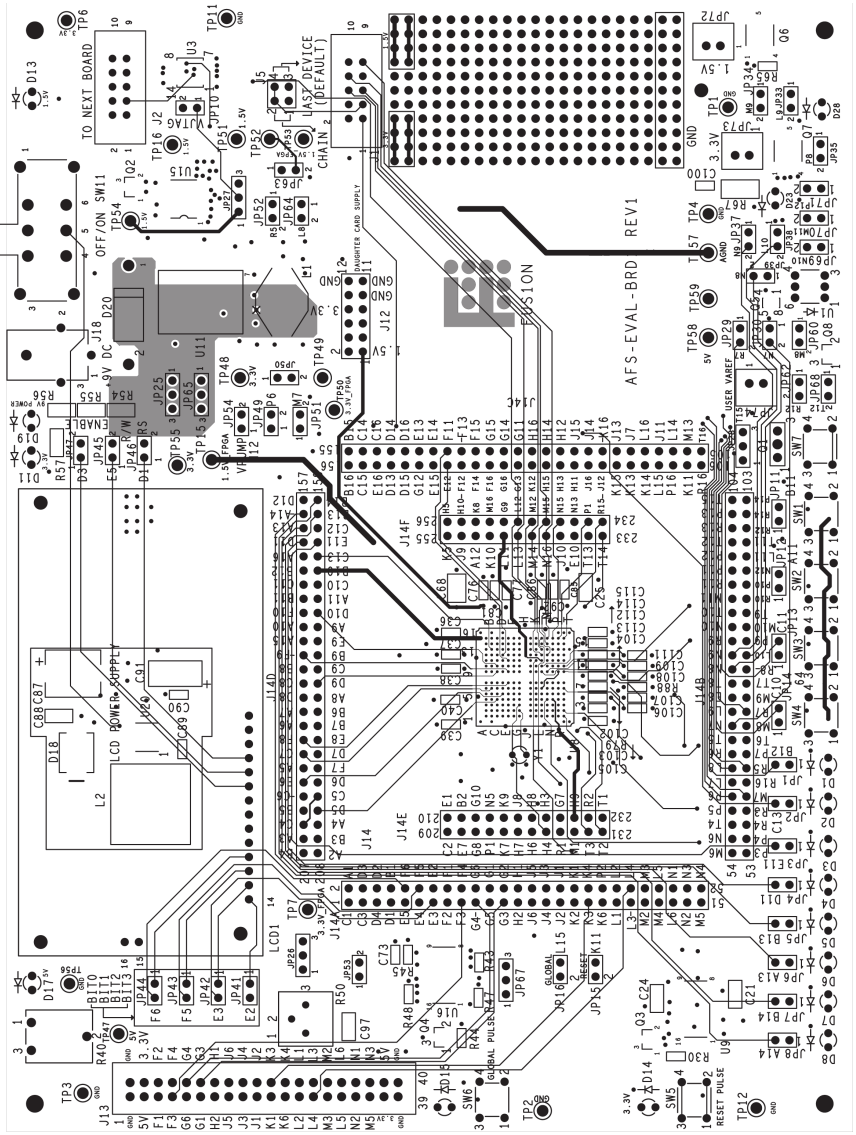


Figure 75 • **Layer 6 – Bottom Signal Layer (viewed from above)**

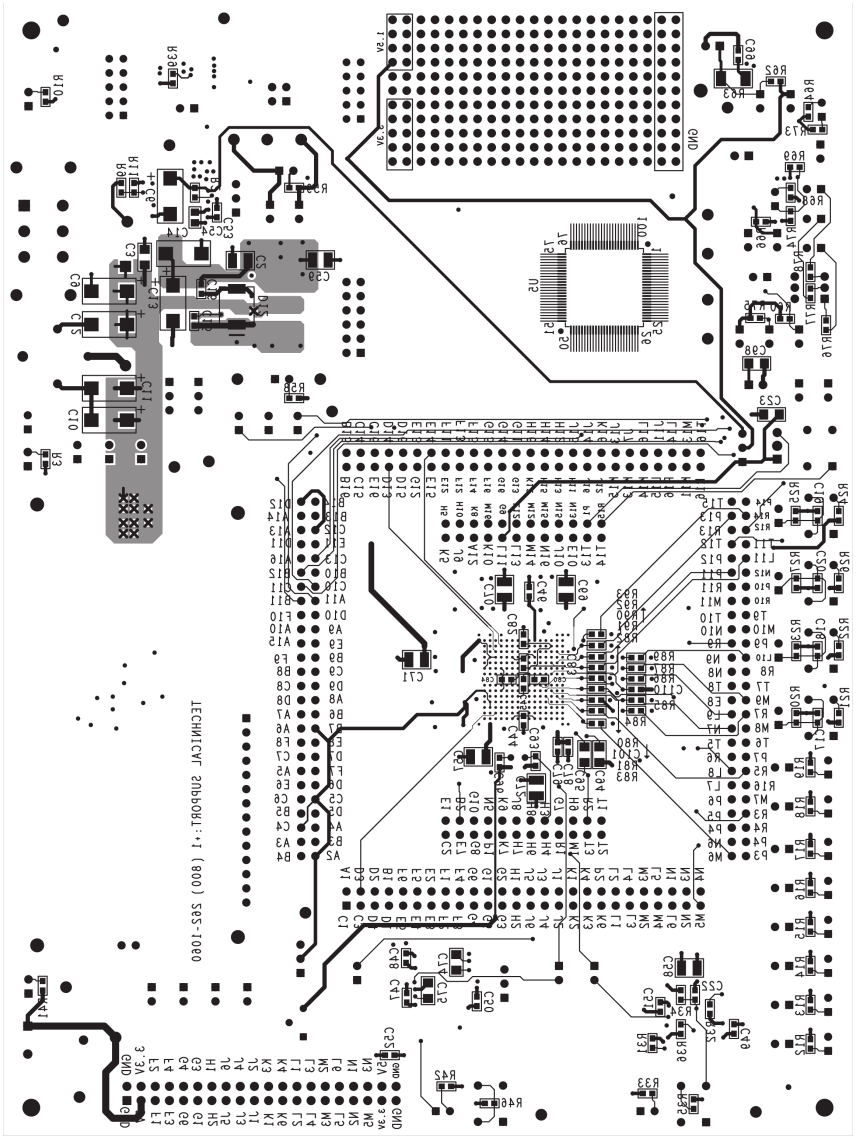
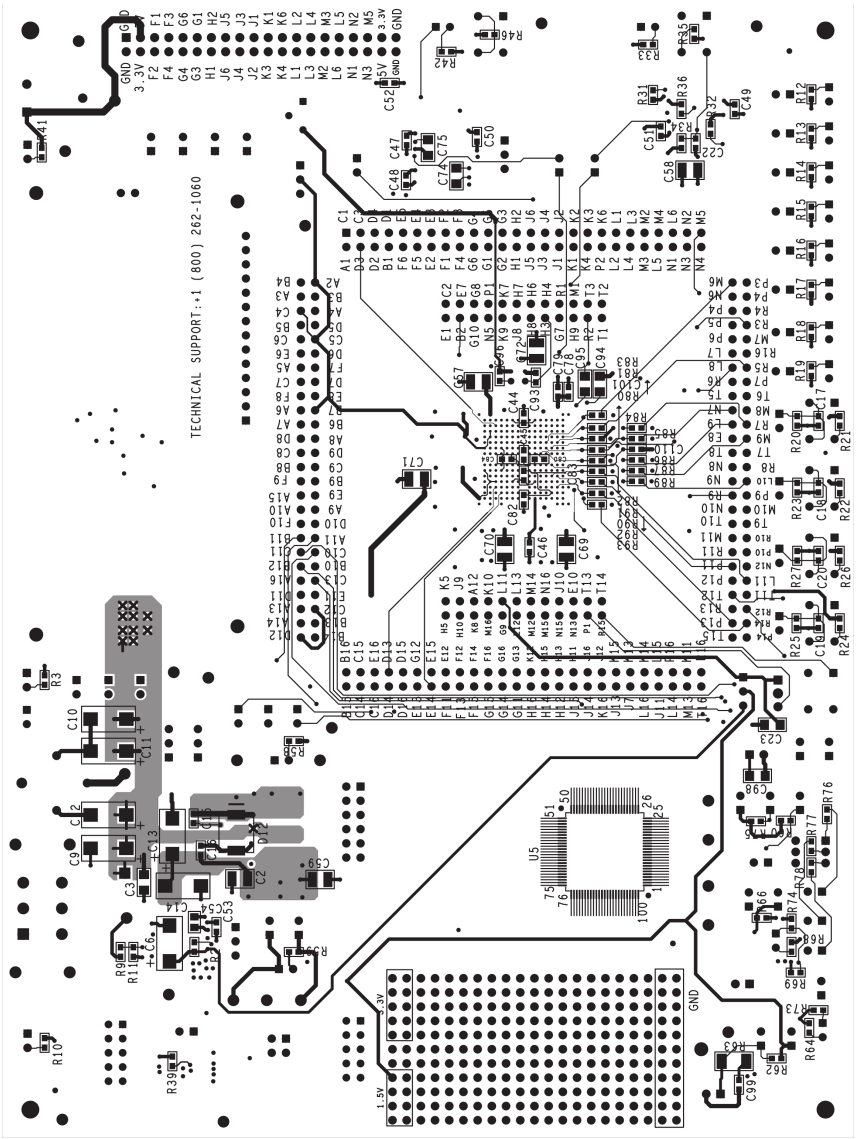


Figure 76 • **Layer 6 – Bottom Signal Layer (viewed from below)**



11 Appendix: SmartDesign Connections

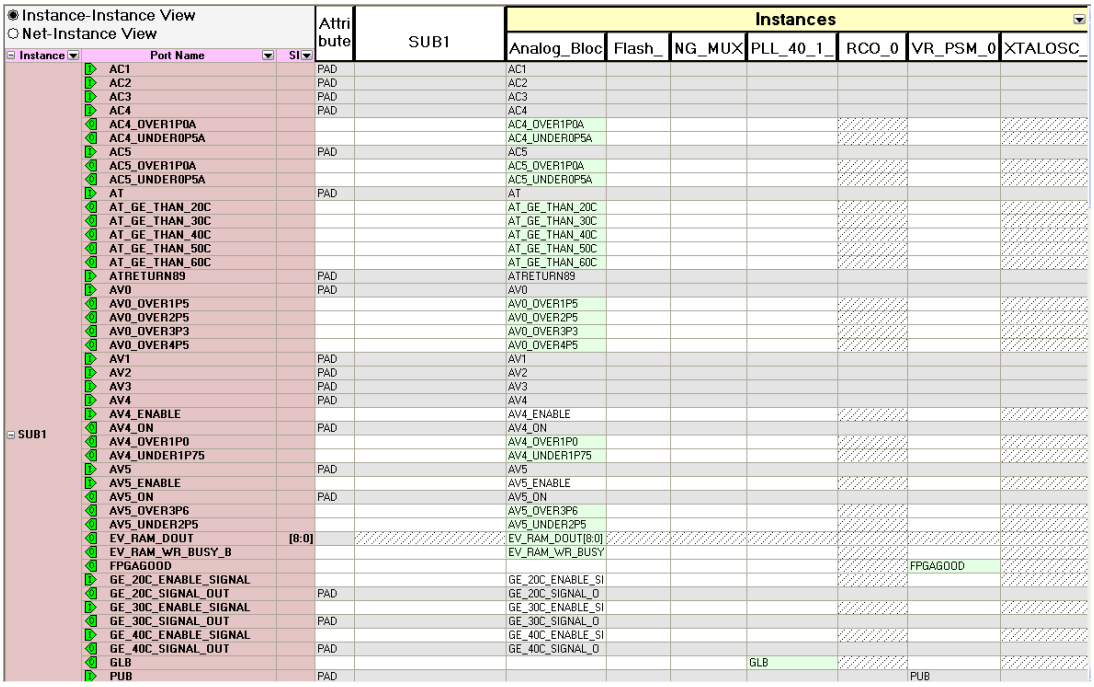
The SmartDesign demonstration requires connections to be made to the SUB1 component and the top-level FSK_Tutorial component.

To promote a port to the top level, right-click the port name and choose **Promote to Top Level**.

Refer to the example files provided in `Fusion_StartKit_UG.zip` to view the completed project files.

11.1 SUB1 Connections

Figure 77 • **SUB1 Connections**



Instance	Port Name	SI	Attribute	SUB1	Instances: Analog_Bloc	Flash_	NG_MUX	PLL_40_1_	RCO_0	VR_PSM_0	XTALOSC_
SUB1	AC1		PAD		AC1						
	AC2		PAD		AC2						
	AC3		PAD		AC3						
	AC4		PAD		AC4						
	AC4_OVER1P0A				AC4_OVER1P0A						
	AC4_UNDER0P5A				AC4_UNDER0P5A						
	AC5		PAD		AC5						
	AC5_OVER1P0A				AC5_OVER1P0A						
	AC5_UNDER0P5A				AC5_UNDER0P5A						
	AT		PAD		AT						
	AT_GE_THAN_20C				AT_GE_THAN_20C						
	AT_GE_THAN_30C				AT_GE_THAN_30C						
	AT_GE_THAN_40C				AT_GE_THAN_40C						
	AT_GE_THAN_50C				AT_GE_THAN_50C						
	AT_GE_THAN_60C				AT_GE_THAN_60C						
	ATRETURN89		PAD		ATRETURN89						
	AV0		PAD		AV0						
	AV0_OVER1P5				AV0_OVER1P5						
	AV0_OVER2P5				AV0_OVER2P5						
	AV0_OVER3P3				AV0_OVER3P3						
	AV0_OVER4P5				AV0_OVER4P5						
	AV1		PAD		AV1						
	AV2		PAD		AV2						
	AV3		PAD		AV3						
	AV4		PAD		AV4						
	AV4_ENABLE				AV4_ENABLE						
	AV4_ON		PAD		AV4_ON						
	AV4_OVER1P0				AV4_OVER1P0						
	AV4_UNDER1P75				AV4_UNDER1P75						
	AV5		PAD		AV5						
	AV5_ENABLE				AV5_ENABLE						
	AV5_ON		PAD		AV5_ON						
	AV5_OVER3P6				AV5_OVER3P6						
	AV5_UNDER2P5				AV5_UNDER2P5						
	EV_RAM_DOUT	[8:0]			EV_RAM_DOUT[8:0]						
	EV_RAM_WR_BUSY_B				EV_RAM_WR_BUSY						
	FPGAGOOD									FPGAGOOD	
	GE_20C_ENABLE_SIGNAL				GE_20C_ENABLE_SI						
	GE_20C_SIGNAL_OUT		PAD		GE_20C_SIGNAL_O						
	GE_30C_ENABLE_SIGNAL				GE_30C_ENABLE_SI						
	GE_30C_SIGNAL_OUT		PAD		GE_30C_SIGNAL_O						
	GE_40C_ENABLE_SIGNAL				GE_40C_ENABLE_SI						
	GE_40C_SIGNAL_OUT		PAD		GE_40C_SIGNAL_O						
	GLB							GLB			
	PUB		PAD							PUB	

Figure 78 • **SUB1 Connections**

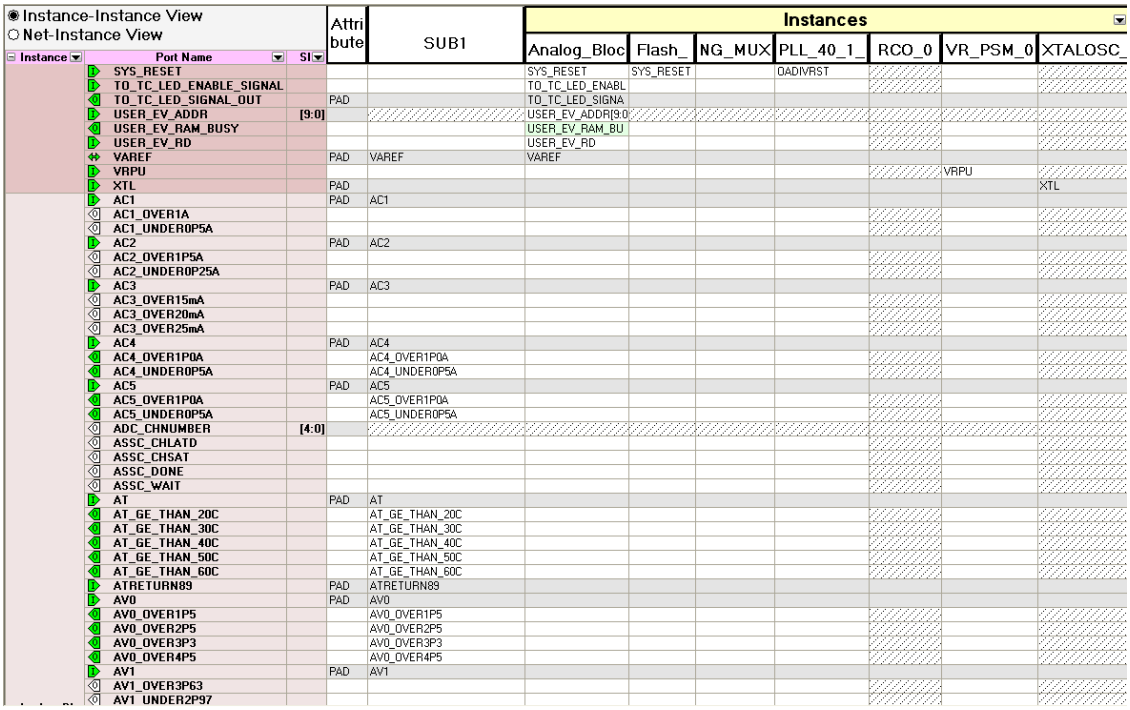
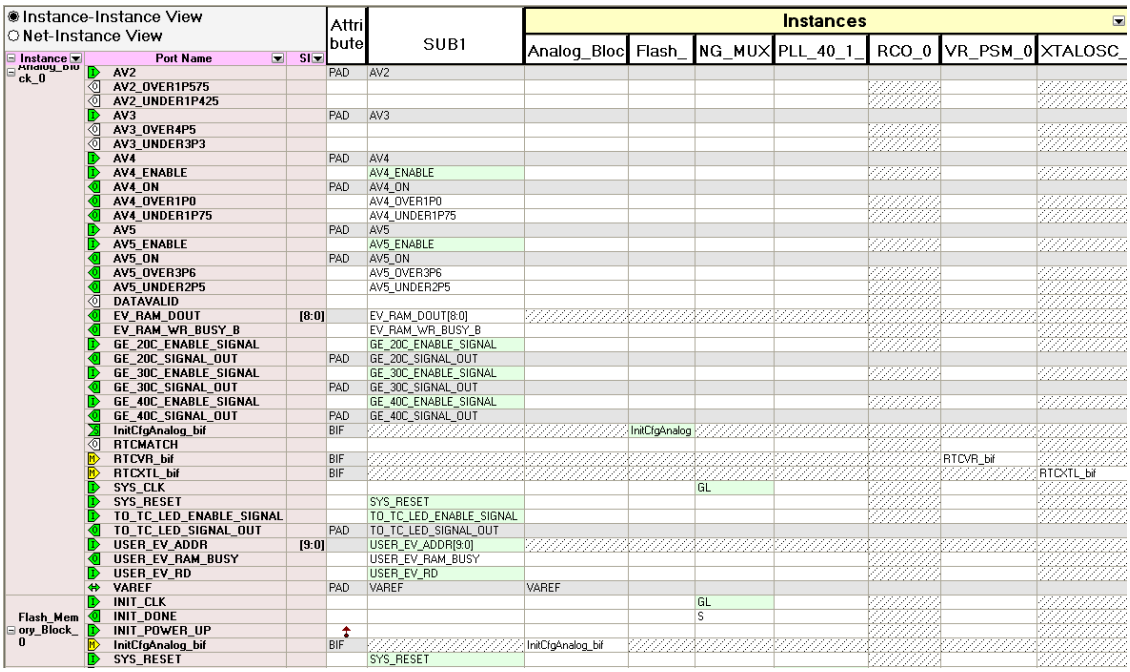
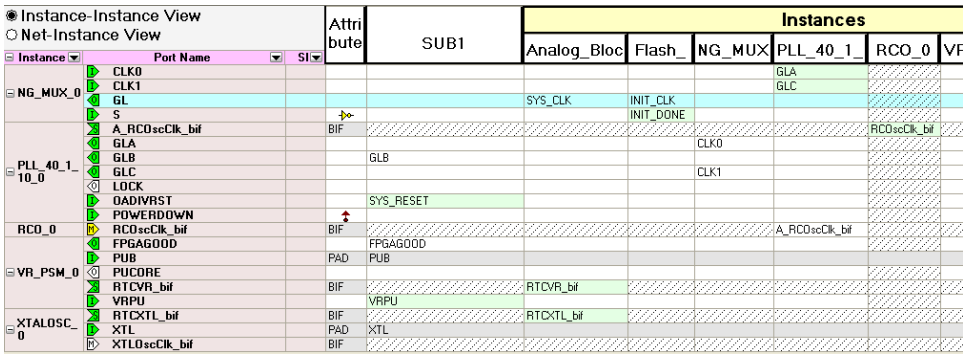


Figure 79 • **SUB1 Connections**



Note: Expose the INIT_DONE pin in the Flash Memory Block by right-clicking **InitCfgAnalog_bif**, choosing **Expose Driver Pins**, and then clicking **OK**.

Figure 80 • **SUB1 Connections**



11.2 FSK_Tutorial Connections

Figure 81 • **FSK_Tutorial Connections**

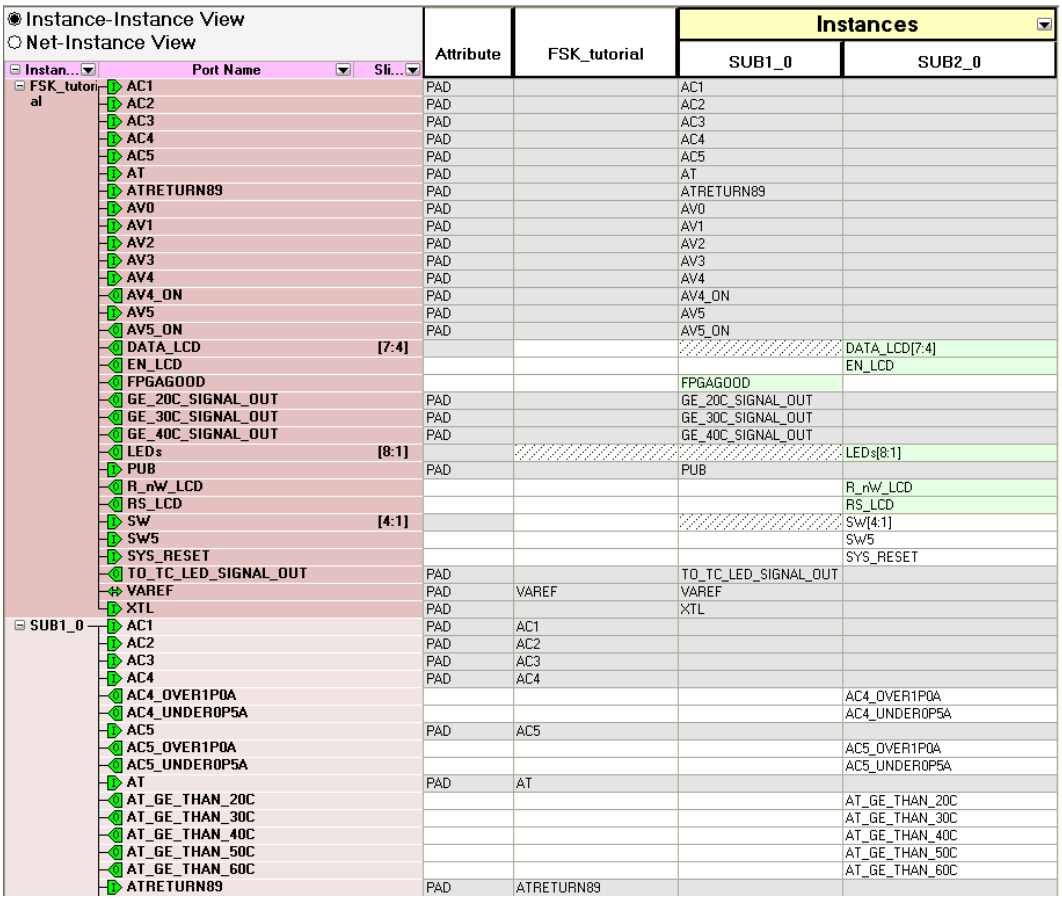


Figure 82 • **FSK_Tutorial Connections**

◉ Instance-Instance View
○ Net-Instance View

Instan...	Port Name	Sli...	Attribute	FSK_tutorial	Instances: SUB1_0	Instances: SUB2_0
	AV0		PAD	AV0		
	AV0_OVER1P5					AV0_OVER1P5
	AV0_OVER2P5					AV0_OVER2P5
	AV0_OVER3P3					AV0_OVER3P3
	AV0_OVER4P5					AV0_OVER4P5
	AV1		PAD	AV1		
	AV2		PAD	AV2		
	AV3		PAD	AV3		
	AV4		PAD	AV4		
	AV4_ENABLE					AV4_ENABLE_OUT
	AV4_ON		PAD	AV4_ON		
	AV4_OVER1P0					AV4_OVER1P0
	AV4_UNDER1P75					AV4_UNDER1P75
	AV5		PAD	AV5		
	AV5_ENABLE					AV5_ENABLE_OUT
	AV5_ON		PAD	AV5_ON		
	AV5_OVER3P6					AV5_OVER3P6
	AV5_UNDER2P5					AV5_UNDER2P5
	EV_RAM_DOUT	[8:0]				EV_RAM_DOUT_bus[8:0]
	EV_RAM_WR_BUSY_B					EV_RAM_WR_BUSY_B_net
	FPGAGOOD			FPGAGOOD		
	GE_20C_ENABLE_SIGNAL					AT_GE_THAN_20C_enb
	GE_20C_SIGNAL_OUT		PAD	GE_20C_SIGNAL_OUT		
	GE_30C_ENABLE_SIGNAL					AT_GE_THAN_30C_enb
	GE_30C_SIGNAL_OUT		PAD	GE_30C_SIGNAL_OUT		
	GE_40C_ENABLE_SIGNAL					AT_GE_THAN_40C_enb
	GE_40C_SIGNAL_OUT		PAD	GE_40C_SIGNAL_OUT		
	GLB					CNT_CLK_int
	PUB		PAD	PUB		
	SYS_RESET					SYS_RESET_gl_out
	TO_TC_LED_ENABLE_SIGNAL					TO_TC_LED_ENABLE_SIGNAL
	TO_TC_LED_SIGNAL_OUT		PAD	TO_TC_LED_SIGNAL_OUT		
	USER_EV_ADDR	[9:0]				USER_EV_ADDR[9:0]
	USER_EV_RAM_BUSY					USER_EV_RAM_BUSY_net
	USER_EV_RD					USER_EV_RD_net
	VAREF		PAD	VAREF	VAREF	
	VRPU					VRPU
	XTL		PAD	XTL		
SUB2_0	AC4_OVER1P0A				AC4_OVER1P0A	
	AC4_UNDER0P5A				AC4_UNDER0P5A	
	AC5_OVER1P0A				AC5_OVER1P0A	
	AC5_UNDER0P5A				AC5_UNDER0P5A	
	AT_GE_THAN_20C				AT_GE_THAN_20C	
	AT_GE_THAN_20C_enb				GE_20C_ENABLE_SIGNAL	
	AT_GE_THAN_30C				AT_GE_THAN_30C	
	AT_GE_THAN_30C_enb				GE_30C_ENABLE_SIGNAL	
	AT_GE_THAN_40C				AT_GE_THAN_40C	

Figure 83 • **FSK_Tutorial Connections**