CoreConsole v1.4 User's Guide

Actel®

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Welcome

CoreConsole is a system-level development tool and IP deployment platform that simplifies the task of assembling and connecting IP for implementation in Actel FPGAs. It enables you to select IP components from a database supplied by Actel and third-party IP vendors, and graphically stitch them together to build a processor-based system-level integration (SLI) design.

When the design is complete, the RTL and other files needed to implement it can be easily generated and written to disk, where they are available for import into the Actel Libero® Integrated Design Environment (IDE). CoreConsole also generates a testbench for the SLI design that you can build to assist in verification. The current release has a practical set of IP components for building CoreMP7 Advanced Microcontroller Bus Architecture (AMBA) based designs. Future releases will support a larger portfolio of IP components and a wide range of generators for different software tools and operating systems, as well as unit testbenches.

What's New in CoreConsole

The following are highlights of new features for CoreConsole. See the CoreConsole release notes for a complete list.

Web-based update of IP cores – CoreConsole v1.4 adds the capability to automatically check for updates to existing IP cores or download new available IP cores. The update option - automatic, standard, or manual- can be set from the Updates tab of the System Options dialog box. When the cores have been downloaded, CoreConsole will prompt you to install them.

Getting Help

Online Help

CoreConsole comes with online help.

User's Guides

All Actel software products include online help and online manuals in PDF format. The PDF manuals are available from the **Start** menu, the CD-ROM, and the Actel website.

Technical Support

Contact Actel Technical Support by phone or e-mail. Search our online database for tips, tricks, and workarounds.

Software Updates

Software updates are available on Actel's website: http://www.actel.com/download/.

Documentation Feedback

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products. We welcome your feedback. Please send your comments to documentation@actel.com.

CoreConsole Online Help

This online help system is designed to open in the HTML Help Viewer – Microsoft's Help window for viewing compiled HTML help. If you do not have the HTML Help Viewer component installed on your system, you can view it with Microsoft's Internet Explorer browser (use version 4.x or later for complete functionality).

This help system is best viewed with the Window's Verdana font. Verdana is included with Internet Explorer 4.x or later. You can also download this free font from Microsoft's Web site.

See Also

Using navigation tabs

Using Navigation Tabs

CoreConsole's online help, which is generated using Microsoft HTML Help, includes the following navigation tabs:

Contents

The Contents tab displays books and pages that represent the categories of information in the online help system. When you click a closed book, it opens to display its content (sub-books and pages). When you click an open book, it closes. When you click pages, you select topics to view in the right-hand pane of the HTML Help viewer.

Search

The Search tab enables you to search for words in the Help system and locate topics containing those words. Full-text searching looks through every word in the online help to find matches. When the search is completed, a list of topics is displayed so you can select a specific topic to view.

CoreConsole Licensing

CoreConsole within Libero Integrated Design Environment (IDE)

The Libero IDE license includes a license for CoreConsole v1.3 and above. For a list of IP cores included in your license, refer to the CoreConsole IP cores page on the Actel web site, at http://www.actel.com/products/software/coreconsole/ipcores.aspx.

You must install Libero IDE and CoreConsole prior to installing your license. For more information about installing Libero IDE and obtaining a license, refer to the Actel Libero® IDE / Designer Installation and Licensing Guide available at http://www.actel.com/documents/install_ug.pdf.

Standalone CoreConsole

CoreConsole requires a new CoreConsole node-locked license and a SysBASIC Subsystem IP license. A new license can be obtained for free from the Actel Customer Portal: http://www.actel.com/portal. Register for a license and receive a 1 year license file.

Note: Licenses for previous versions of CoreConsole will continue to work. FLEXlm Licensing will not work when running CoreConsole remotely over Windows XP Remote Desktop or Terminal Services. If any change is made to the license file, even if it is unrelated to CoreConsole, it will automatically detect this and update its database. This is a correct behavior and is not harmful.

To obtain a CoreConsole license:

1. From the Customer Portal welcome page (http://www.actel.com/portal), click **License and Registration**.
2. Click the **Request Free License** button.
3. Click **Core Console CoreMP7 Full Bundle 1YR Node Locked License**.
4. Read the Licensing Agreement page and click the **Agree** button.

5. Enter your PCs hard disk ID, select your operating system, and click the **Submit** button. Your 1 year CoreConsole license file will be emailed to you.

To install the CoreConsole license:

1. Locate, or create if necessary, a folder named *flexlm* under your C drive.

Note: If you are using Libero IDE v7.3, rename the license file you just received, *license.dat, to cclicense.dat.* CoreConsole is used with Libero IDE software and you should already have a Libero IDE *license.dat*file in your *flexlm* folder. Be sure to rename your CoreConsole license to *cclicense.dat* to avoid overwriting your Libero IDE license.

2. Save your license filein the *flexlm* folder.
3. From the **Start** menu, choose **Settings > Control Panel**.
4. With the Control Panel Window in focus, double-click the **System** icon.
5. In the **Systems Properties** dialog, click the **Advanced** tab.
6. Click the **Environment Variables** button.
7. If you already have an existing *license.dat* file: in the **Variable Name** field type: *LM_LICENSE_FILE* and click **Edit**. Edit the **Variable Name** field to read: *c:\flexlm\license.dat*; *c:\flexlm\cclicense.dat.*If you do not have an existing *license.dat* file: in the **Variable Name** field type: *LM_LICENSE_FILE* and click **New**. and enter the **Variable Name** field to read: *c:\flexlm\license.dat*.
8. Click **OK**.
9. The **Environment Variables** dialog is in view. Click **OK** to close.

See Also

Obtaining an IP license

Installing an IP license

IP Cores

Obtaining and Installing IP

IP cores in CoreConsole can be updated through the Updates tab in the System Options dialog box, through IP database updates, or through Coreconsole component zip (CCZ) files.

Updates Tab in the System Options Dialog Box

IP core updates are available from the Actel IP core web server. The **Updates** tab in the **System Options** dialog box enables you to select the update method of your choice.

To change the update options:

1. From the **Options** menu, choose **System Options**
2. Click the Updates tab
3. Select your update method: Automatical, standard, or manual
4. Click **OK**

IP Database Update

IP database updates are available periodically from the CoreConsole download page: http://www.actel.com/download/software/coreconsole/

To obtain the latest IP database:

1. Go to http://www.actel.com/download/software/coreconsole/
2. Click **Actel CoreConsole IP Database Update**

3. Save the executable file on your PC

To install the IP database:

1. Double-click the executable file, this will open the Actel CoreConsole IP Database Update Wizard. Click **Next**.
2. Read the license agreement and check the **I accept the agreement** box. Click **Next** to continue.
3. The Information dialog box displays the IP component packages that will be added to your CoreConsole IP database. Click **Next** to continue.
4. Select the folder for the IP database and click **Next**.
5. Click **Install**. When the installation is completed, a dialog box informs you that you may need to obtain licenses for the installed components.
6. Click **Next**. A dialog box enables you to go to the Actel License and Registration page, press **Yes** to obtain a license or **No** to do this at a later time.
7. The Actel CoreConsole IP database has been successfully installed. Click **Finish** to launch CoreConsole. The database update will be imported when you restart CoreConsole

CoreConsole Component Zip (CCZ) File

CoreConsole component zip (CCZ) files are available from your Actel or distribution partner sales office.

To download and install a CCZ file:

1. Obtain the CCZ file from your Actel or distribution partner sales office
2. Save the CCZ file on your PC
3. From the **Actions** menu, select **Add to Database**. This opens the Add Actel Supplied IP to the Database dialog box (Figure 1).

Figure 1 · Add Actel Supplied IP to the Database Dialog Box

4. Click **OK**. This opens the Locate CoreConsole Component Zip File dialog box
5. Select the CCZ file you downloaded and click **OK**. This will install all downloaded components
6. From the **Actions** menu, select **Rebuild Database** to rebuild the database of available IP components. Click **OK** in the dialog box to start rebuilding the CoreConsole IP database

See Also

Obtaining an IP license

Installing an IP license

System options

IP Updates dialog box

Obtaining an IP license

License files for CoreConsole and the CoreMP7 + SysBASIC core bundles are available for free from the Actel web site, at http://www.actel.com/portal/. Register for a license and receive a 1 year license file.

To obtain a CoreConsole and CoreMP7 + SysBASIC core bundle license:

1. On the Customer Portal welcome page (http://www.actel.com/portal), click **License and Registration**.
2. Click the **Request Free License** button.
3. Click **Core Console CoreMP7 Full Bundle 1YR Node Locked License**.
4. Read the **Licensing Agreement** and click **the Agree** button.
5. Enter your PC hard disk ID, select your operating system, and click the **Submit** button. Your 1 year CoreConsole license file will be emailed to you.

Licenses for DirectCores delivered through CoreConsole are available from your Actel or distribution partner sales office.

Note: Most DirectCores are licensed for free evaluation (Eval) use through CoreConsole, once you have the CoreConsole + CoreMP7 + SysBASIC bundle license. The Eval license allows you to instantiate, configure and generate the DirectCore in CoreConsole and permits simulation but not synthesis in Libero.

To license DirectCores delivered through CoreConsole:

Order directly from your Actel or distribution partner sales office and complete the license agreement in hard copy. When the order completes you will receive a software ID via email. Register on the Customer Portal http://www.actel.com/portal/:

1. On the Customer Portal welcome page (http://www.actel.com/portal/), click **License and Registration**
2. Enter your new software ID and click the **Register Purchased Product** button
3. Enter your PC hard disk ID, select your operating system, and click the **Submit** button. Your license file will be emailed to you.

See Also

Installing an IP license

CoreConsole Licensing

Installing an IP license

If you have previously installed a CoreConsole license file as *cclicense.dat*, you may append the content of the IP license file you just received to *cclicense.dat* and save it. The next time you run CoreConsole, the relevant IP cores will be licensed.

To install an IP license:

1. Locate, or create if necessary, a folder named *flexlm* under your C drive.
2. Rename the *license.dat* file you just received as *cclicense.dat*.
3. Save *cclicense.dat* in the *flexlm* folder.
   CoreConsole is used with Libero IDE software and you should already have a Libero IDE *license.dat* file in your flexlm folder. Be sure to rename your CoreConsole license to *cclicense.dat* to avoid overwriting your Libero IDE license.
4. From the **Start** menu, choose **Settings** > **Control Panel**.
5. With the Control Panel window in focus, double-click the icon labeled **System**.
6. In the Systems Properties dialog, click the **Advanced** tab.
7. Click the **Environment Variables** button.
8. In the **Variable Name** field type: LM_LICENSE_FILE and click **Edit**.
9. Edit the **Variable Name** field to read: *c:\flexlm\license.dat; c:\flexlm\cclicense.dat*, and click **OK**.

10. The Environment Variables dialog is in view. Click **OK** to close.

See Also

CoreConsole Licensing

Adding User IP

The current release of CoreConsole does not support the addition of user IP. In future releases, it will be possible to integrate user IP components into CoreConsole, and use them in exactly the same way as the supplied IP. In addition, there will be a tool provided to assist in the correct packaging to automate the process. The two key tasks necessary in adding user IP is ensuring that it has a correct bus interface and a full SPIRIT IP-XACT definition.

See Also

Obtaining and installing IP

SPIRIT

SPIRIT (Structure for Packaging, Integrating, and Re-using IP within Tool-flows) is an industry standard with the goal of supporting automated IP re-use. CoreConsole uses a component's SPIRIT IP-XACT description to automatically integrate it into the design and to generate a project system testbench to verify the integrity of the design.

Design Flow

Design Flow Overview

CoreConsole can be used as a standalone tool in a loosely integrated design flow with the Libero IDE Project Manager, or it can be launched directly from the Libero IDE Project Manager in a tightly integrated design flow.

Standalone CoreConsole

You can use CoreConsole to generate a sub-system design for integration in a top-level system design. CoreConsole does not generate the top-level system, and it does not map to pins on the FPGA. Once the CoreConsole design has been imported into Libero IDE project, you must integrate it into your final system-level design (including mapping I/Os). Figure 2 shows the standalone CoreConsole design flow.

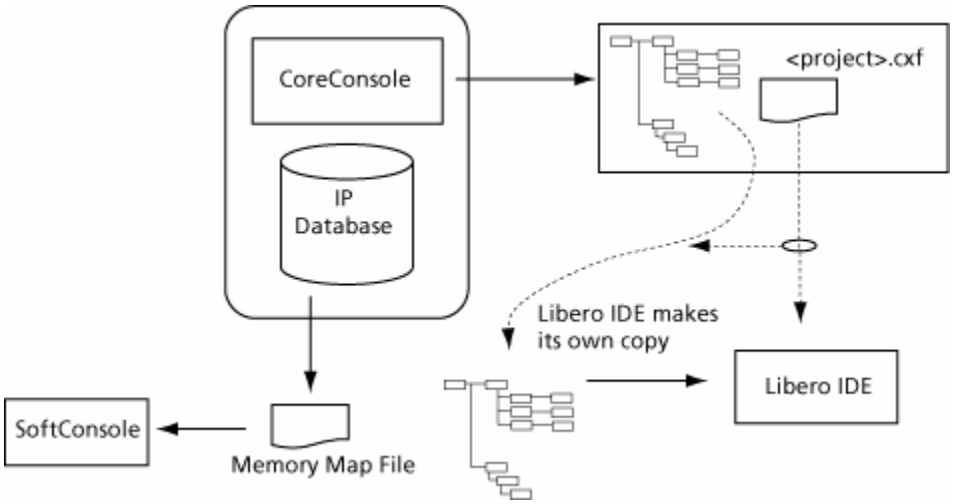


Figure 2 · Standalone CoreConsole Flow

Import to Libero IDE

Importing the CoreConsole design to the Libero IDE project is a simple process. The files generated by CoreConsole and their locations on your hard drive are described in a set of XML files (CXF) that contain the information needed by Libero IDE to locate them and import them into the correct simulation and design directories within the Libero IDE.

From the Libero IDE **File** menu, choose **Import Files**, and select **Files of type: Components (.cxf)** to import a CoreConsole generated design. You must take the sub-system design generated by CoreConsole and instantiate it in your top-level design. In addition to the RTL for the design, Libero IDE generates a BFM (CoreMP7 Bus Functional Model) and script that enable you to test the CoreConsole project system. This is described in detail in the CoreMP7 User's Guide.

Output files describes the files generated by CoreConsole, and how they are organized to enable Libero IDE to import them.

Note: Libero IDE does not audit the standalone CoreConsole output. If a new standalone CoreConsole iteration is performed, the CoreConsole project must be re-imported into Libero IDE.

Note: You can still import pre-CoreConsole v1.3 projects (.ccp) in Libero Project Manager by selecting Files of type: CoreConsole 1.0 to 1.2 Projects (.ccp). However, Actel recommends that you open the pre-CoreConsole v1.3 project in standalone CoreConsole v1.3, re-generate the design, then import the design (by selecting Files of type: Component (.cxf)) in Libero Project Manager.

SoftConsole Files

SoftConsole files are also generated by CoreConsole.

See Also

Output files

Integration with Libero IDE tool flow

Integration with Software Developers Console IDE (SoftConsole) tool flow

Libero IDE Integration

CoreConsole can now be launched directly from the Libero IDE Project Manager and can create CoreConsole design components or individual IP core components directly within the Libero project. Libero passes the project information to CoreConsole, where the IP component is created. CoreConsole then passes the RTL source files back into your Libero IDE project, where they are shown as Components in the Hierarchy and Files window.

Refer to the Libero User's Guide for further details on the use of CoreConsole, directly from the Libero IDE Project Manager, to create CoreConsole components and IP Core components in a Libero IDE project.

SoftConsole Integration

There is automatic support for CoreConsole integration with the SoftConsole IDE. This includes export of a memory map file and any driver files that are available for peripheral cores used in a CoreConsole project design. Driver files are not available for all peripheral cores.

Integration with Other Tools

CoreConsole outputs RTL, and it has been verified that this RTL works with ModelSim®, Synplify®, Designer®, and other tools incorporated into the Libero IDE. As a result, it is possible to use a point tool flow instead of the Libero IDE. CoreConsole does not automatically generate any scripts to automate this process.

User Interface

User Interface Overview

CoreConsole's user interface (Figure 3) is organized in a **Components** tab, a **Generate** tab and a **Schematic** window.

The Components tab lists all of the IP components you can incorporate into your design.

The Generate tab is where you create the CoreConsole output that can you can import into the Libero IDE.

The Schematic window displays the graphical representation of the project, and enables you to add or delete connections and configure cores.

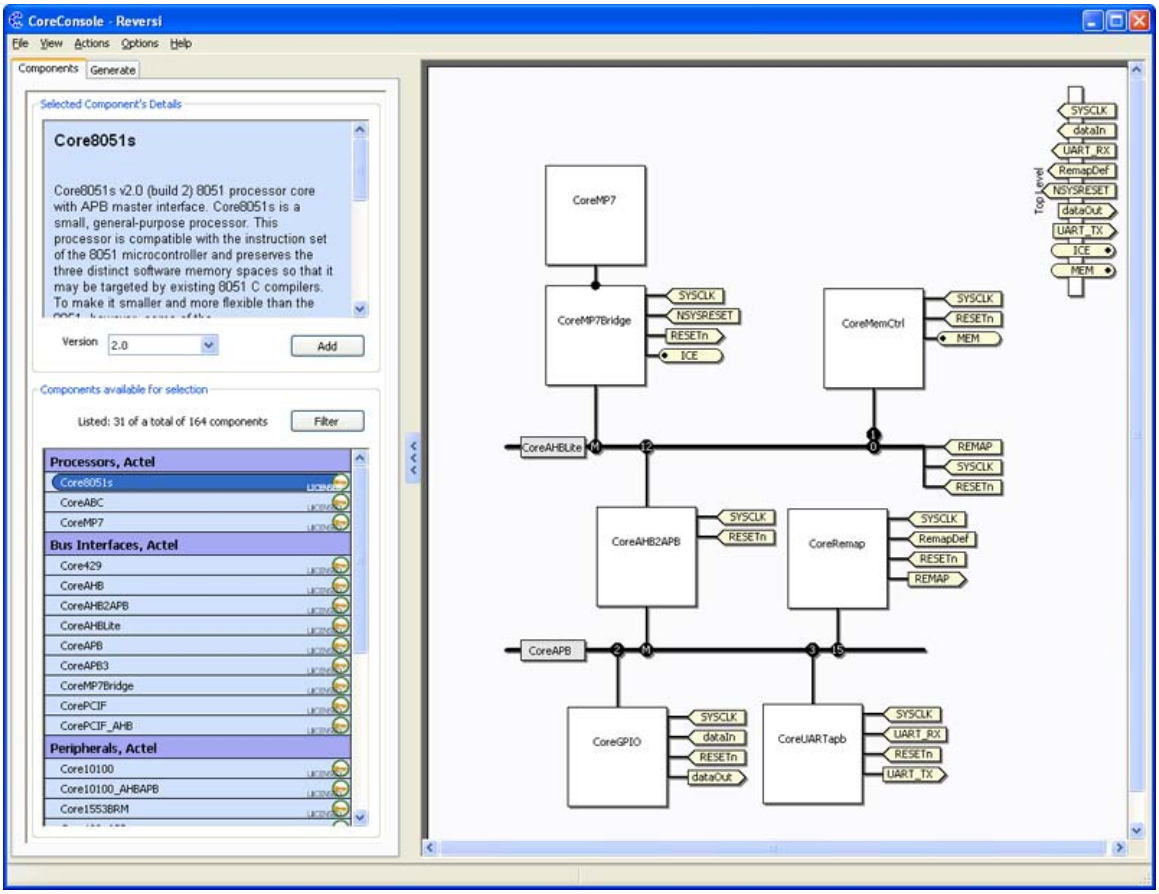


Figure 3 · CoreConsole User Interface

See Also

Components tab

Generate tab

Schematic window

Components Tab

The Components tab (Figure 4) lists all the IP components available in the CoreConsole database. You can use this tab to configure the component display filter and select a component and add it to a design.

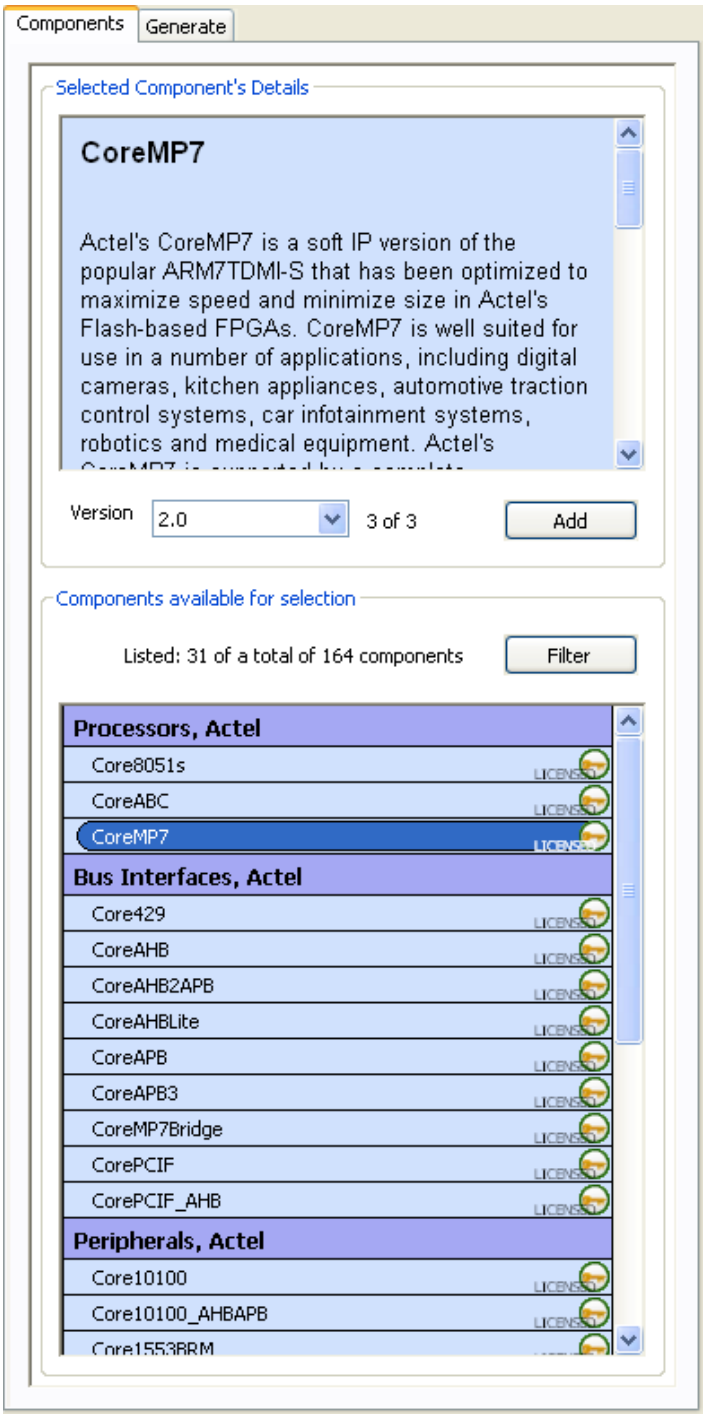


Figure 4 · Components Tab

The Components tab lists Selected Component Details, the Version, and Components available for selection.

Selected Component Details displays a description of the selected component, the components functional category, the provider, and the version number.

Components can be added in any order. Bus fabric components are included in the list of available components and can be added to the design just like any other components, although they display as buses rather than as block components.

The **Components available for selection** displays available components and license status for each component. Use the System Options dialog box (from the Options menu, choose System Options) to display the license status of your core as an icon, as text, or both.

If there are multiple versions of a component available in the IP database, the latest (or highest) version will be the default selection and will be shown in the box. If a previous version of a component is available and you want to use it, you can select it from the **Version** pull-down.

You can activate **Show Linked Connections** to highlight where each connection in your design goes. The only fixed element in the Schematic window is the **Top Level**, which displays the connections to the rest of the design outside of the CoreConsole project (Figure 5).

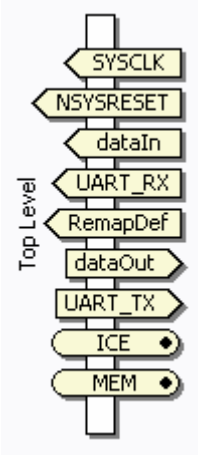


Figure 5 · Top Level

Component Filter

CoreConsole can be used with an unlimited number of IP components. CoreConsole has a component filter and search capability that enables you to find a specific component. Click the **Filter** button on the **Components** tab to open the Filter dialog.

On the dialog, you can choose to list components with or without the version information and you can sort them by name or function. There is a search capability that enables you to search on the component name, manufacturer, market segment, function, interface, and availability on your computer.

See Also

Generate tab

Schematic window

Generate Tab

The Generate tab (Figure 6) is used to set final system configuration options (HDL language and license options) and to generate the design for export to Libero IDE.

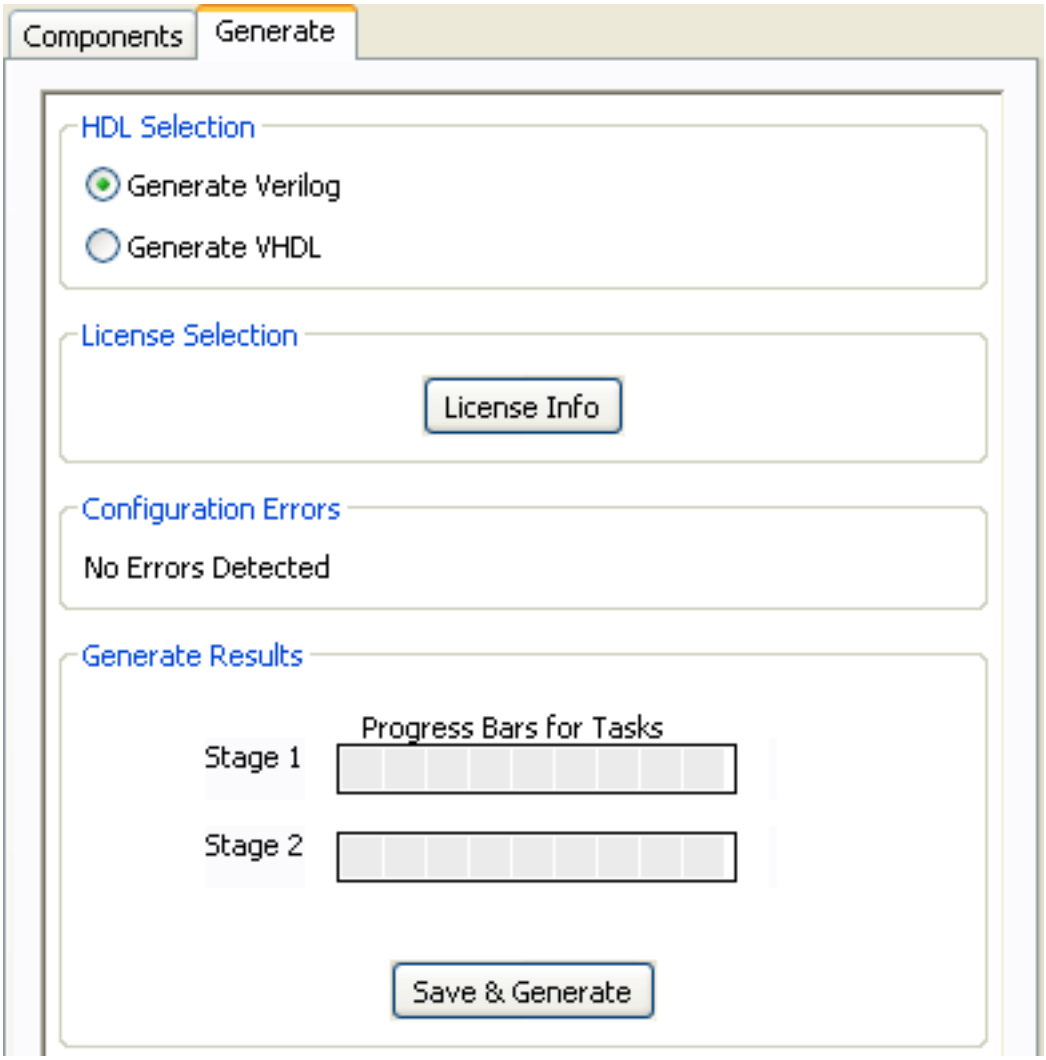


Figure 6 · Generate Tab

The Generate tab has three sections: HDL Selection, License Selection, and Generate Results.

HDL Selection

CoreConsole supports both Verilog and VHDL RTL generation. Selecting one or the other will cause your system project design to be generated and saved to disk on your computer in that format.

License Selection

Clicking the **License Info** button opens the License info dialog box that lists all of the components and buses in your design and their license status. RTL output is generated only for components and buses for which you have an appropriate license.

Configuration Errors

This section displays configuration errors in your design.

Generate Results

Click the **Save & Generate** button to generate all items in your project design and save it to your specified directory. This saves the project to the Console designs directory specified at installation. Then it generates the exported set of output files for Libero, the memory map (in HTML format) and SoftConsole support files.

See Also

Components tab

Schematic window

Generating a design

Schematic Window

A design project is represented graphically as a conventional bus-centric processor system in the Schematicwindow.

Components are added from the Components tab, but once they have been added to the diagram, all other design activities can be carried out directly in the Schematic window. Components are represented as boxes.

Float the mouse over a component and select an item from the tool bar, or right-click and select an item from the shortcut menu to modify a component.

Double-click a component to open the Configuration dialog box. You can move all components (including buses) around the screen.

The schematic window (Figure 7) is controlled by the System Options dialog box.

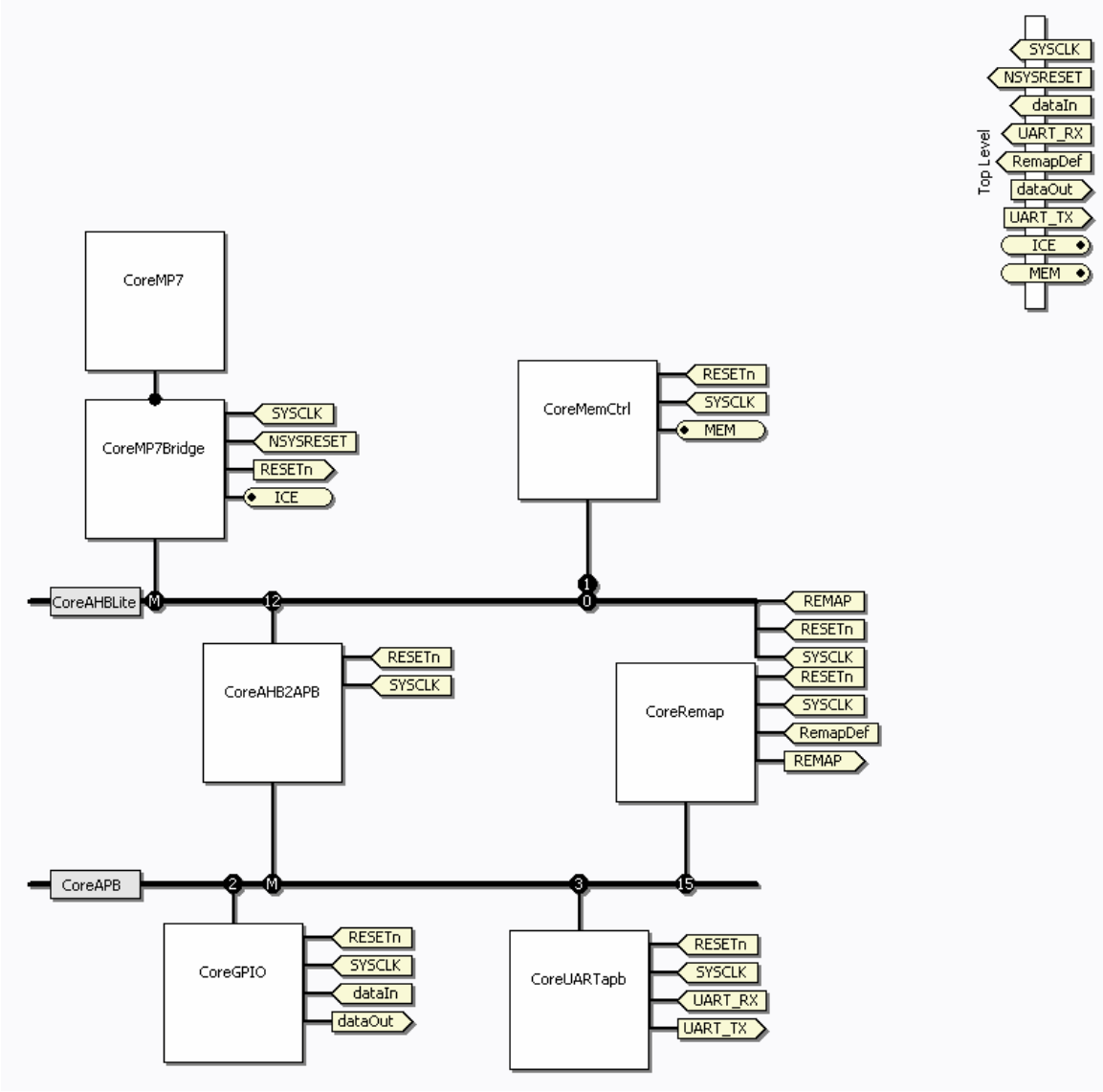


Figure 7 · Schematic Window

The **Top-Level** toolbar (Figure 8) displays the connections to the rest of the design outside of the CoreConsole project.

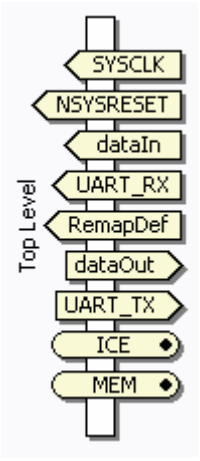


Figure 8 · Top-Level Toolbar

See Also

Components tab

Generate tab

Connections

Connections are central to the operation of CoreConsole. The various types of connections define the nets that bind the components together. The main connections are the bus interfaces.

Bus Interface Connections

The bus interface connections are represented as solid vertical lines between a component and the bus (Figure 9).

Figure 9 · Bus Representation

Each component connection to a bus displays either an M for a bus master or a number (0-15) for a bus slave. This is shown in Figure 9 and the Standard AMBA bus dialog box connections in Figure 10.

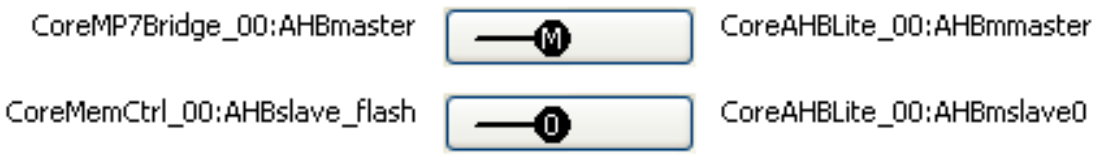


Figure 10 · Bus Representation in Dialog Boxes

Non-Fabric Bus Connections

Bus connections can be made that do not attach directly to the AMBA fabric. This occurs when there are other groups of wires that are described as buses (e.g., the SRAM interface to the memory controller), or when the AMBA interfaces are exported to the external system outside the CoreConsole project. In these cases the buses are represented by the symbol shown in Figure 11:

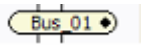


Figure 11 · Bus Connection Icon

These bus interfaces can include connection of both input and output types. There are no bidirectional signals in CoreConsole, but buses can encapsulate both input and output signals.

Ad-Hoc Connections

Apart from the AMBA fabric connections, most of the connections shown on the diagram and in the connection dialog are Ad Hoc connections. These are equivalent to wires connecting pins on a component. They are unidirectional, point to point connections. They are represented by the symbol shownin Figure 12:

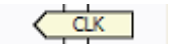


Figure 12 ·Ad-Hoc Connection Icon

The direction (i.e., whether it is Input or Output) is indicated by the orientation of the arrow on the signal.

System-Level Design

CoreConsole enables you to build a system-level design by automating the design process and connecting the sub-system and IP components that surround a processor core. CoreConsole is a bus-centric tool. CoreConsole currently supports the AMBA bus interfaces to connect the IP within a design. Building the system around the bus fabric enables the extension of the system outside of CoreConsole.

You can export the AMBA Advanced High-Performance Bus (AHB) or Advanced Peripheral Bus (APB) interfaces to the CoreConsole top-level and then connect them to AMBA compliant IP outside of CoreConsole (Figure 13):

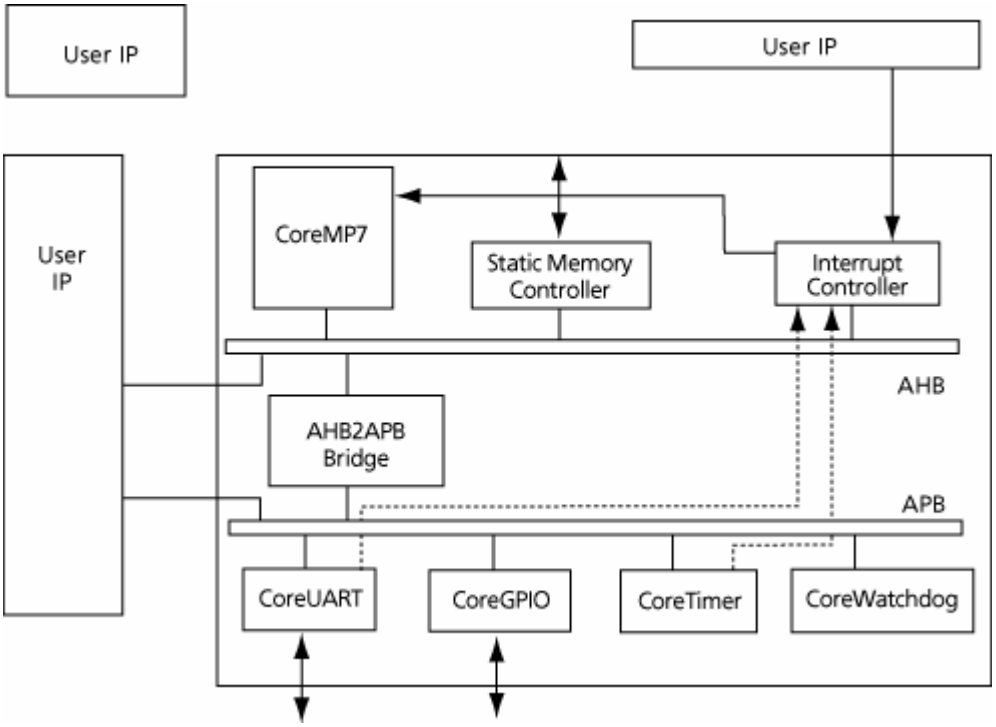


Figure 13 · Example CoreMP7 System

A typical system consists of the project system generated by CoreConsole, user IP components, and the top-level instantiation of the project system that connects it to any top-level IP and wires it to the I/O pads.

Bus-Centric Design

The current release of CoreConsole uses AMBA buses. Future versions of CoreConsole may support other bus protocols in addition to AMBA. The principal requirement of the bus-centric approach is that all of the IP components must have the correct bus interface to be integrated by CoreConsole into a design.

The current release supports AMBA AHB and APB. Most of the components in the database have AHB or APB interfaces. The CoreMP7 processor has an AHB master interface, so it must be one of the three masters on the AHB bus.

System Options

The **System Options** dialog box (Figure 14) controls the display on the schematic window through the **General** tab and the IP cores updates through the **Updates** tab.

To open the system options dialog box, from the Options menu, choose **System Options**.

General Tab

The General tab controls the display on the schematic window.

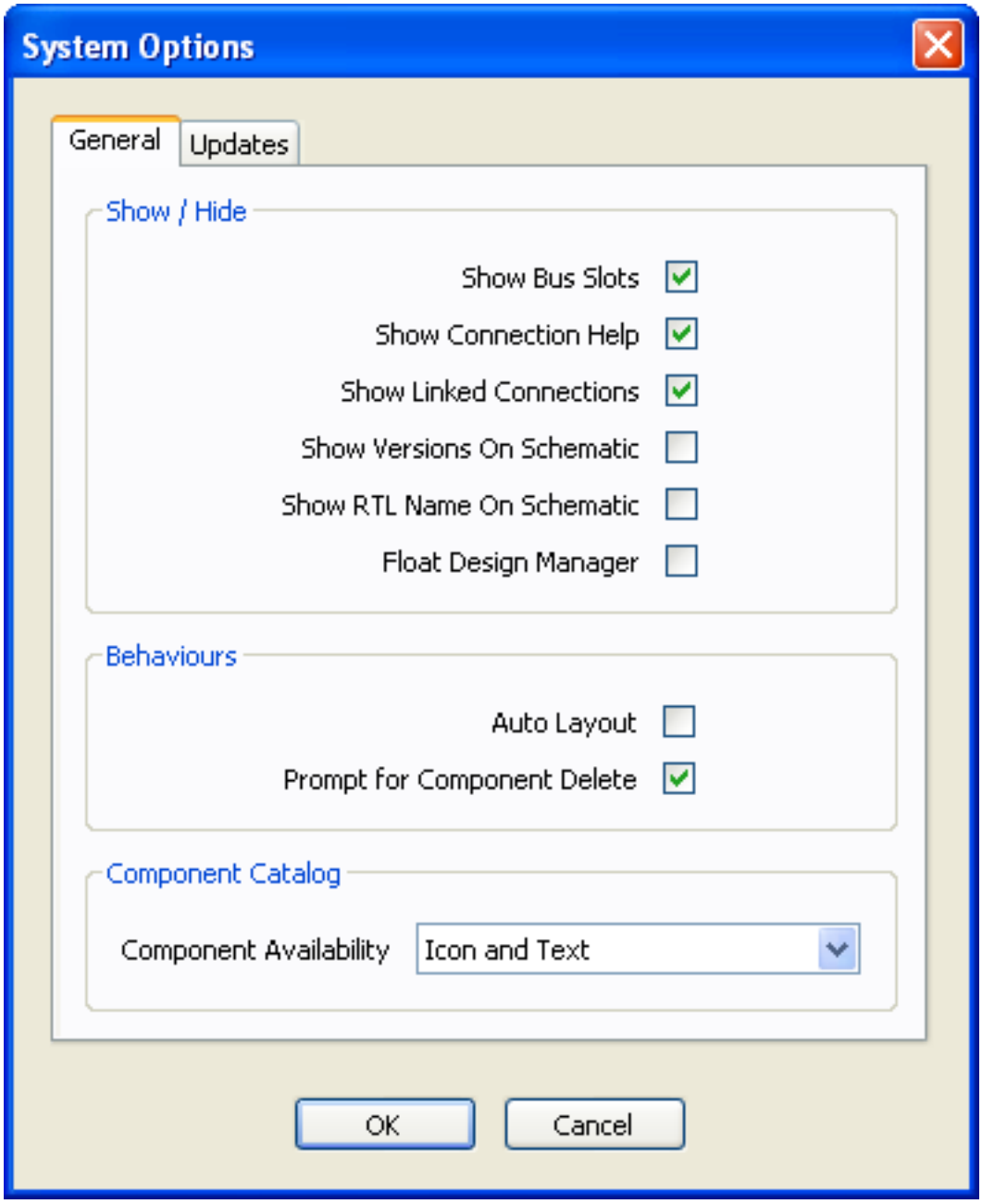


Figure 14 · System Options Dialog Box - General Tab

The following options are available:

Show Bus Slots

Choose this option to display the slot number on the bus to which each component is attached. The slot number indicates the component's location in the project system memory map. If it is not selected, the slot number is replaced by a connection point only.

Show Connection Help

This option enables the help window for each component. See Components help for more information.

Show Linked Connections

Select this option to float over a connection in the schematic and highlight all the other points connected to the net.

Show Versions on Schematic

Select this option to display the version number of each block under the component name of the block.

Show RTL Name on the Schematic

Select this option to display the RTL name of each block in your design under the component name.

Float Design Manager

Select this option to unlock the Design Manager (Components and Generate) tabs and move them around the screen; this enables you to create more screen area for the schematic window.

Auto Layout

Select this option to automatically place the components drawn in the schematic window.

Prompt for Component Delete

Select this option to enable or disable the confirm delete dialog box.

Component Availability

Set this option to display a components license status as icon and text, icon only, text only, or don't show.

Updates Tab

The **Updates** tab enables you to choose from several IP core update methods (Figure 15).

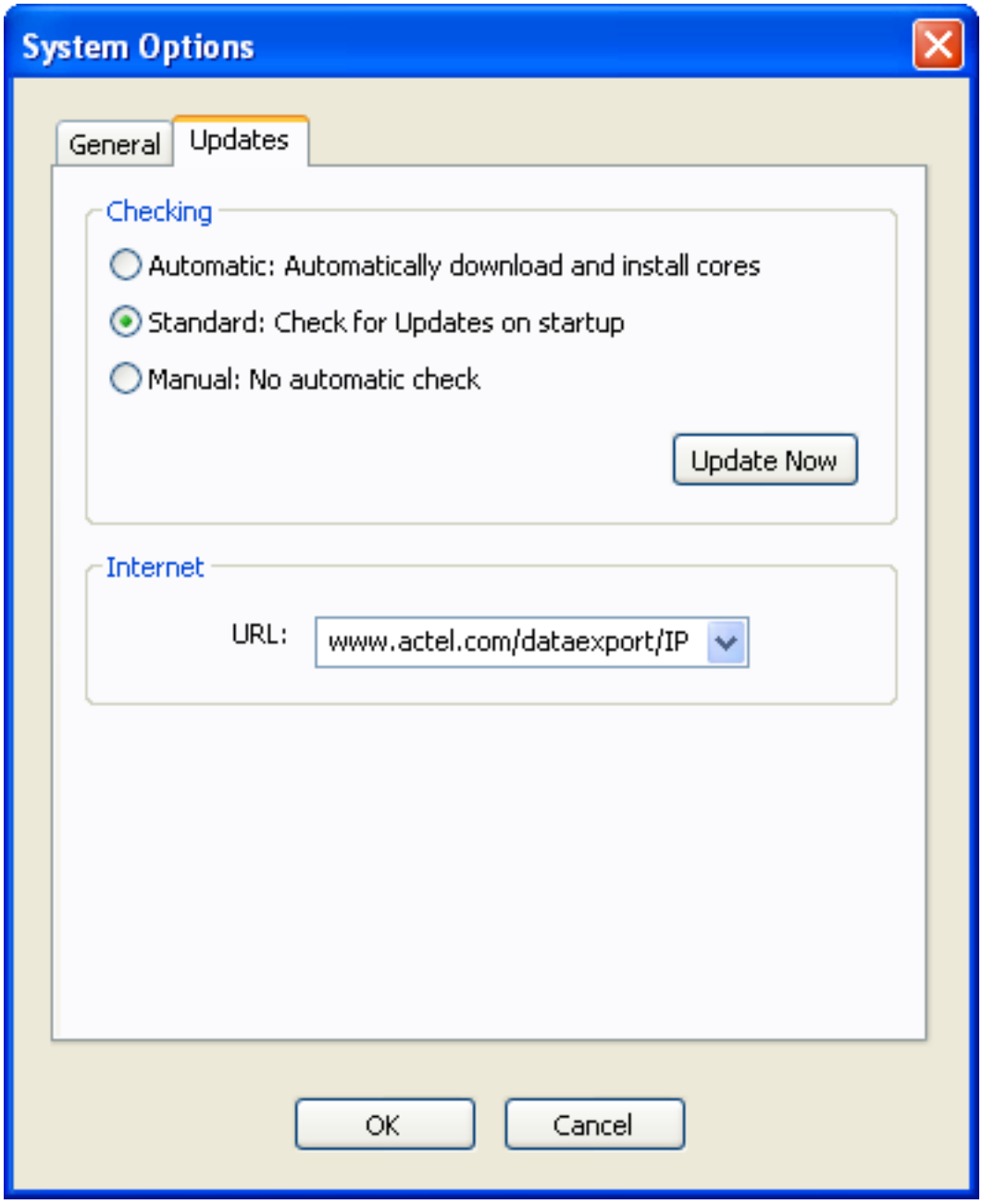


Figure 15 · System Options Dialog Box - Updates Tab

Automatic: Automatically download and install cores

CoreConsole will obtain the most recent versions of any cores on the update server that are not already in your database. When the cores have been downloaded, CoreConsole will prompt you to install them (Figure 16).

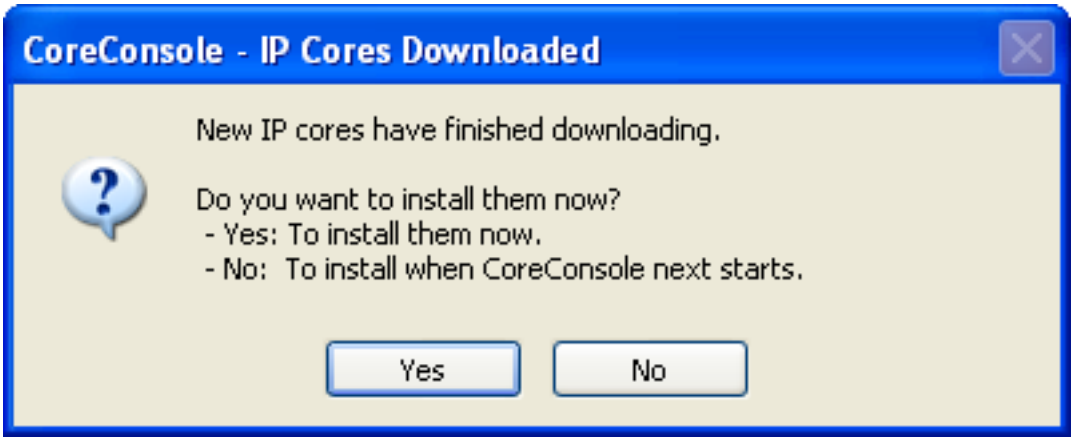


Figure 16 · IP Download Complete Dialog Box

Click **Yes** to install the cores, and they will appear on the **Components** tab. If you click **No**, the next time you start CoreConsole, the Add Downloaded IP to Database dialog box will appear. The message will continue to show each time you restart CoreConsole until you accept installing the downloaded cores.

Standard: Check for updates on startup

CoreConsole will automatically obtain a list of the most recent versions of any cores on the update server on startup. This is the default option. If the list contains any new cores that are not in your database and that you have not previously declined, the New IP dialog box appears (Figure 17).

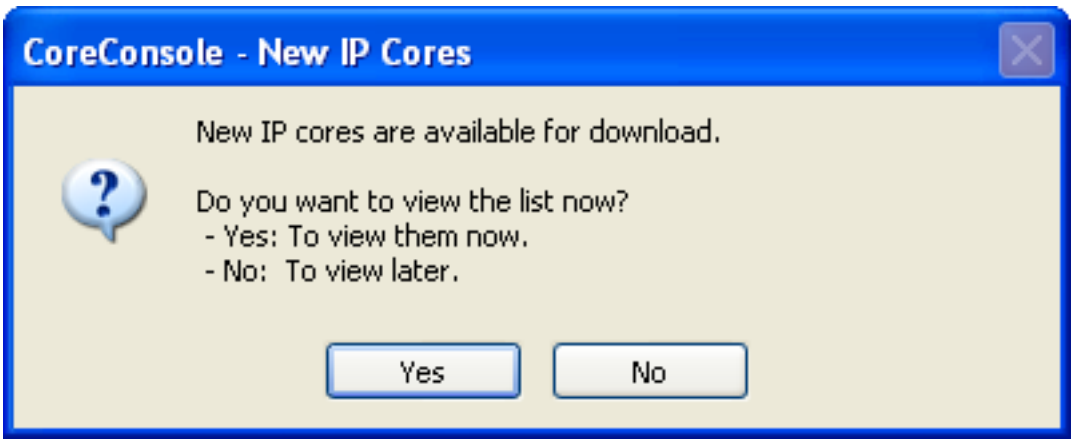


Figure 17 · New IP Dialog Box

Click **Yes** to view the list of cores. This opens the IP Updates dialog box.

CoreConsole remembers which cores you have specifically declined to download. When in **standard** mode, you will only be prompted to choose cores at start up if there are some new cores available.

Manual: No automatic check

CoreConsole will not do any automatic checking. To perform a manual update, click the **Update Now** button in the System Options dialog box, or from the **Actions** menu, select **Show Updates**, this will bring up the IP Updates dialog box. Select the cores you want to download and click the **Get Cores** button.

Internet

The System Options dialog box also allows you to select the URL of the web server from which the updates will be downloaded. The standard URL is *www.actel.com/dataexport/IP*, and it is not recommended to change this URL.

See Also

IP Updates dialog box

Creating a CoreConsole Project

Project Overview

CoreConsole organizes designs into projects. A project is a self-contained collection of all the files and information needed to generate an export set for Libero IDE and various other files including the memory map report, and any SoftConsole support files.

Opening a project

To open an existing project:

1. From the **File** menu, choose **Open.**
2. Select the project from the list of previous projects and click **Open**.

To create a new project:

1. From the **File** menu, choose **New**. The New Design dialog box opens.
2. Enter the design name, and click the **OK** button.

Adding Components

To add a component:

1. Click the Components tab
2. Select the desired component. Information on that component and links to relevant datasheets are displayed in the **Selected Components Details** panel. You may also select which version of that component you wish to use by using the drop-down menu provided in the same panel.
3. Click **Add.** The new component appears in the Schematic window. Repeat this step for any additional component you want to add to your design.

Note: You cannot drag-and-drop components into the Schematic window.

If you are using auto stitching, add the processor, MP7Bridge, and bus (in that order), so that auto stitching does most of the connection work.

Connecting Components

To open the Configuring Connection dialog box:

1. Select a component on the schematic window and click the Connect button  in the toolbar.
2. Click the **Connect** button in the **Component Configuration** dialog box (Figure 18).
3. From the **View** menu, choose **Connections**.

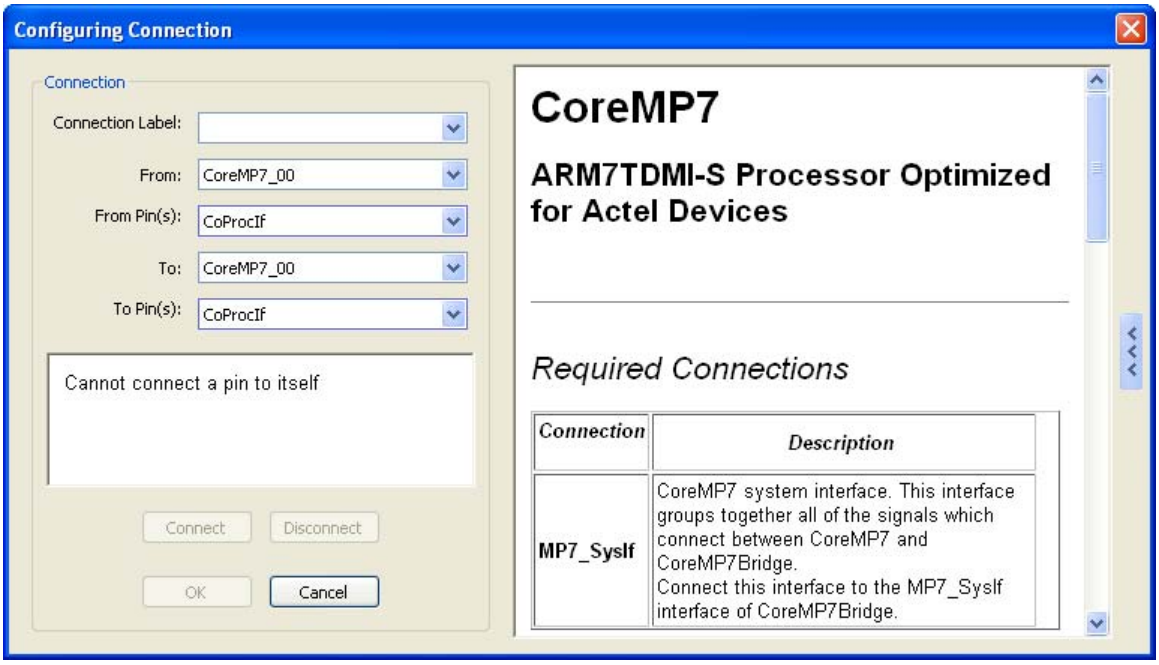


Figure 18 · Configuring Connection Dialog Box

To connect the components:

1. Select the source component in the **From** list.
2. Select the source pin or bus in the **From Pin(s)** list (this can be either an input or an output from this component).
3. Select the destination component in the **To** list.
4. Select the destination pin in the **To Pin(s) list** (this can be either an input or an output from this component). This list only shows compatible pins. If the destination you select is **Top Level**, then the **To Pin(s)** remains blank, and you add or select a label for the connection.
5. If you are connecting to a connection that has not been labeled previously, enter a name in the **Connection Label**. If you are connecting to a point that has been labeled previously, select the name from the list in **Connection Label**.

   If the **From** and **To** component and pins are compatible with the label selected, the **Connect** button will be activated.

   If either the **From** or **To** component and pins are not compatible with the label selected (i.e., if the label is already in use for a net to which it cannot connect), a warning will be given and the **Connect** button will be unavailable.

   If you are making a bus connection, the label will be generated automatically.
6. After all selections are made and the connection is labeled, press **Connect** to make the connection. The status panel below the drop-down lists gives an indication if the attempted connection is allowed or not. The **Connect** and **Ok** buttons remain unavailable until all of the selections and labels are correct. Only the **Connect** button makes the connection. The **OK** button exits the window and does not make a connection.

Connecting to the Bus

When you connect a component to the AHB or ABP bus, CoreConsole automatically assigns a name to the connection. The point at which you connect on the bus also defines your memory map.

Connecting to the Top Level

Connecting to the top level is how you get signals into and out of the CoreConsole project system. These connections are made in the same way as other connections except that the top level does not have pins and you can either select an existing connection from the **Connection Label** drop-down list, or if it does not exist, create a new one.

See Also

Adding CoreMP7

Adding CoreMP7

When adding the CoreMP7 to the system, you must enable or disable the **Debug** option and select a **Die** (Figure 19).

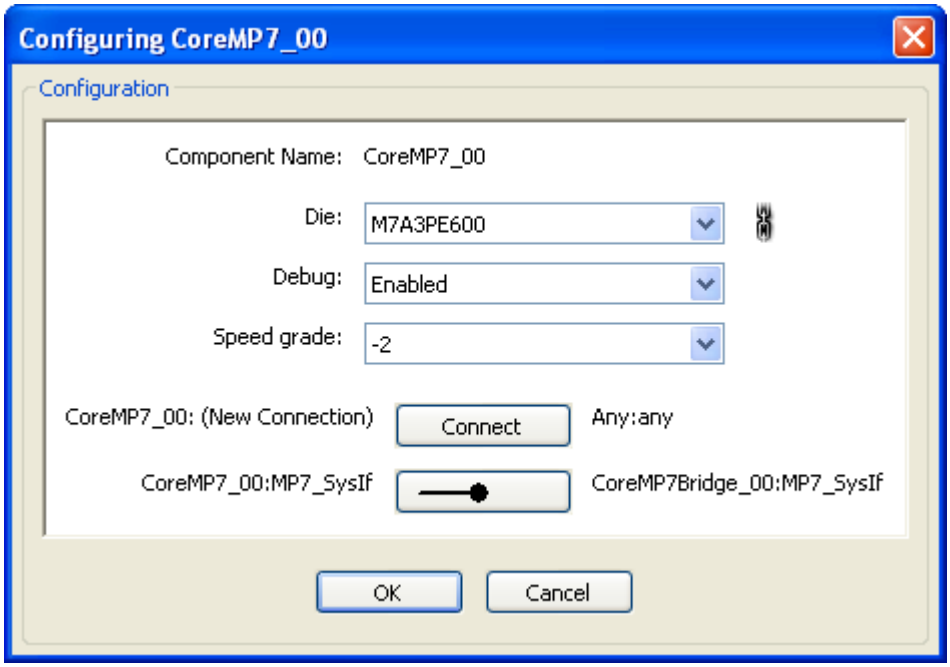


Figure 19 · Debug Option

Die

You must specify a die (target device) for your core. Cores are unique to each device; you must create a new core if you select a new device.

Chain icon

The chain icon indicates that this is a linked parameter. Changing it may lead to changes in other parameters in the design. In this example it ensures that all components in the design are set to use the same die.

Debug

Selecting the debug option includes the debug block in the core; this increases the overall size of the core.

Components Help

Each component has online help associated with it, which can be useful when you need to find out what any or all of its connections are.

The component help can be enabled or disabled from the System Options dialog box.

To enable the Components help:

1. From the **Options** menu, select **System Options**.
2. Check the **Show Connection Help** box.

The help window can be expanded from the side of the component connection dialog window (Figure 20).

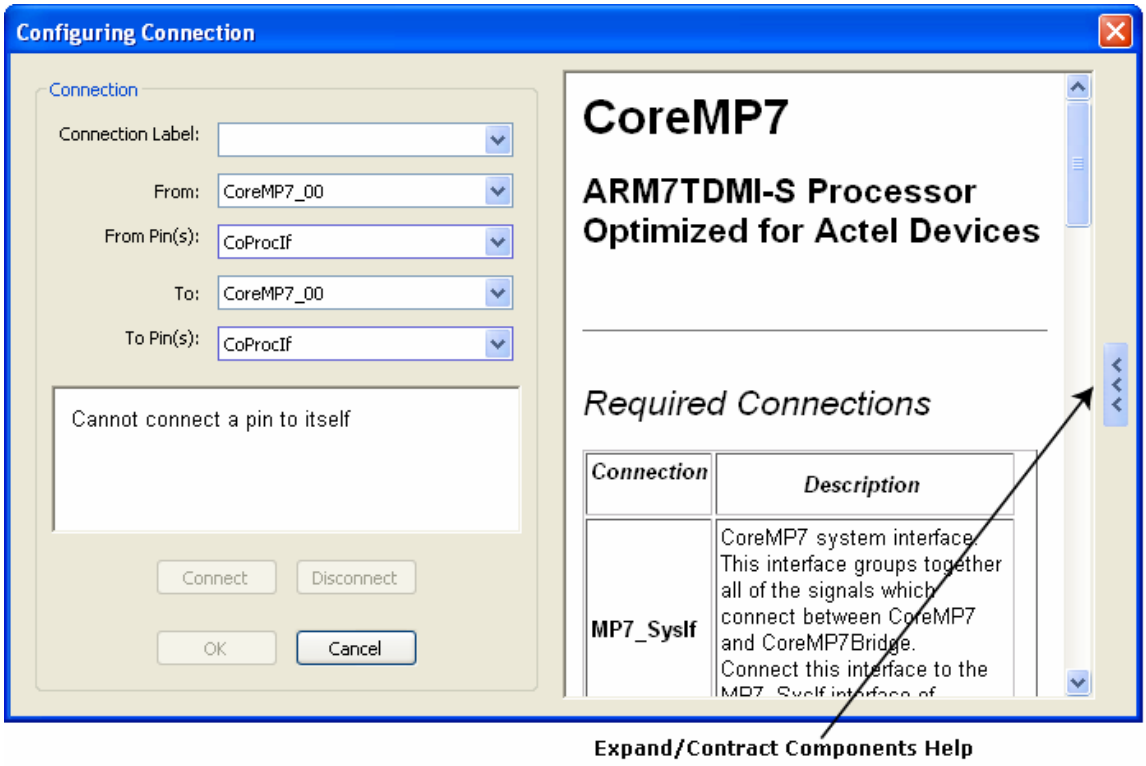


Figure 20 · Components Help

Auto Stitching

CoreConsole has the ability to automatically connect together standard interfaces for components. This is referred to as Auto Stitching. Many of the interfaces to standard components are well defined and uniform, and permit unambiguous automatic connection. These include clock and reset lines, AHB and APB connections, CoreMP7 debug interface and watchdog connections, and others. CoreConsole makes its best guess at which connections need to be made and then presents the list of proposed connections to you for confirmation before making the connections.

Auto stitching can be applied repeatedly and at any time. It is possible to make some of the connections you require manually and then select **Actions > Auto Stitch**. The recommended sequence is: add all the components, auto stitch, and add the additional connections manually (e.g., exporting Rx or Tx from the CoreUART).

Auto stitching is capable of connecting complex components correctly, in particular the watchdog component, which requires different reset connections.

To auto stitch:

1. Add components to your design.
2. From the **Actions** menu, choose **Auto Stitch**. The **Auto Stitching** dialog box appears with CoreConsole's proposed connections (Figure 21).

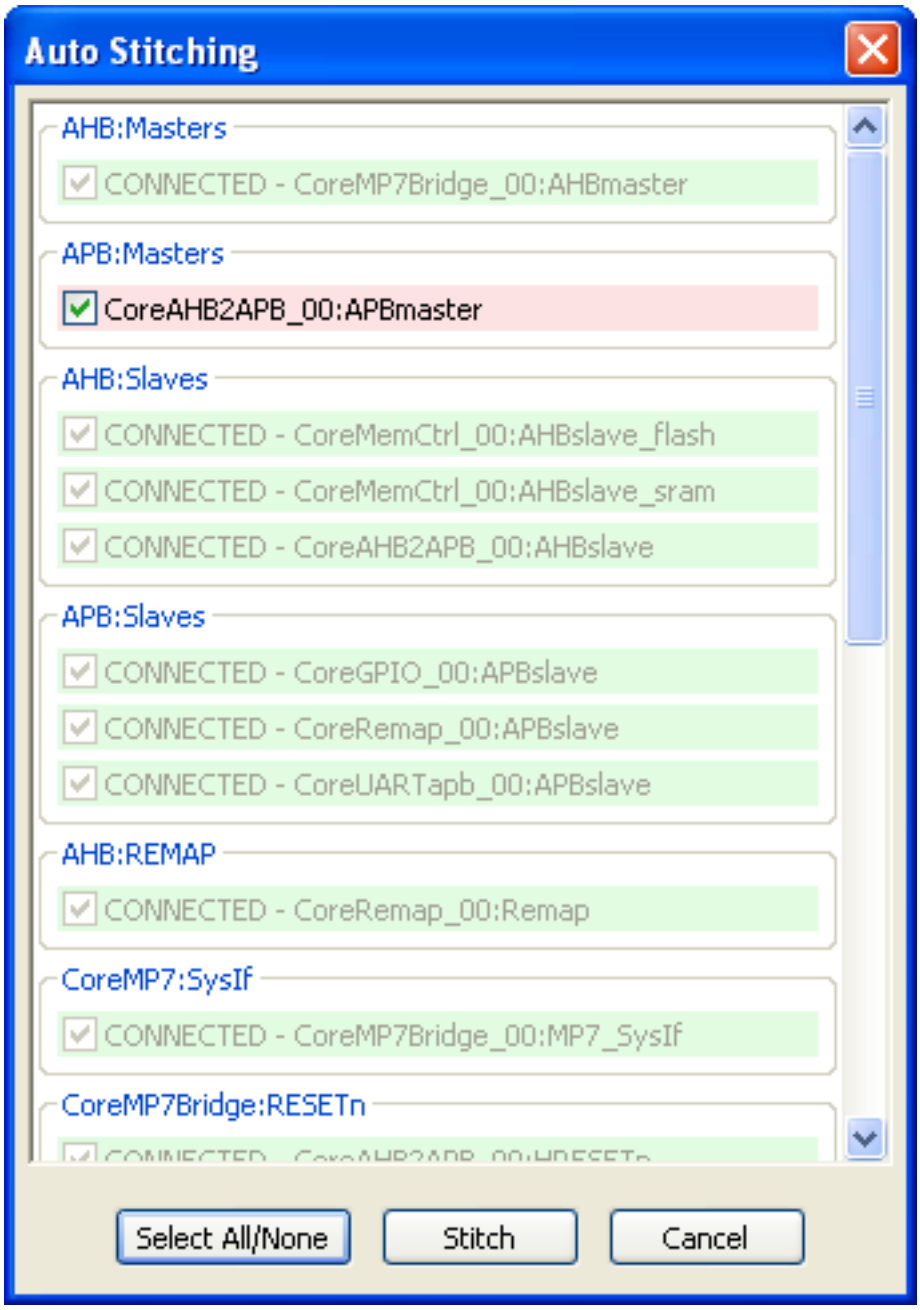


Figure 21 · Auto Stitching

3. If there are any connections you do not wish CoreConsole to make, deselect them in this window.

4. It is possible to select which slot (AHBMaster, AHBSlave or APBSlave) you want to connect to by selecting it from the drop-down menu before stitching.
5. Click **Stitch** and watch as the connections are made.

You can use **Auto Stitch to Top Level** to stitch single components to the top level.

Note: Auto stitch to top level does not rename signals to avoid two signals having the same name. Do not use auto stitch to top level to stitch two instances of the same components to the top level.

To auto stitch to top level:

1. Add components to your design.
2. From the **Actions** menu, choose **Auto Stitch to Top Level**. The **Auto Stitching** dialog box appears with CoreConsole's proposed top-level connections (Figure 22).

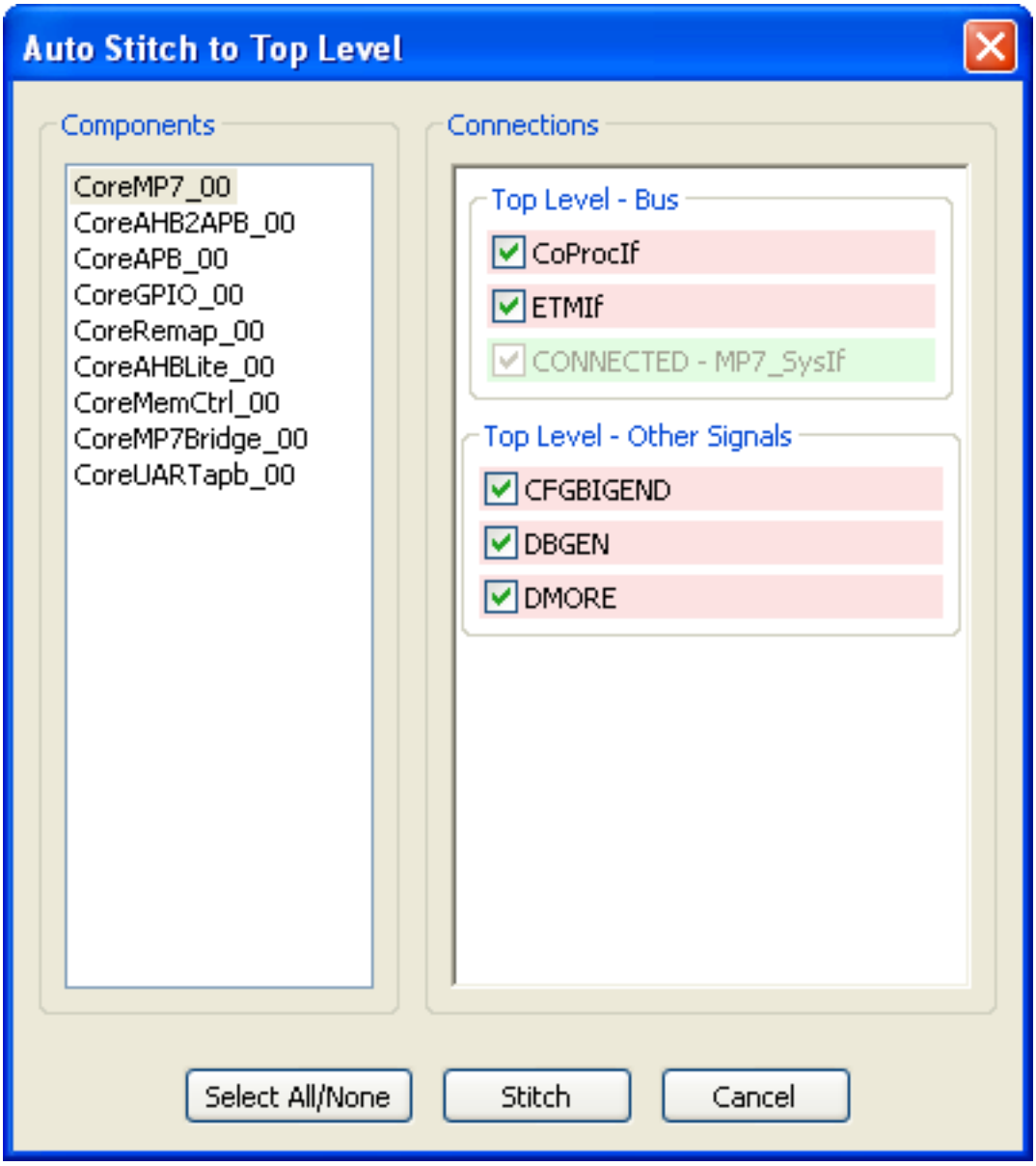


Figure 22 · Auto Stitching to Top Level

3. If there are any connections you do not wish CoreConsole to make, deselect them in this window.
4. Click **Stitch** and watch as the connections are made.

Specifying Memory Map

The bus fabric generated by CoreConsole is either AMBA AHB or APB. The bus fabric consists of an AHB controller, an AHB2APB bridge, and an APB controller. The bridge can be connected to any slot on the AHB bus, setting the addresses for the peripherals connected to it.

The CoreConsole project system memory map is defined by the connections you make to the AHB and APB bus. The specific details of the bus fabric and components can be found in the specific datasheet for the bus or components.

The bus structure is hierarchical with the APB bus: always a slave of the AHB bus. The AHB address space is divided into 16 equal sized slots. Connecting a peripheral component to one of these slots defines its position in the project system memory map. The bridge can be connected to any slot on the AHB, setting the addresses for all the peripherals connected to it.

Memory Map Requirements and Recommendations

CoreMP7 must be added as an AHB Master on the AHB bus.

The memory controller must be connected to Slot0 on the AHB bus, because on reset the processor vectors to this address.

The interrupt controller if present is most often connected to Slot 15 on the AHB bus so that it sits at the top of memory.

It is possible to select which slot (AHBMaster, AHBSlave or APBSlave) you want to connect to by clicking in the drop-down menu in the Auto-Stitching dialog box before stitching.

You can see how each component connection to a bus displays either an M for a bus master or a number (0-15) for a bus slave. This is shown in the bus representation image in Bus Interface Connections and the Standard AMBA bus dialog box connections.

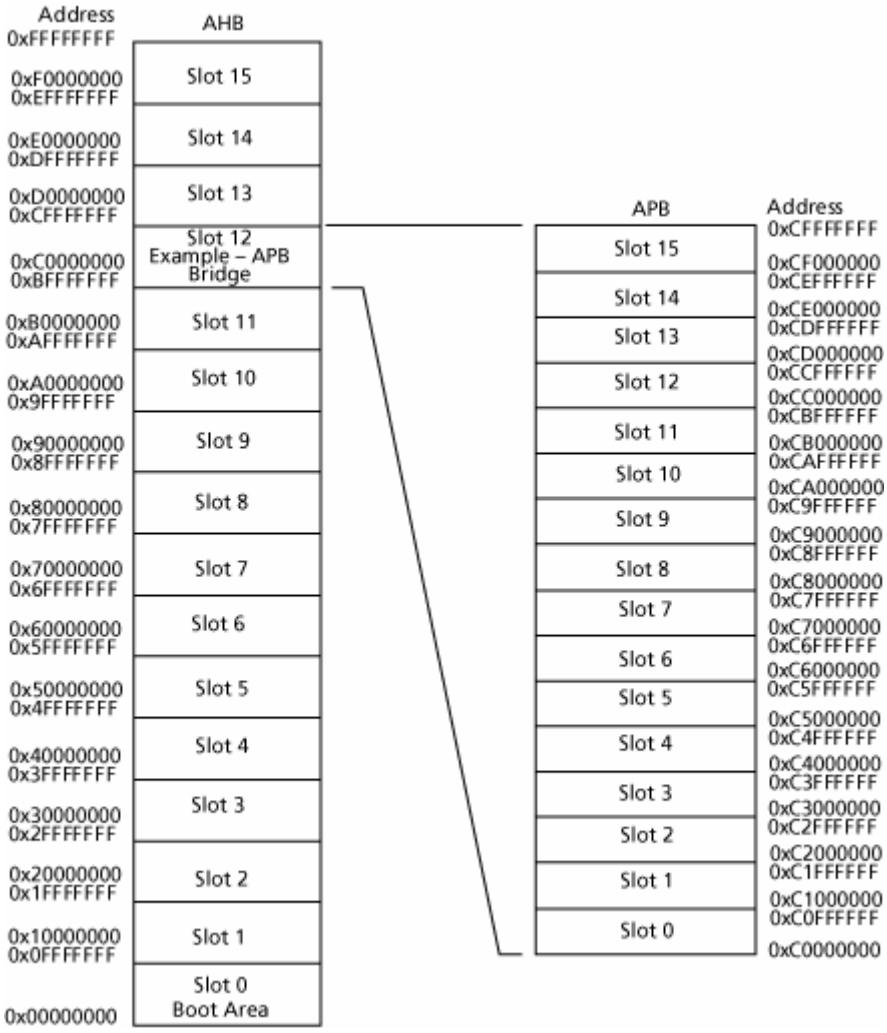


Figure 23 · Project System Memory Map

See Also

Memory map

Auto stitching

Deleting Connections and Components

To delete a component:

1. Move your mouse over a component and click the **Recycle Bin** icon in the **Component Toolbar**.
2. Move your mouse over a component and press the **Delete** key.
3. Right-click a highlighted component to display the shortcut menu and choose **Delete**.

When you delete a component, all of its connections are also deleted.

If you have selected the **Prompt for Component Delete** option in the System Options dialog box, a Confirm Delete dialog box will open. Click Yes to delete the component.

To delete a connection:

1. For bus connections, move your mouse over the connection you wish to remove and click (right or left) or press the **Delete** key.
2. For labeled connections, click the label to bring up the Configuration dialog box and click **Disconnect**.

When you delete a connection, only that specific connection will be removed even if the same source (e.g., CLK) is used elsewhere in the design. When you delete the source driver of a connection with multiple driven pins, the entire net is deleted.

Note: Actions done to the design, including delete or disconnect, are not applied until the project has been saved or generated.

Saving a Project

If you open an existing project, you can save it by choosing **File > Save**, or you can create a new project from the existing project by saving it under a different name by choosing **File > Save As**.

Note: Designs should be saved when you make any changes. There is no undo option.

The **Save and Generate** button on the Generate tab also saves the project before generating the RTL.

Generating a Design

To generate a design:

1. Click the Generate tab.
2. Select the HDL for your generated design.
3. Click the **Save & Generate** button (Figure 24).

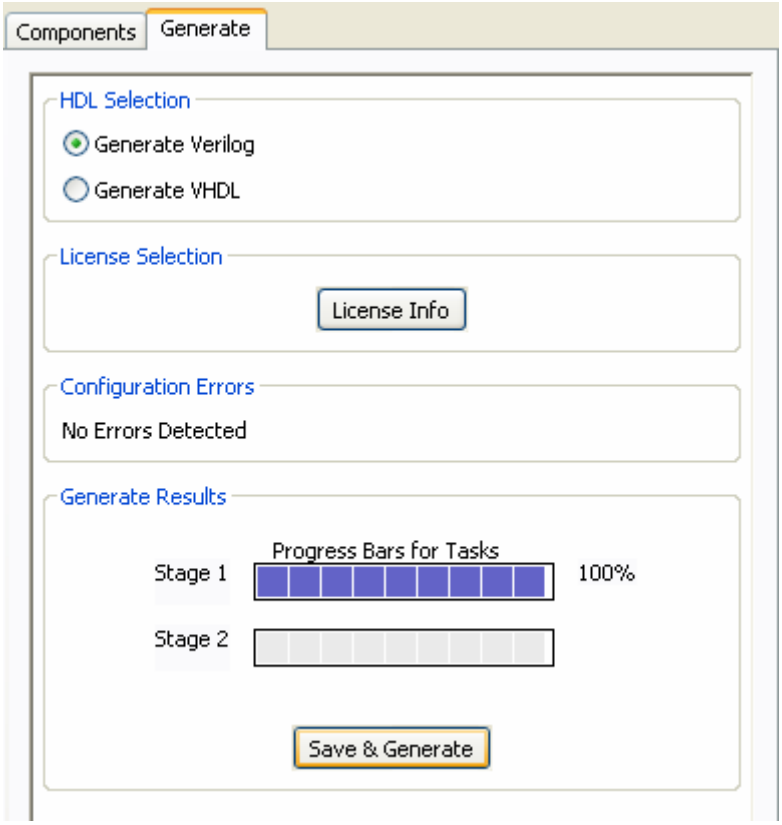


Figure 24 · Generate Tab

HDL Selection

CoreConsole supports both Verilog and VHDL RTL generation. Selecting one or the other will cause your system project design to be generated and saved to disk on your computer in that format.

License Selection

Clicking on the **License Info** button opens a dialog box that lists all of the components and buses in your design and their license status. RTL output is generated only for components and buses for which you have an appropriate license.

Configuration Errors

This section displays configuration errors in your design.

Generate Results

Click the **Save & Generate** button to generate all items in your project design and save it to your specified directory.

Output Files

This section describes the structure of the folders and files generated by standalone CoreConsole.

Note: When CoreConsole is launched from Libero IDE, the CoreConsole design is located under the Libero project folder, with a slightly different file structure, and Libero IDE manages the import of the generated files to the Libero project transparently to the user.

CoreConsole outputs the generated files by default into: *CoreConsole\LiberoExport\<my_coreconsole_project>*

Where *CoreConsole* is the root folder of the CoreConsole installation, and <*my_coreconsole_project*> is the name of the project being generated. These files can be examined by navigating to the folder on your computer.

When you install CoreConsole, you are given the option of selecting the name and location of the *CoreConsole* designs folder, in which case the files are output in <your_selected_folder>*LiberoExport*\<*my_coreconsole_project*>.

Inside the *LiberoExport* folder, you will find the full list of projects. Within each project folder you will find a common folder and project folder; they follow the template:

```
<my_coreconsole_project>/
      <common>/
            <comp1>/
                  <comp1>.cxf
            <comp2>/
                  <comp2>.cxf
      <my_coreconsole_project>/
            <my_coreconsole_project>.cxf
```

The <*my_coreconsole_project*>.*cxf* is an XML file that describes the layout and content of the design, and is used by Libero IDE to import the CoreConsole project. Within the file set for each component there is a <*comp_n*>.*cxf* XML file, and describes the sub-component of the design.

You have to import *my_coreconsole_project/my_coreconsole_project/my_coreconsole_project.cxf* into Libero IDE, and Libero IDE then copies the *my_coreconsole_project* folder and locates all the files in the appropriate locations in the Libero workspace, refer to the Libero User's Guide for more information on importing a CoreConsole project.

Within the output file list there are a variety of different file types associated with the design including the CXF XML description files. Other file extensions used by CoreConsole and accepted by Libero IDE include the following:

Verilog files (sources, stimulus, BFM): *.v

VHDL files (sources, stimulus, packages): *.vhd

Verilog headers: *.h

PDC file: *.pdc

DB file: *.cdb

Simulation files: *.vec

PALACE library: *.lib

SLI Testbench

CoreConsole generates a project system testbench that enables you to test the integrity and connectivity of a design. The testbench is supported by the CoreMP7 Bus Functional Model (BFM) that is output as part of the generated design and imported into Libero IDE.

The testbench creation is fully automatic, but it is possible to extend the level of testing by editing the *subsystem.bfm* test script from within Libero IDE.

The testbench generation logic in CoreConsole assumes that you have named the clock and reset signals coming into the system as **SYSCLK** and **NSYSRESET**, and these are the names it expects to see on the CoreConsole project system port list. The testbench simulation does not run properly if you do not use these names.

Limitations of the Testbench

The testbench only tests within the boundary of the CoreConsole project system design. It does not include memory or other external models.

The testbench tests the connectivity of the project system based on the SPIRIT IP-XACT component definitions. This is done by reading and writing to component registers that are exposed to the AMBA bus. It does not do any functional testing of the components; this has to be done before they are submitted to the CoreConsole database. It is possible for you to extend the testbench to achieve a higher degree of functional testing.

Extending the Generated Testbench and Scripts

When the testbench and script files (*subsystem.bfm*) have been imported into Libero IDE, it is possible to extend them and perform a higher degree of functional testing on a system. The most straightforward method is to extend the *subsystem.bfm* script. The CoreMP7 datasheet gives details of the basic scripting syntax, and it is not difficult to add more or deeper tests to the ones automatically created.

SLI Licensing

CoreConsole uses FLEXlm licensing to enable delivery of IP components. You must acquire the appropriate licenses from Actel. There are two classes of IP component delivery:

Obfuscated: The component is delivered as obfuscated Verilog or VHDL, fully synthesizable RTL. This is not intended for user modification.

RTL: The component is delivered as VHDL or Verilog.

The class of license you have determines the type of component delivered.

Note: If you do not have an IP license but have a CoreConsole license, you can build your design, but you will not be able to Generate it. If you subsequently acquire a license, you can re-open your design and then generate it.

To display licensing information for the components in your design, from the **Generate** menu, choose **License Info** (Figure 25).

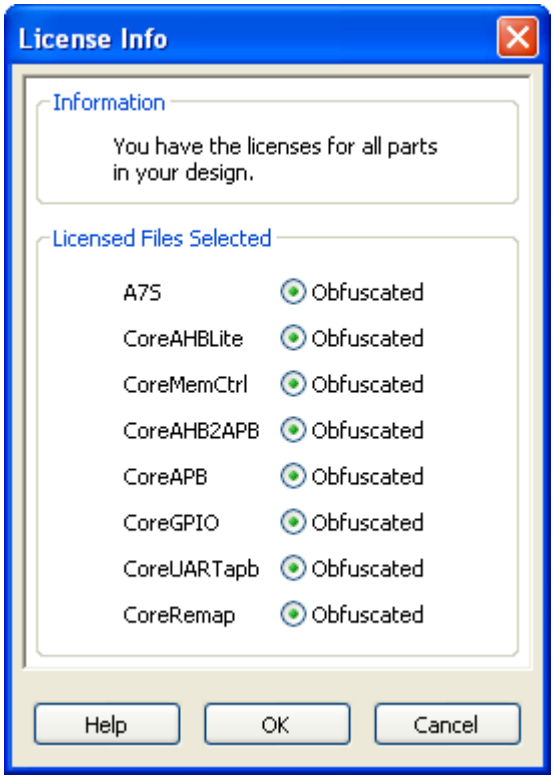


Figure 25 · License Info

If you have licenses for both obfuscated and RTL delivery, you can select which type of output you require on a per component basis by selecting the appropriate box beside each component.

See Also

Obtaining and installing IP
Obtaining an IP license
Installing an IP license

CoreConsole Reference

Menus

File Menu

The following commands are available from the **File** menu:

Table 1 · File Menu Commands

Command	Function
New	Creates a new design
Open	Opens a design into CoreConsole
Save	Saves changes to the working design
Save As	Saves changes to the working design with a new name
Close	Closes the design
Page Setup	Sets up the page for printing
Print	Prints the design
Print Preview	Displays the design in print mode
Exit	Closes CoreConsole

Note: When CoreConsole is launched by Libero IDE, only Page Setup, Print, Print Preview and Exit are available on the File Menu.

View Menu

The following commands are available from the **View** menu:

Table 2 · View Menu Commands

Command	Function
Connections	Displays all connections within the design. Click the connection name to display the Connections dialog box.
Memory Map	Displays the memory map
Debug Logger	This option is reserved for developers
Debug Console	This option is reserved for developers
Float/Dock Design Manager	Floats or docks the design manager

Actions Menu

The following commands are available from the **Actions** menu:

Table 3 · Actions Menu Commands

Command	Function
Recenter Diagram	Centers the design in the schematic window
Auto Layout	Automatically lays out the design, taking account of connections
Auto Stitch	Connects together standard interfaces for components
Auto Stitch To Top Level	Connects components interfaces to the design top level
Change Versions	Changes versions of the IP cores in the design
Show Updates	Opens the IP Updates dialog box and displays a list of available IP for download
Add to Database	Adds a new IP component (CCZ file) to the CoreConsole database
Rebuild Database	Rebuilds the IP database after adding a new IP component

Note: When CoreConsole is launched by Libero IDE, Add to Database and Rebuild Database are not available. You must use standalone CoreConsole to add a new IP Core (CCZ file) to the CoreConsole IP database.

Options Menu

The following commands are available from the **Options** menu:

Table 4 · Options Menu Commands

Command	Function
System Options	Displays the **System Options** dialog box, which allows you to set up the show/hide options, the behaviors and the components catalog.

Help Menu

The following commands are available from the **Help** menu:

Table 5 · Help Menu

Command	Function
Contents	Opens the online help
Licenses	Opens the help topic for obtaining an IP license
Obtaining IP	Opens the help topic for obtaining IP
Reference Docs	Opens the list of reference documents for CoreConsole
About	Displays the current version of CoreConsole

Dialog Boxes and Toolbars

About CoreConsole

The **About CoreConsole** window, available in the Help menu, displays the current CoreConsole version, the current build number, the database checksum and Actel's year of copyright (Figure 26).

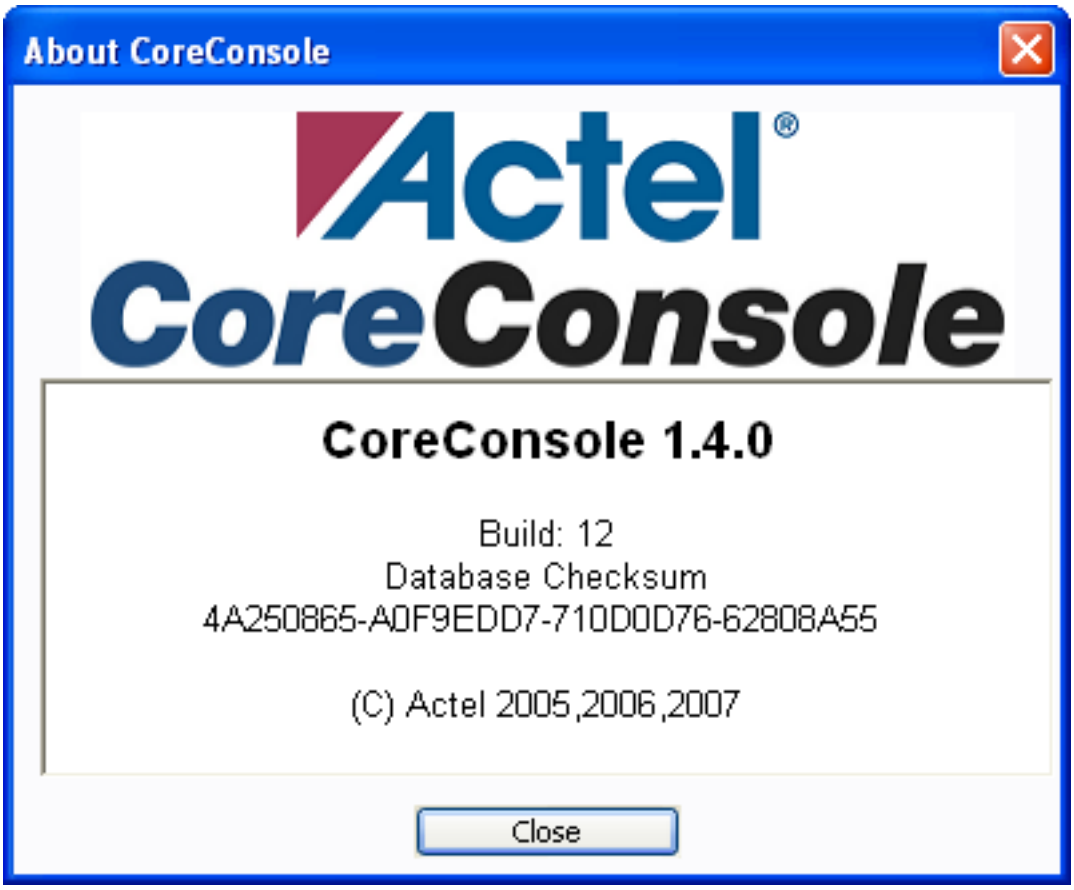


Figure 26 · About CoreConsole

The database checksum displays the checksum of your specific database. The checksum is calculated on the RTL and other files in your database, and reflects any new components or new versions of components you may have added since you installed CoreConsole. Report the database checksum to Technical Support if you have any difficulties. The checksum in the figure above is for illustration only and will differ from your own one.

Auto Stitching

CoreConsole has the ability to automatically connect together standard interfaces for components. This is referred to as Auto Stitching. Many of the interfaces to standard components are well defined and uniform, and permit unambiguous automatic connection. These include clock and reset lines, AHB and APB connections, CoreMP7 debug interface and watchdog connections, and others. CoreConsole makes its best guess at which connections need to be made and then presents the list of proposed connections to you for confirmation before making the connections.

Auto stitching can be applied repeatedly and at any time. It is possible to make some of the connections you require manually and then select **Actions > Auto Stitch**. The recommended sequence is: add all the components, auto stitch, and add the additional connections manually (e.g., exporting Rx or Tx from the CoreUART).

Auto stitching is capable of connecting complex components correctly, in particular the watchdog component, which requires different reset connections.

To auto stitch:

1. Add components to your design.
2. From the **Actions** menu, choose **Auto Stitch**. The **Auto Stitching** dialog box appears with CoreConsole's proposed connections (Figure 27).

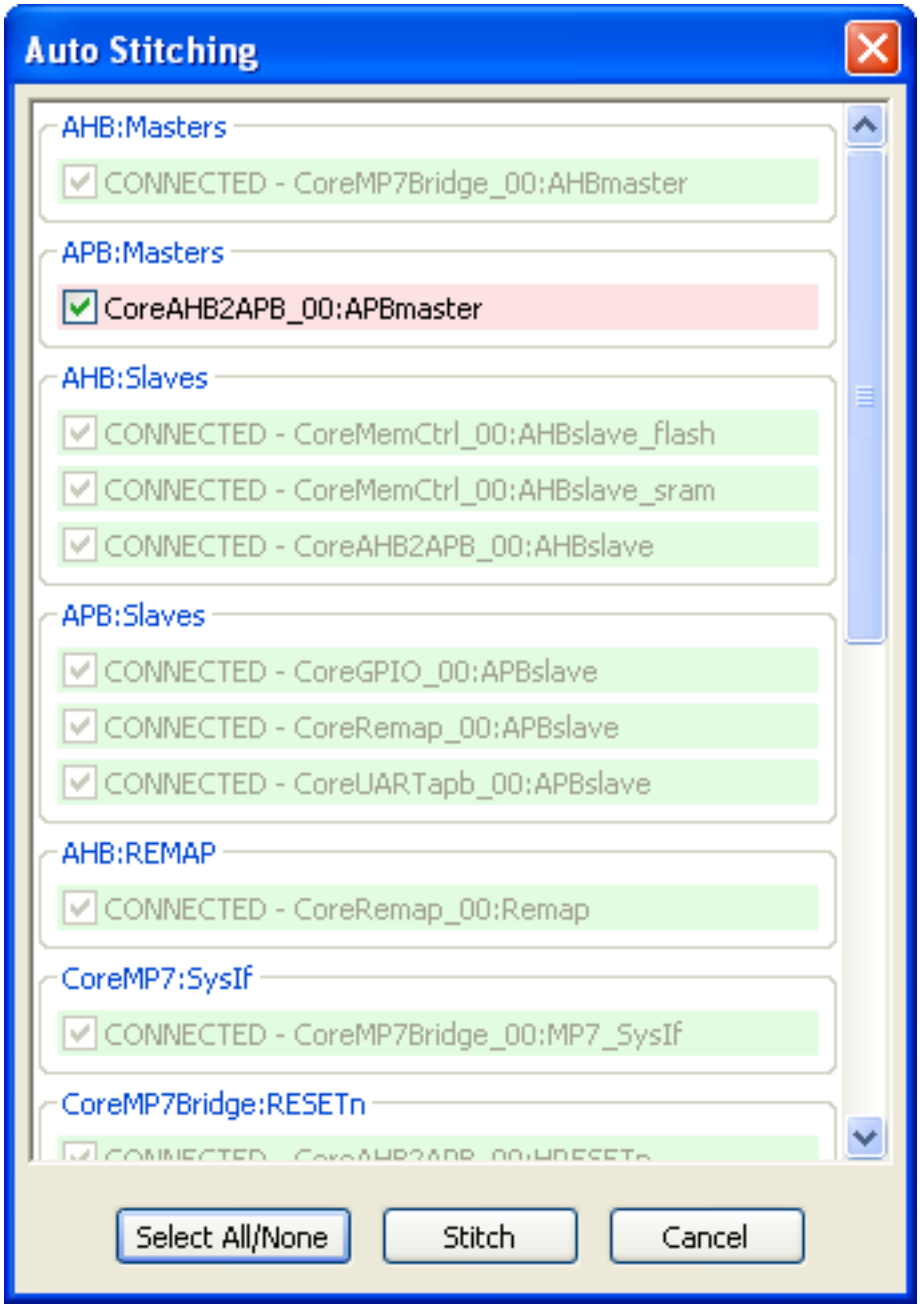


Figure 27 · Auto Stitching

3. If there are any connections you do not wish CoreConsole to make, deselect them in this window.
4. It is possible to select which slot (AHBMaster, AHBSlave or APBSlave) you want to connect to by selecting it from the drop-down menu before stitching.
5. Click **Stitch** and watch as the connections are made.

You can use **Auto Stitch to Top Level** to stitch single components to the top level.

Note: Auto stitch to top level does not rename signals to avoid two signals having the same name. Do not use auto stitch to top level to stitch two instances of the same components to the top level.

To auto stitch to top level:

1. Add components to your design.
2. From the **Actions** menu, choose **Auto Stitch to Top Level**. The **Auto Stitching** dialog box appears with CoreConsole's proposed top-level connections (Figure 28).

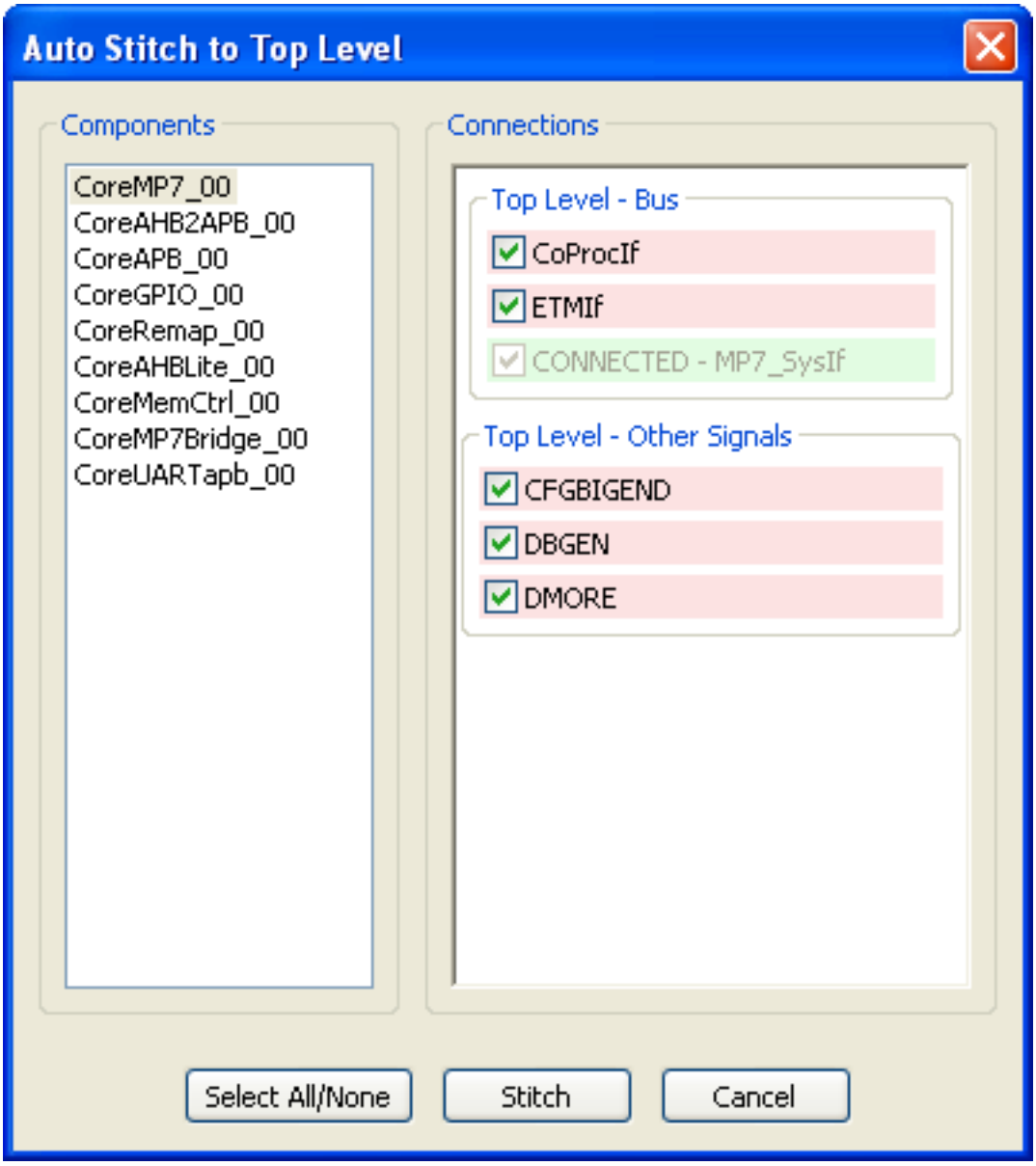


Figure 28 · Auto Stitching to Top Level

3. If there are any connections you do not wish CoreConsole to make, deselect them in this window.

3. Click **Stitch** and watch as the connections are made.

Change Versions

The Change Versionsdialog box, available in the Actions Menu, enables you to change the versions of each component in the schematic window. Select the desired version for each component from the drop-down menu. When you are done with the version changes, click the **Change** button (Figure 29).

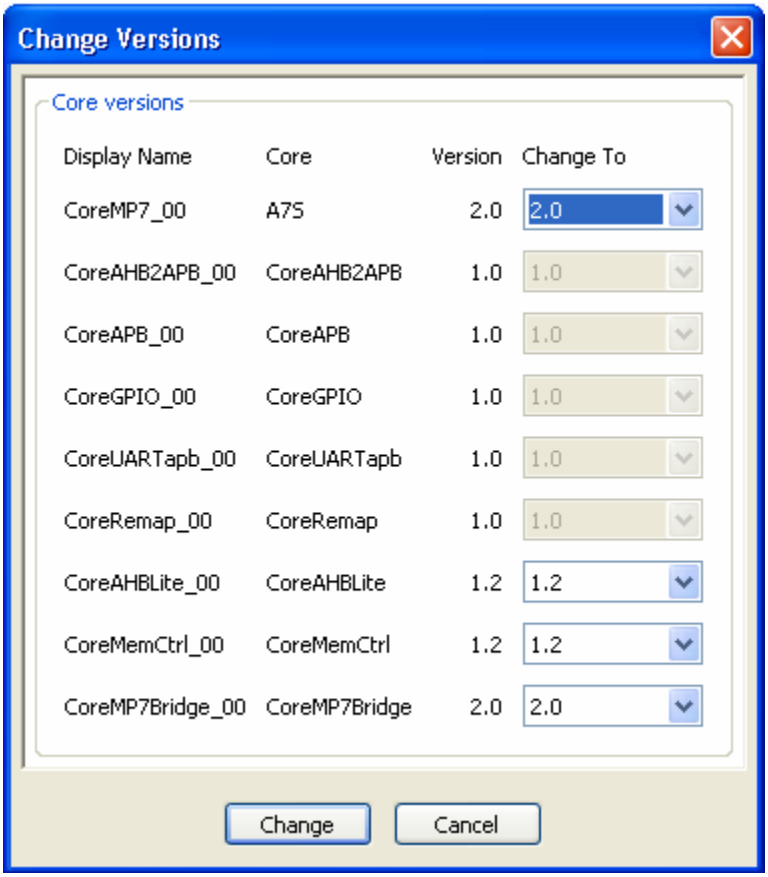


Figure 29 · Change Versions

You can change the version of individual components by right-clicking the desired component and selecting **Change Version** from the drop-down (Figure 30).

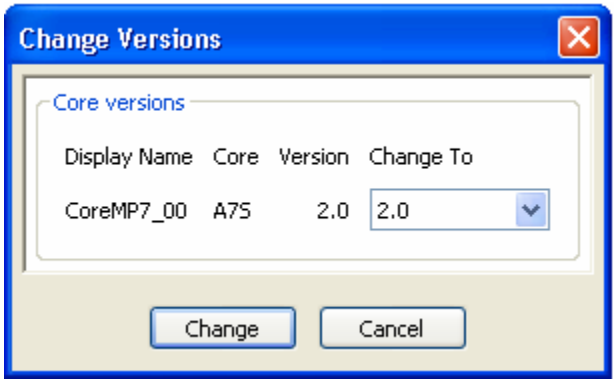


Figure 30 · Change Versions

Changes will not take effect until you save, close and re-open the project.

Component Options

The Component options are available by right-clicking any component in the schematic window.

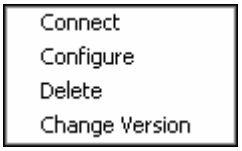


Figure 31 · Component Options

Connect – Displays the Connect Component dialog box.

Configure – Displays the Configure Component dialog box.

Delete – Deletes the selected component and its related connections, see Deleting connections and components.

Change Version – Displays the Change Versions dialog box.

Component Toolbar

The Component toolbar (Figure 32) is available by floating the mouse over any component, wire or bus in the schematic window.

Figure 32 · Component Toolbar

Table 6 · Component Toolbar Options

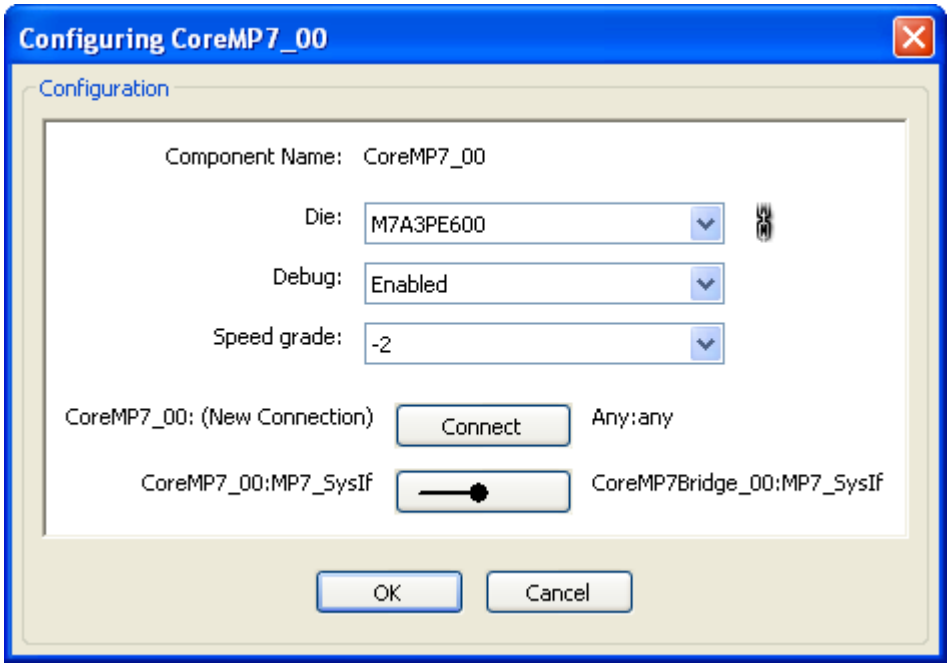
Option	Icon	Description
Connect		Displays the Configuring Connection dialog box
Configure		Displays current configuration for the selected component in the Configure Component dialog box
Delete		Deletes the selected component, wire or bus, see Deleting connections and components
Help		Displays the component toolbar help

See Also

Component options

Configuring Component

The Configuring Component dialog box displays current configuration for the selected component, the example below is for CoreMP7.



Configuring Component: CoreMP7 Example

Die

You must specify a die (target device) for your core. Cores are unique to each device; you must create a new core if you select a new device.

Chain icon

The chain icon indicates that this is a linked parameter. Changing it may lead to changes in other parameters in the design. In this example it ensures that all components in the design are set to use the same die.

Debug

Selecting the debug option includes the debug block in the core; this increases the overall size of the core.

Connecting Components

To open the Configuring Connection dialog box:

1. Select a component on the schematic window and click the Connect button in the toolbar.
2. Click the **Connect** button in the **Component Configuration** dialog box.
3. From the **View** menu, choose **Connections** (Figure 33).

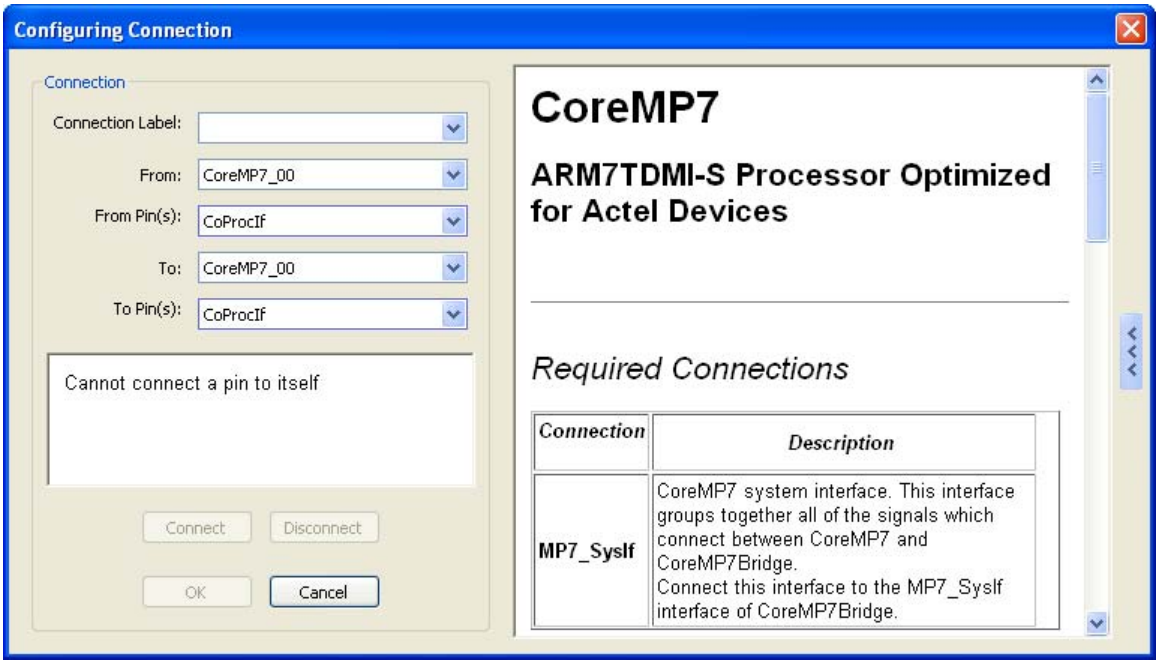


Figure 33 · Configuring Connection Dialog Box

To connect the components:

1. Select the source component in the **From** list.
2. Select the source pin or bus in the **From Pin(s)** list (this can be either an input or an output from this component).
3. Select the destination component in the **To** list.
4. Select the destination pin in the **To Pin(s) list** (this can be either an input or an output from this component). This list only shows compatible pins. If the destination you select is **Top Level**, then the **To Pin(s)** remains blank, and you add or select a label for the connection.
5. If you are connecting to a connection that has not been labeled previously, enter a name in the **Connection Label**. If you are connecting to a point that has been labeled previously, select the name from the list in **Connection Label**.

   If the **From** and **To** component and pins are compatible with the label selected, the **Connect** button will be activated.

   If either the **From** or **To** component and pins are not compatible with the label selected (i.e., if the label is already in use for a net to which it cannot connect), a warning will be given and the **Connect** button will be unavailable.

   If you are making a bus connection, the label will be generated automatically.
6. After all selections are made and the connection is labeled, press **Connect** to make the connection. The status panel below the drop-down lists gives an indication if the attempted connection is allowed or not. The **Connect** and **Ok** buttons remain unavailable until all of the selections and labels are correct. Only the **Connect** button makes the connection. The **OK** button exits the window and does not make a connection.

Connecting to the Bus

When you connect a component to the AHB or ABP bus, CoreConsole automatically assigns a name to the connection. The point at which you connect on the bus also defines your memory map.

Connecting to the Top Level

Connecting to the top level is how you get signals into and out of the CoreConsole project system. These connections are made in the same way as other connections except that the top level does not have pins and you can either select an existing connection from the **Connection Label** drop-down list, or if it does not exist, create a new one.

See Also

Adding CoreMP7

Filter Dialog Box

The Filter dialog box, available from the Components tab, allows you to filter the list of components available in the CoreConsole database. The filter dialog box is organized in 5 sections: Quick Filter, List What?, Sort By, Search Criteria, and Product Family (Figure 34).

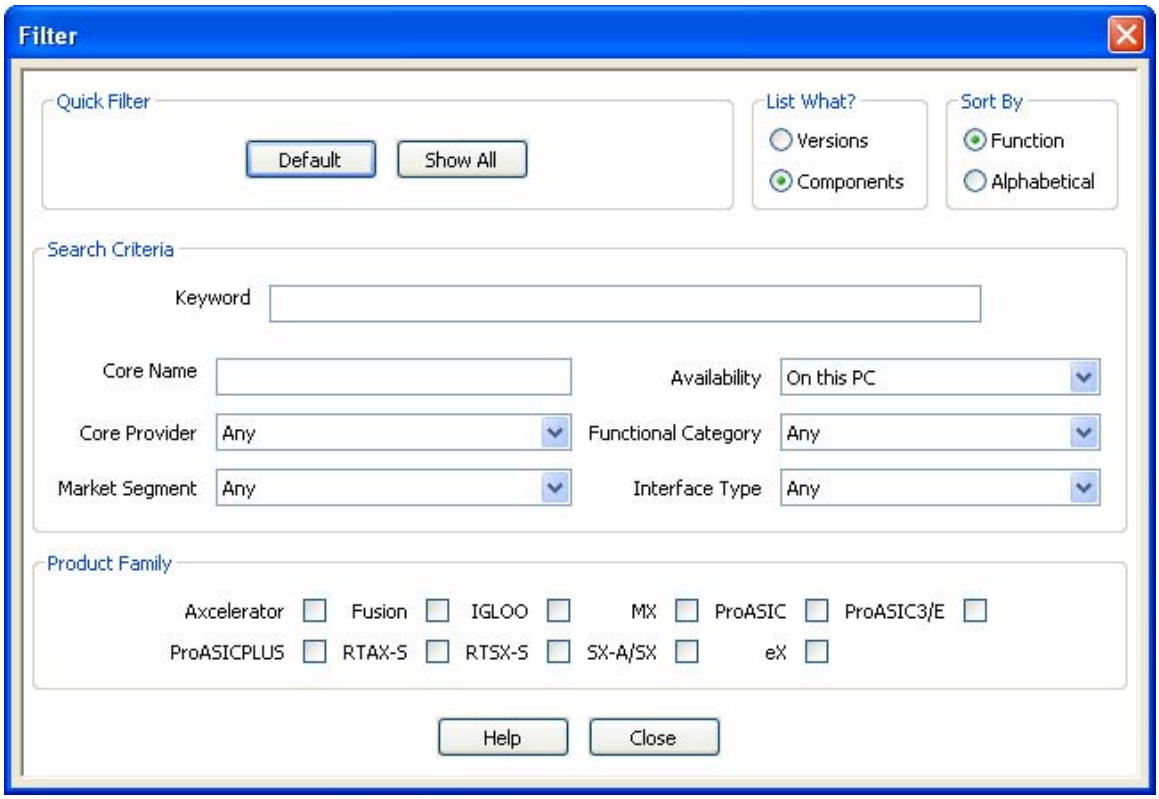


Figure 34 · Filter Dialog Box

Quick Filter

Default – Sets standard settings for the filter.

Show All – Shows all components, including preview components, and all versions of each component.

Note: Note: Selecting either of these buttons modifies the options available in the Search Criteria.

List What?

Versions - shows each version of each component.

Components - shows the most recent version of each component. To display a particular version of the selected component, select the component on the **Components** tab and select a version form the **Version** pull-down menu.

Sort By

Function - The results are sorted by function.

Alphabetical - The results are sorted by alphabetical order.

Search Criteria

The Search Criteria filters the list of components based on the criteria selected. You can add the following criteria:

Keyword - searches the name of the component and the associated text. It uses an exact term search, so if you type *JTAG interface* it looks for that exact term rather than finding text that contain both *JTAG* and *interface*.

Core Name - filters the results based on the core name.

Availability - filters the results based on the availability of the component.

Core Provider - filters the results based on the core provider.

Functional Category - filters the results based on the selected functional category.

Market Segment - filters the results based on the selected market segment.

Interface Type - filters the results based on the selected interface type.

Product Family

When all the boxes are unchecked the filter considers all product families.

When one box is checked, only IP for that family is considered.

When two or more boxes are checked, IP in either of the families is considered.

Note: The selections chosen in List What? and Sort By will remain the same through CoreConsole exit and re-launch, whereas all other selections revert to the Default Settings upon exit.

IP Updates Dialog Box

The IP Updates dialog box appears when the manual or the standard update options are checked in the system options dialog box.

The Updates dialog box is divided into the IP Cores Available for Download panel and the Details panel (Figure 35).

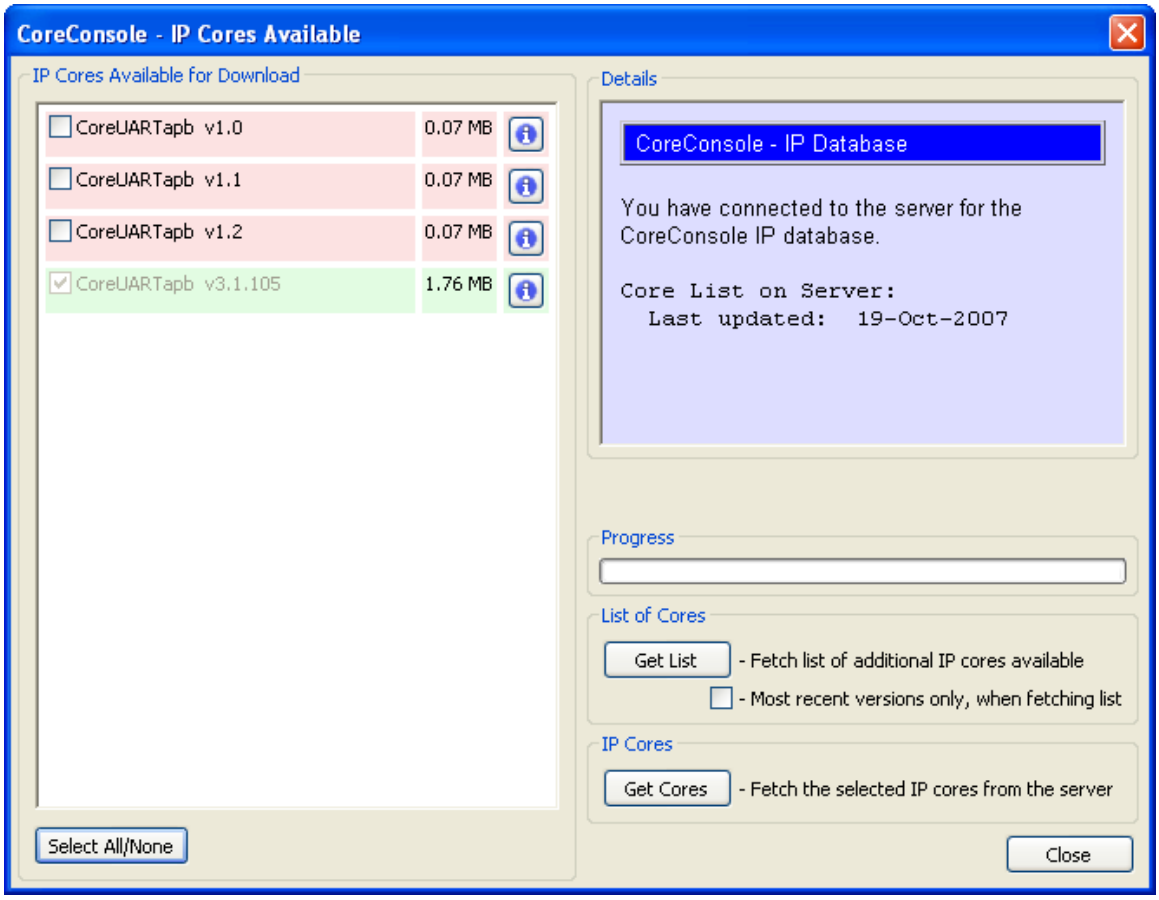


Figure 35 · IP Updates Dialog Box

IP Cores Available for Download

The IP Cores Available for Download panel lists IP available for download and not present in the local CoreConsole database. Items in green have been downloaded to your machine but have not yet been installed. Items in pink are available for download. Click the icon to obtain more information about that IP core in the details panel.

Use the **Select All/None** button to select all or none of the cores.

CoreConsole remembers which cores you have specifically declined to download. When in **Standard: Check for updates at start up mode**, you will only be prompted to choose cores at start up if there are some new cores available.

Details

The details panel gives information about the database on the remote server and additional information about upgrades to CoreConsole. The detail panel also displays information about a specific core when you click the icon on the Cores Available for Download panel.

If there are any problems connecting with the server, the details panel will also provide information about the error.

The **Get List** button refreshes the list of cores from the server. If you had problems contacting the server or have just changed the URL, you can press this button to try again. Only the most recent version of each core on the server will ever be shown. If you uncheck **most recent version only** and click **Get List**, a full list of cores will be shown, including legacy cores, but excluding cores already on your local server.

Click **Get Cores** to download the selected cores from the server. A progress indicator shows the download progress. The **Close** button changes to **Hide**, click the **Hide** button to hide the dialog and return to CoreConsole while the

download continues in the background. When all downloads are complete, the Download Complete dialog box will appear (Figure 36).

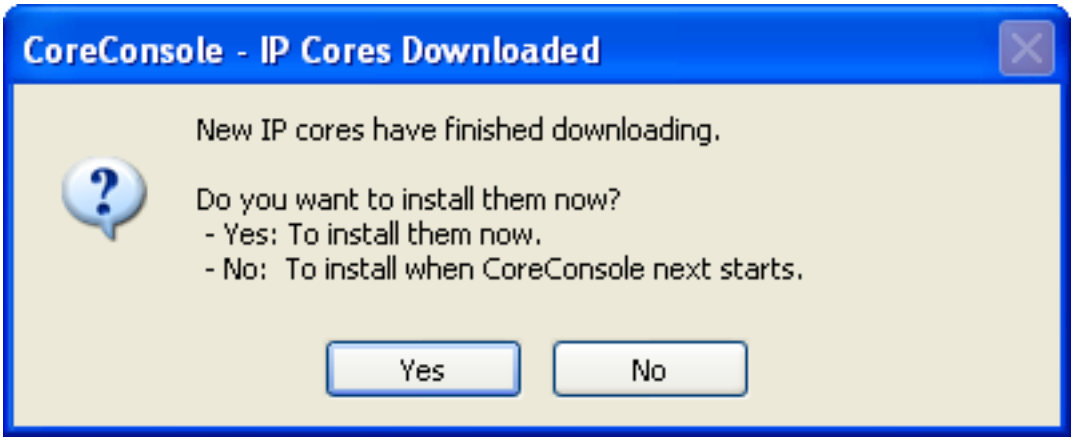


Figure 36 · IP Download Complete Dialog Box

Click **Yes** to install the cores, and they will appear on the **Components** tab. If you click **No**, the next time you start CoreConsole, the Add Downloaded IP to Database dialog box will appear (Figure 37). The message will continue to show each time you restart CoreConsole until you accept installing the downloaded cores.

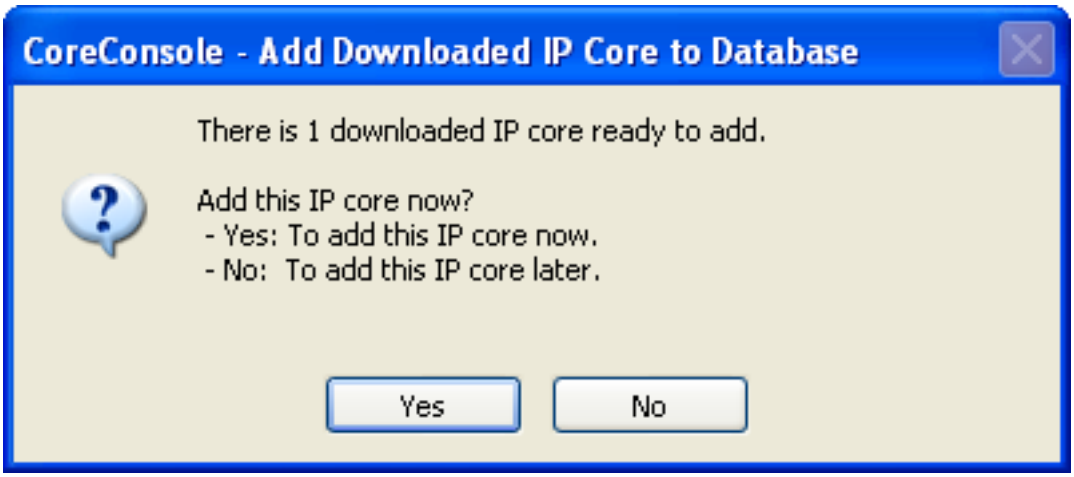


Figure 37 · Add Downloaded IP to Database Dialog Box

Click **Yes** to install the cores, and they will appear on the **Components** tab.

See Also

System Options dialog box - Updates tab

License Info

The **License Info** dialog box, available in the Generate tab, provides license information for all parts of your design. CoreConsole uses FLEXlm licensing to enable delivery of IP Components. Therefore you need to acquire the appropriate License from Actel. There are three classes of IP Component Delivery:

Obfuscated - The component is delivered as obfuscated Verilog or VHDL, fully synthesizable RTL. This is not intended for user modification.

RTL - The component is delivered as clear VHDL or Verilog.

Eval - The component is available as a pre-compiled ModelSim library. This restricts use to Simulation only.

The class of license you have determines the type of delivered component.

If you do not have an IP License but have a CoreConsole license, you can build your design, but you will not be able to generate it. If you subsequently acquire a license, you can re-open your design and then generate it (see Figure 38).

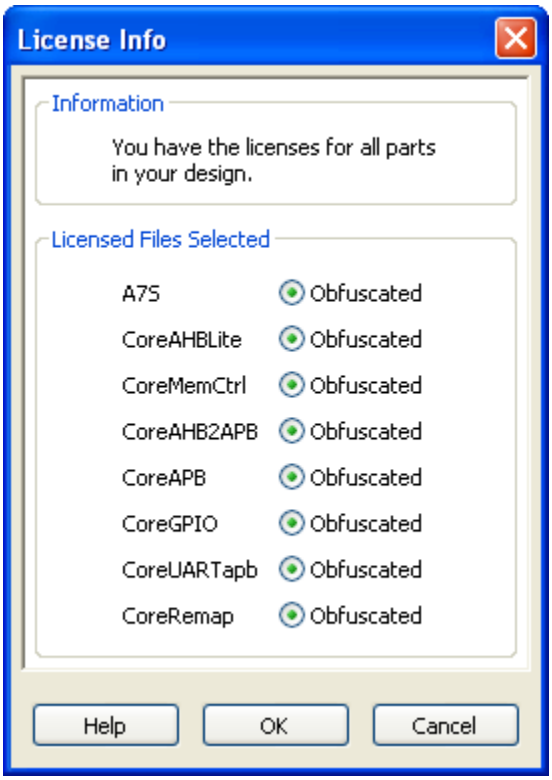


Figure 38 · License Info Dialog Box

See Also

Generate tab

Generating a design

CoreConsole Licensing

Obtaining an IP license

Memory Map

The **Memory Map** window, available in the View menu, displays the memory mapping for the current generated schematic (Figure 39).

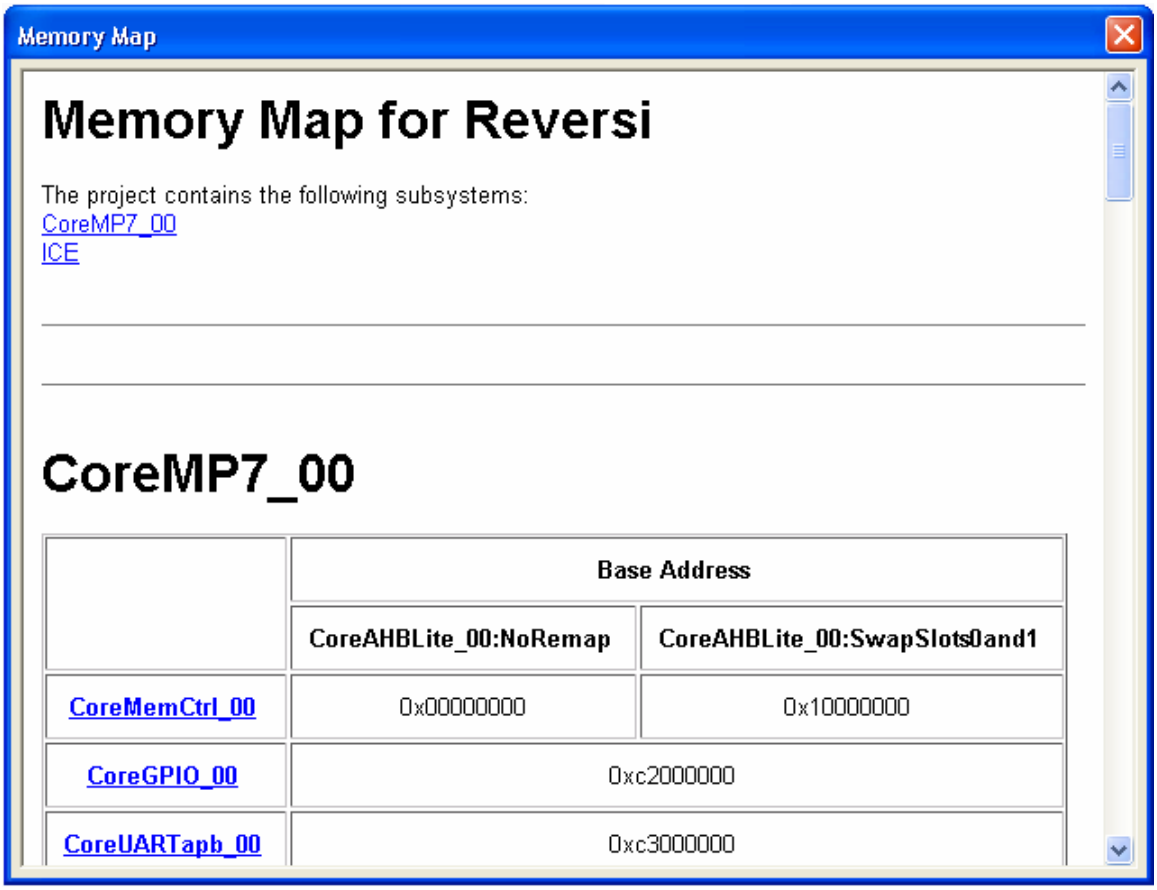


Figure 39 · Memory Map

In the **Memory Map** window, you can view each component and their individual memory mapping, showing range, type, width, name, description, bit offset, address and reset value relevant to each component.

See Also

Auto stitching

Specifying memory map

System Options

The **System Options** dialog box controls the display on the schematic window through the **General** tab and the IP cores updates through the **Updates** tab.

To open the system options dialog box, from the Options menu, choose System Options.

General Tab

The General tab controls the display on the schematic window (Figure 40).

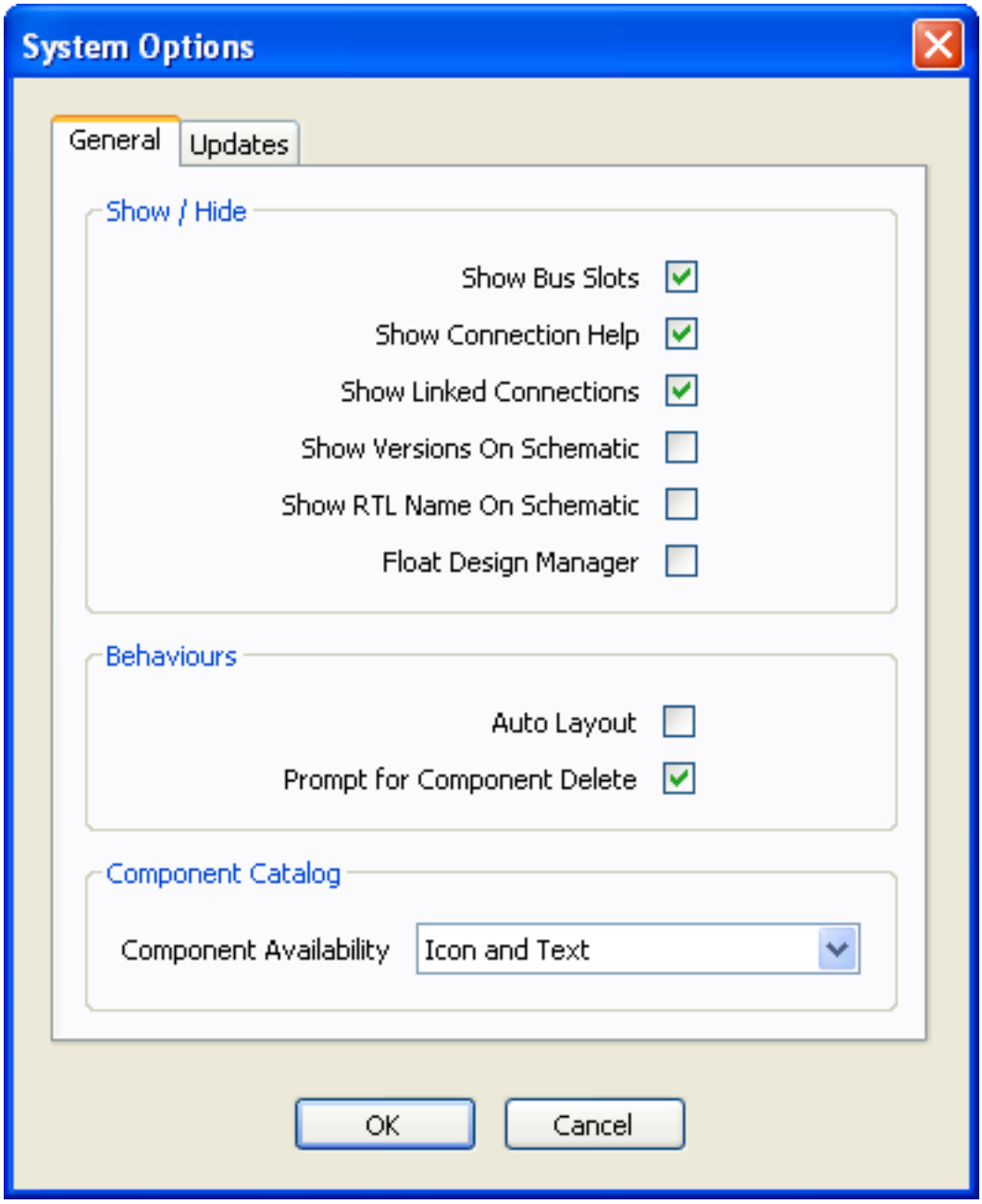


Figure 40 · System Options Dialog Box - General Tab

The following options are available:

Show Bus Slots

Choose this option to display the slot number on the bus to which each component is attached. The slot number indicates the component's location in the project system memory map. If it is not selected, the slot number is replaced by a connection point only.

Show Connection Help

This option enables the help window for each component. See Components help for more information.

Show Linked Connections

Select this option to float over a connection in the schematic and highlight all the other points connected to the net.

Show Versions on Schematic

Select this option to display the version number of each block under the component name of the block.

Show RTL Name on the Schematic

Select this option to display the RTL name of each block in your design under the component name.

Float Design Manager

Select this option to unlock the Design Manager (Components and Generate) tabs and move them around the screen; this enables you to create more screen area for the schematic window.

Auto Layout

Select this option to automatically place the components drawn in the schematic window.

Prompt for Component Delete

Select this option to enable or disable the confirm delete dialog box.

Component Availability

Set this option to display a components license status as icon and text, icon only, text only, or don't show.

Updates Tab

The **Updates** tab enables you to choose from several IP core update methods (Figure 41).

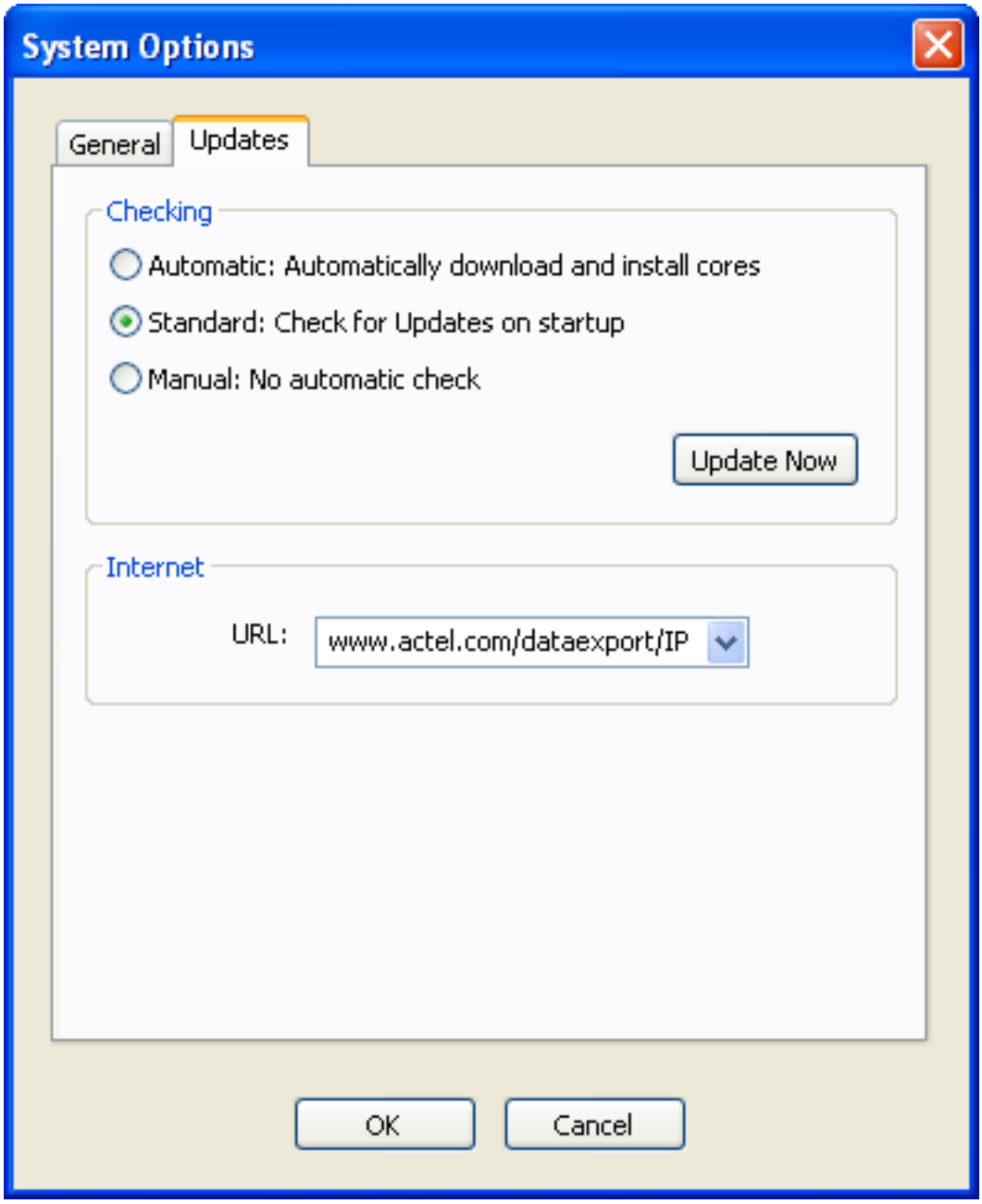


Figure 41 · System Options Dialog Box - Updates Tab

Automatic: Automatically download and install cores

CoreConsole will obtain the most recent versions of any cores on the update server that are not already in your database. When the cores have been downloaded, CoreConsole will prompt you to install them (Figure 42).

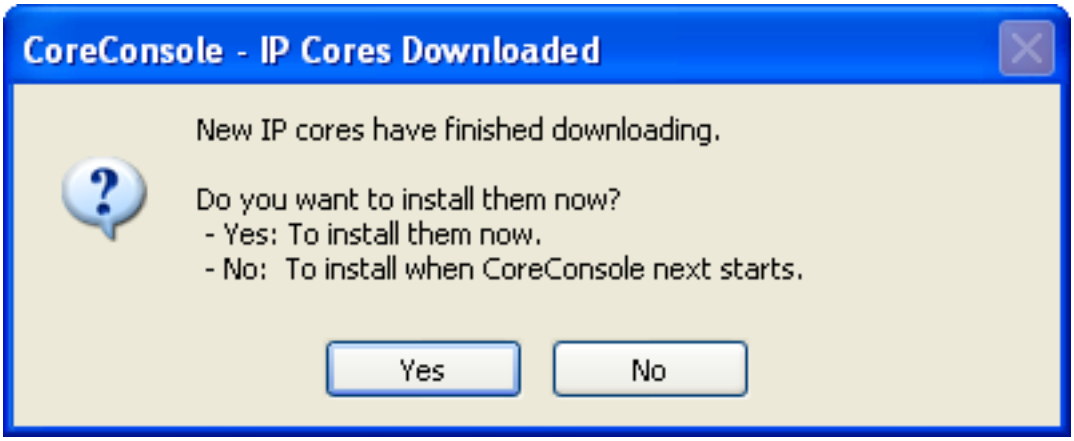


Figure 42 · IP Download Complete Dialog Box

Click **Yes** to install the cores, and they will appear on the **Components** tab. If you click **No**, the next time you start CoreConsole, the Add Downloaded IP to Database dialog box will appear. The message will continue to show each time you restart CoreConsole until you accept installing the downloaded cores.

Standard: Check for updates on startup

CoreConsole will automatically obtain a list of the most recent versions of any cores on the update server on startup. This is the default option. If the list contains any new cores that are not in your database and that you have not previously declined, the New IP dialog box appears (Figure 43).

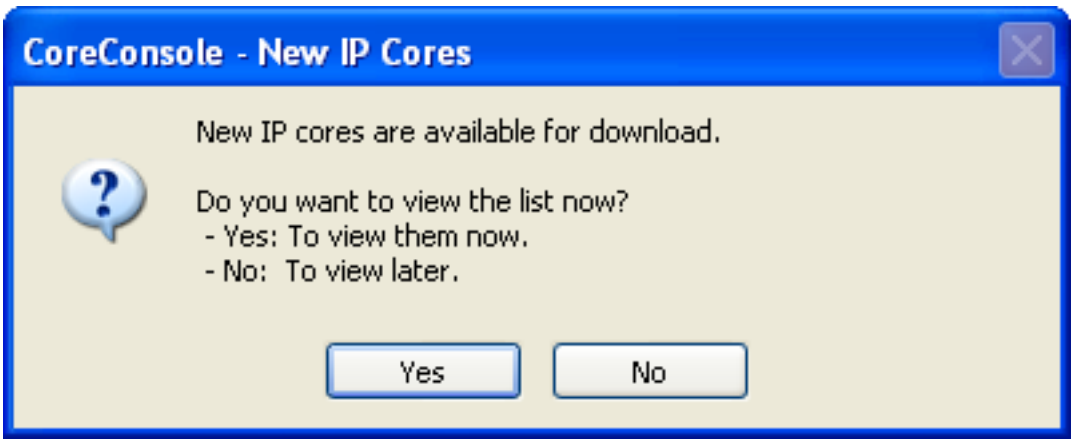


Figure 43 · New IP Dialog Box

Click **Yes** to view the list of cores. This opens the IP Updates dialog box.

CoreConsole remembers which cores you have specifically declined to download. When in **standard** mode, you will only be prompted to choose cores at start up if there are some new cores available.

Manual: No automatic check

CoreConsole will not do any automatic checking. To perform a manual update, click the **Update Now** button in the System Options dialog box, or from the **Actions** menu, select **Show Updates**, this will bring up the IP Updates dialog box. Select the cores you want to download and click the **Get Cores** button.

Internet

The System Options dialog box also allows you to select the URL of the web server from which the updates will be downloaded. The standard URL is *www.actel.com/dataexport/IP*, and it is not recommended to change this URL.

See Also

IP Updates dialog box

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (http://www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at http://www.actel.com/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

For more information about Actel's products, visit our website at http://www.actel.com

Actel Corporation *• 2061 Stierlin Court • Mountain View, CA 94043 USA*
Phone 650.318.4200 • Fax 650.318.4600 • Customer Service: 650.318.1010 • Customer Applications Center: 800.262.1060

Actel Europe Ltd*. • River Court, Meadows Business Park • Station Approach, Blackwater • Camberley Surrey GU17 9AB • United Kingdom*
Phone +44 (0) 1276 609 300 • Fax +44 (0) 1276 607 540

Actel Japan *• EXOS Ebisu Bldg. 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan*
Phone +81.03.3445.7671 • Fax +81.03.3445.7668 • www.jp.actel.com

Actel Hong Kong *• Suite 2114, Two Pacific Place • 88 Queensway, Admiralty • Hong Kong*
Phone +852 2185 6460 • Fax +852 2185 6488 • www.actel.com.cn

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