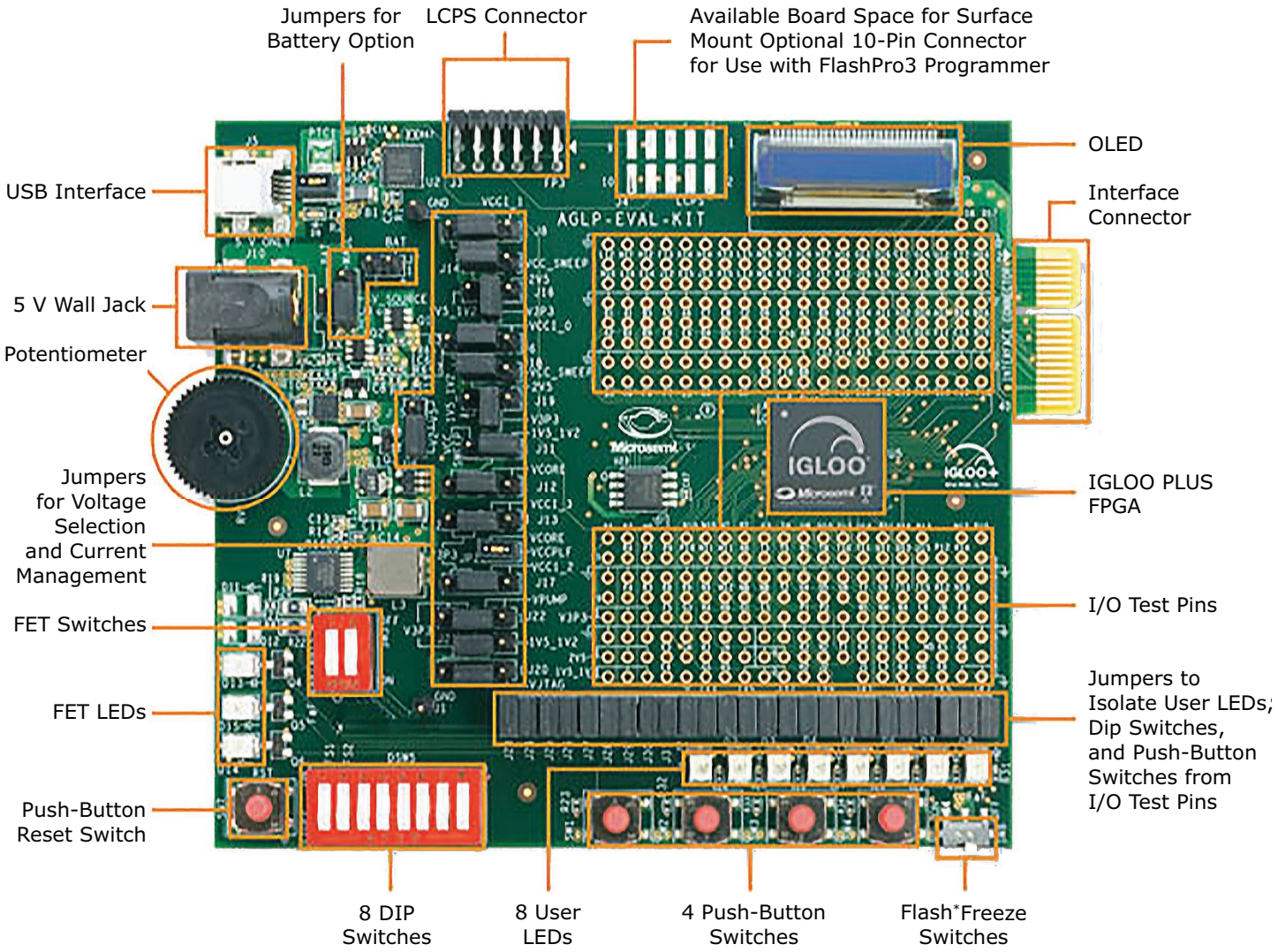
IGLOO PLUS Starter Kit Quickstart Card

Kit Contents—AGLP-EVAL-KIT

Quantity	Description
1	IGLOO PLUS Evaluation Board with AGLP125-CSG289 IGLOO PLUS device
1	FlashPro3-compatible programmer
1	5 V power supply
1	USB 2.0 high-speed cables and packet of jumpers
1	Quickstart card



Overview

The IGLOO PLUS Starter Kit board is intended to provide a low-cost system platfor for evaluating IGLOO PLUS (AGLP) technology, such as low-power, I/O state preservation during Flash*Freeze mode, and Schmitt triggered I/Os. The board also enables use of hot-swappable FPGA I/Os in the Expansion Header, and Schmitt triggered FPGA inputs for improved noise immunity.

Jumper Settings

The following table lists the default factory-supplied jumper settings required for the preprogrammed demonstration designs to function. The current measurement jumpers must be connected to permit current to flow.

Jumper	Setting	Comment
J6	Pin 2–3	Remove jumper to disconnect VCCI_0 power
J7	Remove	Remove jumper to disconnect external battery source
J8	Pin 2–3	Remove jumper to disconnect VCCI_1 power
J9	Pin 1–4	Select WALL, BAT, VUSB for 5V_SOURCE Pin 1–4 = VUSB Pin 2–4 = BAT Pin 3–4 = WALL
J11*	Pin 1–2	Select VCC or VCC_SWEEP for VCORE Pin 1–2 = VCC Pin 3–2 = VCC_SWEEP
J12	Pin 2–3	Current measurement header for VCORE
J13	Pin 2–3	Current measurement header for VCCI_3
J14*	Pin 1–2	Select VCC or VCC_SWEEP for VCORE Pin 1–2 = VCC Pin 3–2 = VCC_SWEEP
J15*	Pin 2–3	Select VJTAGENB or 3.3 V Pin 2–3 = VJTAGENB Pin 1–2 = 3.3 V
J16*	Pin 2–4	Select 3.3 V, 1.5/1.2 V, or 2.5 V for VCCI_1 Pin 2–4 = 3.3 V Pin 3–4 = 1.5 V or 1.2 V Pin 1–4= 2.5 V
J17	Pin 2–3	Current measurement header for VCCI_2
J18	Pin 1–2	Select VCC or VCC_SWEEP for VCCI_0 Pin 1–2 = VCC Pin 3–2 = VCC_SWEEP

Jumper	Setting	Comment
J19*	Pin 2–4	Select 3.3 V, 1.5/1.2 V, or 2.5 V for VCCI_0 Pin 2–4 = 3.3 V Pin 3–4 = 1.5 V or 1.2 V Pin 1–4 = 2.5 V
J20	Pin 2–3	Current measurement header for VJTAG
J21*	Pin 1–2	Select 3.3 V or 1.5/1.2 V for VJTAG Pin 1–2 = 3.3 V Pin 2–3 = 1.5 V or 1.2 V
J22	Pin2–3	Current measurement header for VPUMP

*Voltage selection jumper.

Remove short default jumpers to disconnect LEDs and switches from FPGA: J40–J47 for the 8 LEDs, J28–J35 for DIP switches DSW5, and J36-J39 for the 4 push-button switches, SW1 to SW4. All DIP switches should be closed.

To enable Flash*Freeze mode, slide SW8 toward ON. To disable Flash*Freeze mode, slide SW8 toward OFF. In Flash*Freeze mode, FPGA current consumption will drop below 50 µA.

Demo Design 1—IGLOO PLUS Counter

This design demonstrates a LED a binary counter with various frequenceis using dip-switches.

1. Plug one end of the USB cable into a powered USB hub or a powered PC.
2. Plug the other end of the USB cable into the board to power it up. The board is powered from the USB connection and no external supply is required. A 5 V wall-jack connector is provided on the board as an alternative if USB power is not available.
3. Verify the green LED next to the USB jack is ON.
4. Press and release the System Reset button to reset the IGLOO PLUS FPGA. LED D1 is ON during reset.
5. LEDs D[3:8] represent a binary counter which counts up from 000000 to 111111 and loops back. After reset, LEDs D[3:8] should restart counting from zero.

Demo Design 2—Flash*Freeze Demonstration

This design demonstrates the IGLOO PLUS ability to save power while holding an internal logging state while in Flash*Freeze mode.

1. Slide the F*F switch to ON to enter Flash*Freeze mode.
2. LEDs D[1:8] retain the last state they were driven to when Flash*Freeze was asserted. Their ON state is weak since they are driven by the weak hold state resistors.
3. Slide the F*F switch to OFF to exit Flash*Freeze mode. LEDs D[3:8] resume counting from the count value prior to entering Flash*Freeze mode.
4. To measure the power of the FPGA core during and after Flash*Freeze mode, remove jumper J12 and use a multimeter across J12 that can read µA current.

Software and Licensing

Libero® SoC Design Suite is required for designing with the IGLOO PLUS Starter Kit.

Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's low power Flash FPGAs and SoC. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management and debug capabilities.

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Documentation Resources

For information about the IGLOO PLUS Starter Kit, including user's guides, tutorials, and design examples, see the documentation at
www.microsemi.com/products/fpga-soc/design-resources/dev-kits/igloo/igloo-plus-starter-kit#documents

Support

Technical support is available online at www.microsemi.com/soc/support and by email at soc_tech@microsemi.com

Microsemi sales offices, including representatives and distributors, are located worldwide.
To find your local representative, go to www.microsemi.com/salescontacts

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