

Board-Level Considerations for Power-Up and Power-Down of RTAX-S/SL FPGAs

Table of Contents

Introduction	1
Overview	1
Characterization	2
VCCDA Ramp-Down Rate Effects On Transient Current	10
Maximum Core Current Spike	12
Reliability Analysis	13
Summary	16
Power Supply Recommendations	16
Conclusion	17
List of Changes	17

Introduction

The high performance RTAX-S/SL devices by Microsemi are designed to be tolerant of any power-up or power-down sequence. While this offers flexibility for the power supply design, designers need to be aware of several other factors, such as power supply sizing, appropriate point-of-load (PoL) DC/DC converters, ramp rates, and clean monotonic ramp-up and ramp-down of the various supplies. In general there is no power-up or power-down requirement for RTAX-S/SL devices but a spike in ICCA current is observed only at power-down when VCCDA powers down before VCCA. Data analysis indicates that the amplitude and duration of this ICCA transient depends on power supply ramp-down rates, junction temperature, and the specific RTAX-S/SL device type.

Even though this current spike does not affect reliability of RTAX-S/SL devices, designers may wish to eliminate or minimize this transient on their board by ensuring that the power supply is capable of supplying the required current. Microsemi has conducted a series of experiments and characterized power-up and power-down phenomena, identified cases where the transient load currents may occur, and provided some recommendations on how to eliminate the transient.

Details on the RTAX-S/SL power supplies are covered in several sections of the [RTAX-S/SL RadTolerant FPGAs](#) datasheet.

Overview

This application note is separated into three sections:

- **"Characterization"** – Reproduce and observe the relationship between transient current and other variables, such as voltage level, die size, ramp rates, and temperature.
- **"Reliability Analysis"** – Isolate location(s) of transient current on the die and consider the impact on reliability.
- **"Summary"** and **"Power Supply Recommendations"**.

Characterization

Power-Up Characterization

Power supplies for the RTAX-S/SL devices can power up in any sequence. Figure 1 and Figure 2 show the power-up characteristics for the different sequencing between VCCA (1.5 V) and VCCDA/VCCIBx (3.3 V). No significant transient current (>5 mA) is observed with either sequence.

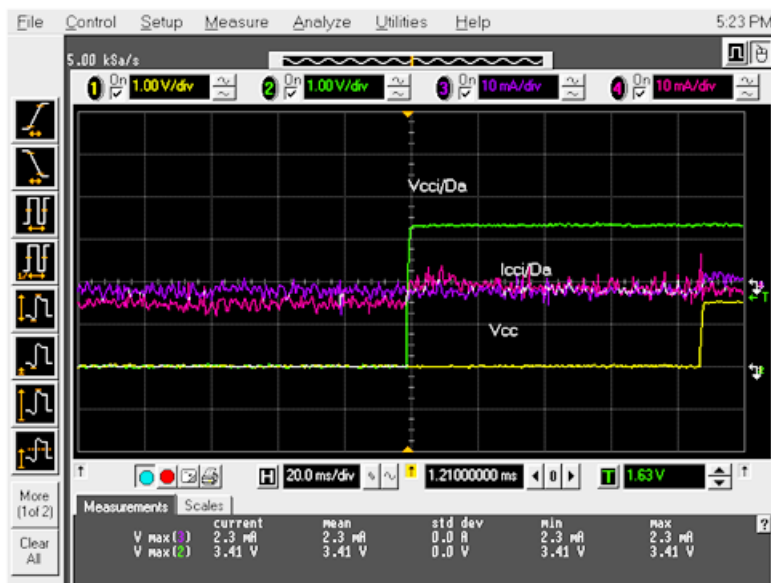


Figure 1 • Power-Up (VCCIBx + VCCDA → VCCA)

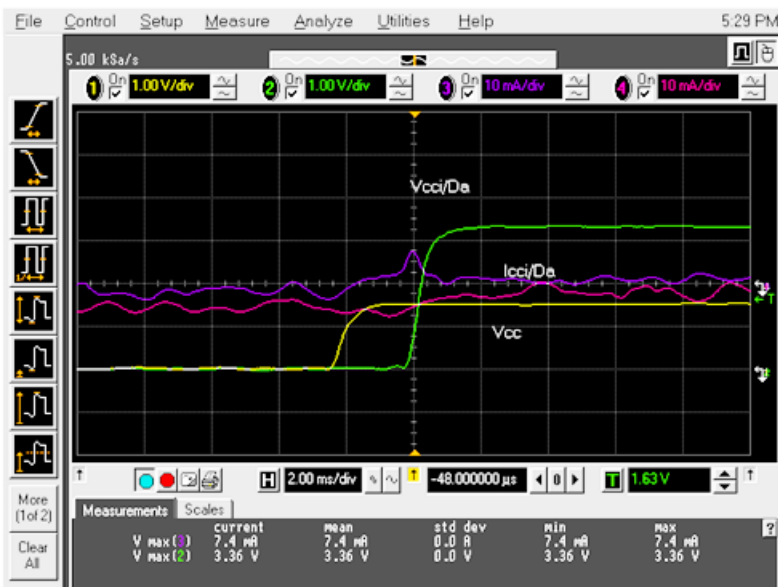


Figure 2 • Power-Up (VCCA → VCCIBx + VCCDA)

Microsemi recommends the use of best practices for powering up a system by terminating the inputs or configuring them with pull-up or pull-downs so that no I/Os are floating at any given time.

Power-Down Characterization

While there is no exact sequencing required to power-down the various supplies of the RTAX-S/SL devices, this section covers the impact of each supply power-down on core or I/O currents. [Figure 3](#) to [Figure 5](#) on [page 4](#) show the power-down characteristics for the different sequencing between VCCA (1.5 V) and VCCDA/VCCIBx (3.3 V).

- In [Figure 3](#), no transient current is observed when VCCA is powered down to 0 V before VCCDA/VCCIBx.
- [Figure 4](#) shows ICCA transient current when VCCDA/VCCIBx is powered down before VCCA.
- [Figure 5](#) on [page 4](#) shows a similar transient on ICCA when only VCCDA is powered down first.

This set of experiments demonstrates that VCCDA is the cause of the transient current.

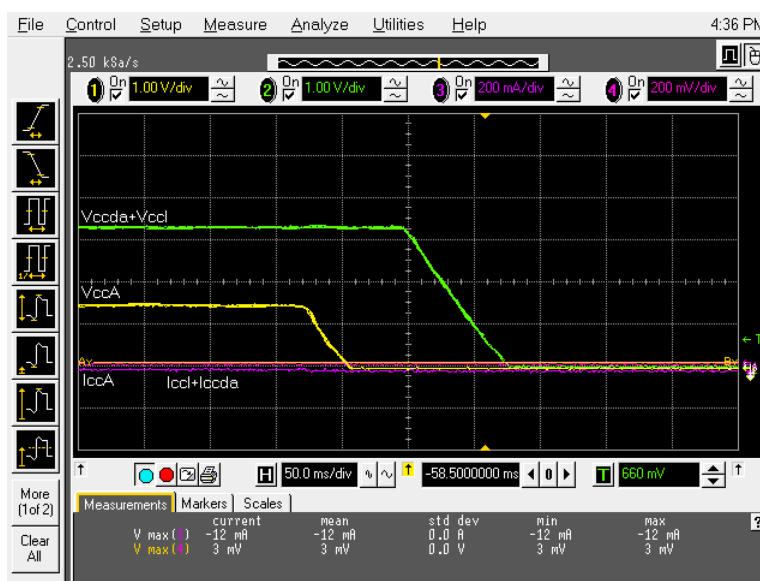


Figure 3 • Power-Down VCCA Before VCCABX + VCCDA

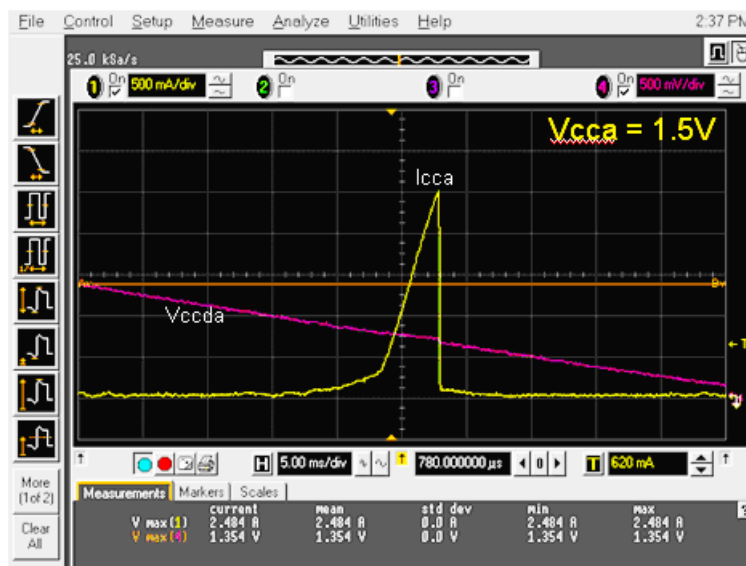


Figure 4 • Power-Down VCCIBx + VCCDA Before VCCA

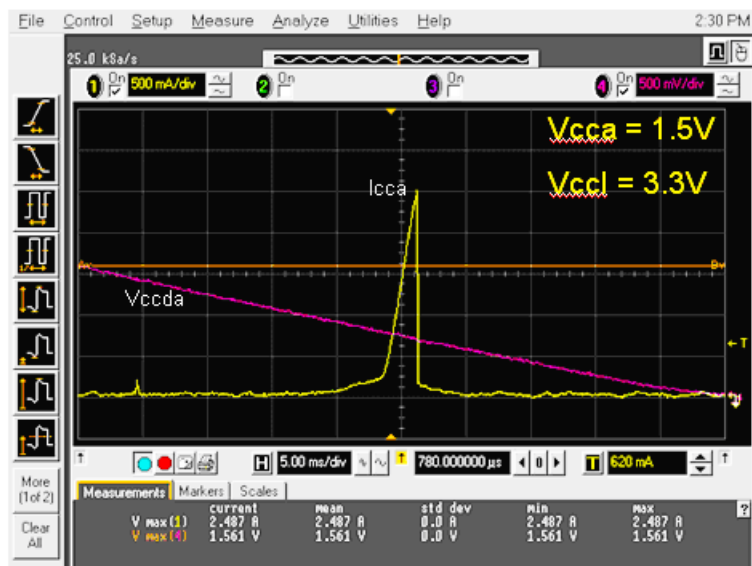


Figure 5 • Power-Down VCCDA Before VCCA + VCCIBx

If during power-down, VCCA is powered down before or at the same time as the power-down of VCCDA, no transient core is observed (Figure 1 on page 2). However, if VCCDA ramps down while the core supply VCCA continues to be ON, a transient core current may occur for a period of time that depends on the ramp-down rate of VCCDA and the level of VCCA. Experiments varying the value of the core supply voltage from 1.8 V down to 0.8 V while powering down VCCDA were performed and the results are summarized. Figure 6 through Figure 9 on page 6 show the characteristics of the ICCA transient current when powering down VCCDA while VCCA is at various levels (from 0.83 V to 1.5 V).

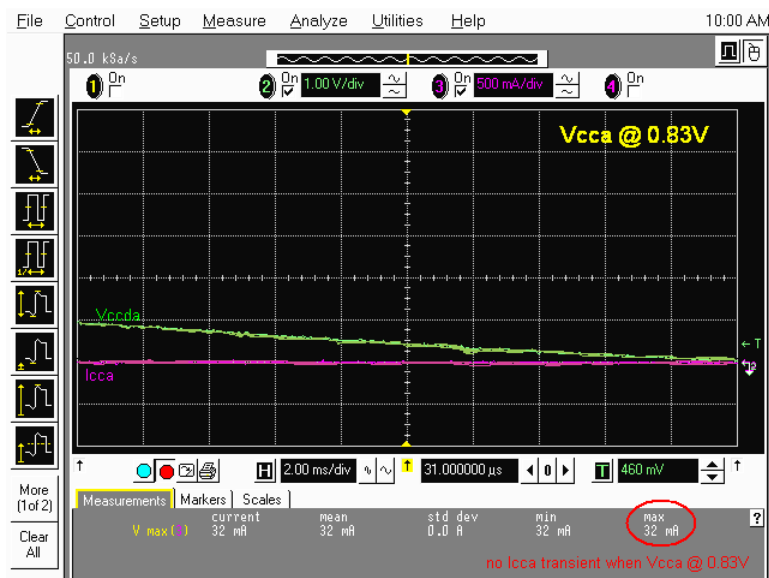


Figure 6 • Power-Down VCCDA with VCCA at 0.83 V

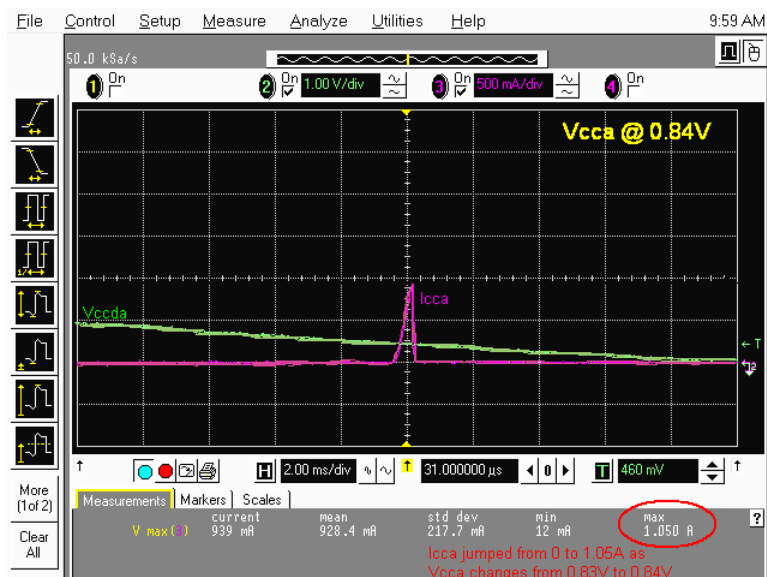


Figure 7 • Power-Down VCCDA with VCCA at 0.84 V

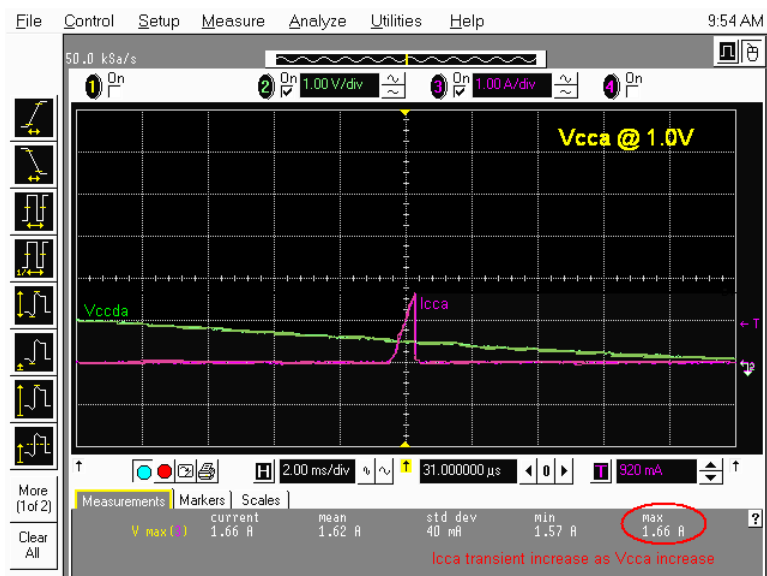


Figure 8 • Power-Down VCCDA with VCCA at 1.0 V

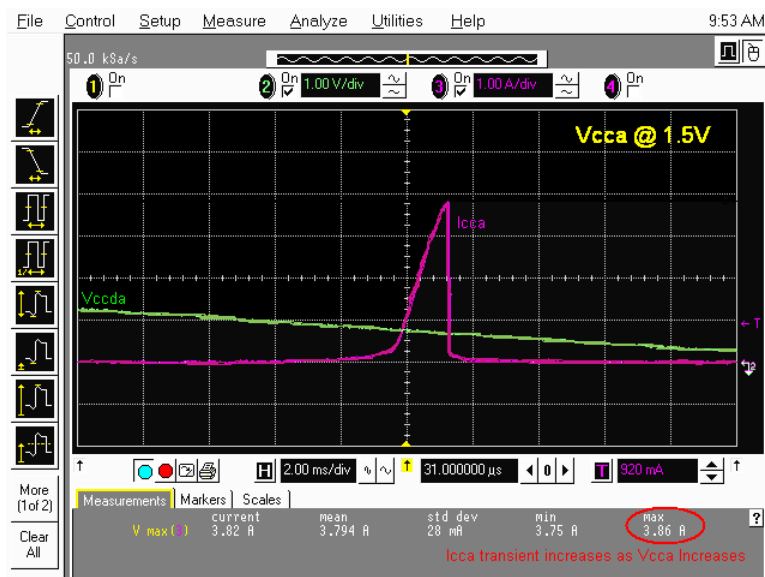


Figure 9 • Power-Down VCCDA with VCCA at 1.5 V

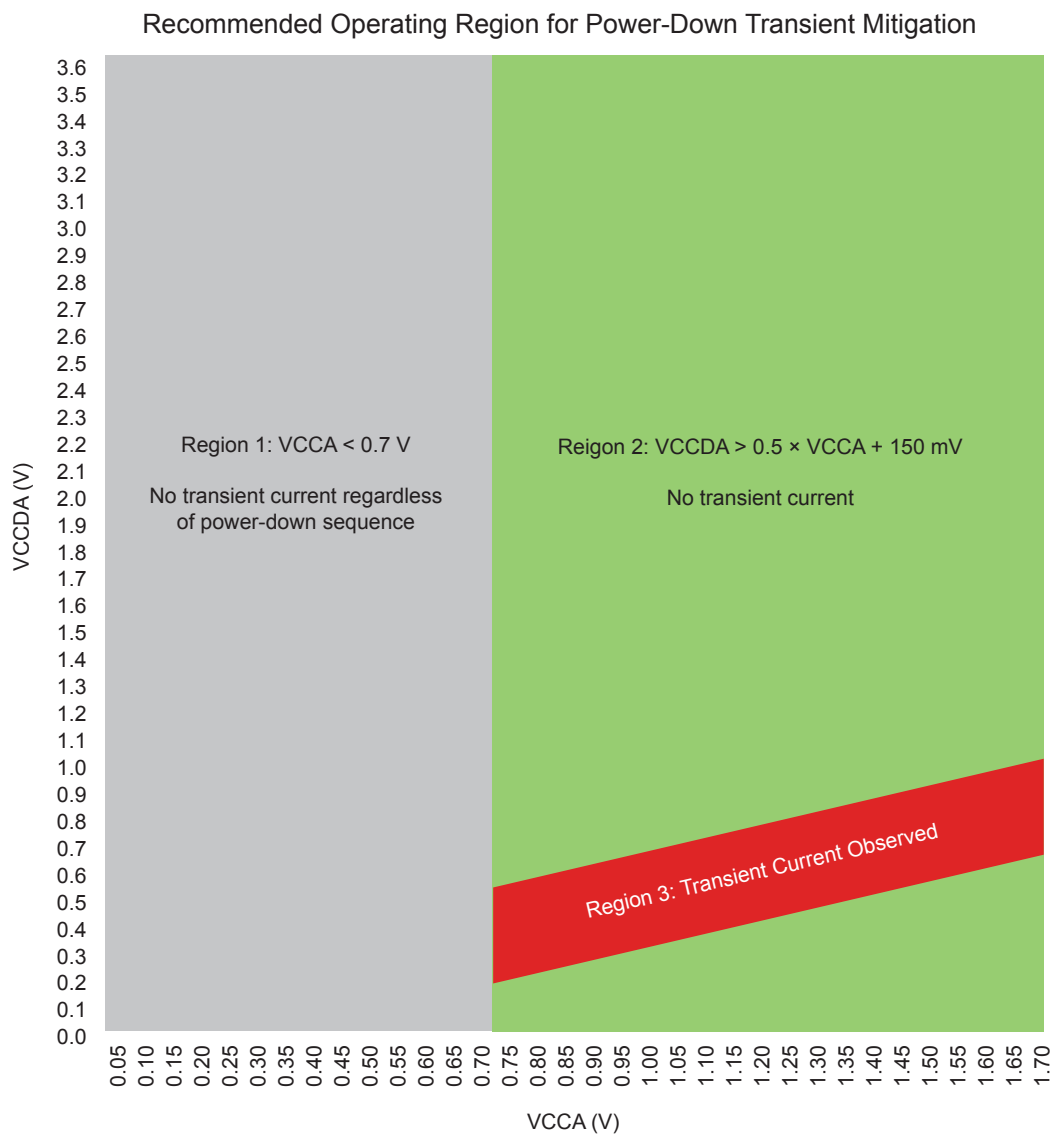
The following three statements can be made based on the results above:

1. Higher VCCA level induces a larger ICCA transient.
2. The VCCDA threshold that induces ICCA transient changes based on VCCA level. This threshold follows the approximate relationship: $VCCDA = 0.5 \times VCCA$.
 - If $0.5 \times VCCA - 150 \text{ mV} = VCCDA = 0.5 \times VCCA + 150 \text{ mV}$, then a transient core current is observed. The amplitude and the duration of this current depends on the ramp-down rate of VCCDA and the actual value of the core supply.

There is no core current spike outside the range above.

- In other words, if $VCCDA > 0.5 \times VCCA + 150 \text{ mV}$ or $VCCDA < 0.5 \times VCCA - 150 \text{ mV}$ while $VCCA > 0.7 \text{ V}$, then there is no transient current observed.
3. When $VCCA < 0.84 \text{ V}$ (at 25°C), transient on ICCA is no longer observed. To be conservative and account for all temperature effects, $VCCA < 0.7 \text{ V}$ is used.

The conclusions above are illustrated [Figure 10 on page 7](#) where the critical region, called Region 3, is depicted in red. This curve covers all temperature ranges.



Note: Region 3 Equation: $0.5 \times V_{CCA} - 150 \text{ mV} = V_{CCDA} = 0.5 \times V_{CCA} + 150 \text{ mV}$

Figure 10 • Operating Regions for Power-Down Sequencing for all Temperature Conditions

Brown-Out and Power-Up Voltages

Brown-Out Voltages

Brown-out is a condition where a power supply dips below the recommended operating conditions. Microsemi cannot guarantee proper functionality of devices operating outside the recommended operating conditions. The following table indicates the voltage level at which functionality ceased for each power supply. The data in [Table 1](#) is collected at the room temperature.

Table 1 • Brownout Voltage for Power Supplies

Supply	Brownout Point (V)
VCCA	0.91
VCCI	0.84
VCCDA	1.46

Power-Up Voltages

The I/Os are tristated during power-up. At the following power-up voltages, RTAX-S I/Os go from tristated to functional state:

- VCCA = 0.99 V
- VCCI = 0.84 V
- VCCDA = 1.5 V

These power-up voltage can vary slightly with the Power Supply Ramp Rates.

Die Size Versus Transient Current

The ICCA transient current is characterized across all die types in the RTAX-S/SL family. Figure 11 shows a summary of the results with the RTAX4000S device showing the higher peak transient current. The data indicates that the larger die size results in higher peak transient. However, the current magnitude does not scale proportionally with die size. This is further discussed in the "Reliability Analysis" section on page 13.

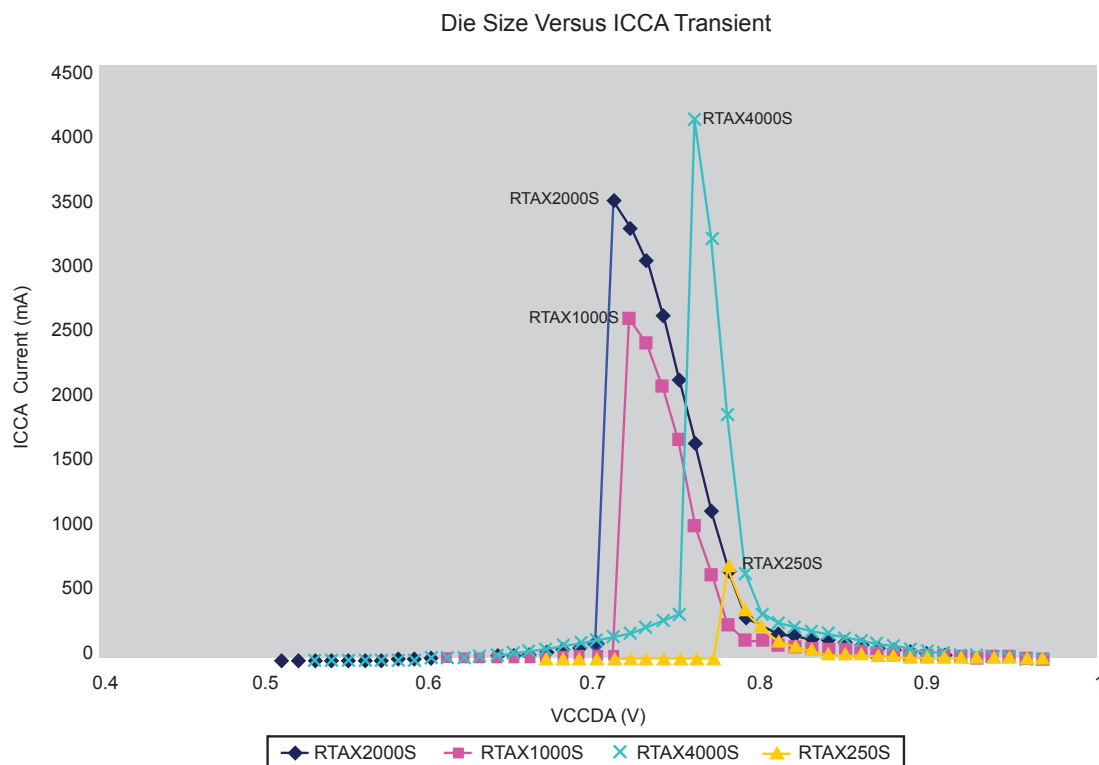


Figure 11 • Power-Down VCCDA with VCCA at 1.5 V and 25°C

VCCDA Ramp-Down Rate Effects On Transient Current

Since ramp-down rates vary greatly depending on current drive and board capacitance, it is important to understand the effects of the VCCDA ramp rate on the ICCA transient. Table 2 summarizes this effect for various ramp-down rates across the RTAX250S/1000S/2000S die types. From the collected silicon data, the following conclusions can be made:

- For a faster VCCDA ramp-down rate, the current surge amplitude is lower and the duration is shorter.
- The VCCDA ramp-down rate has more of an impact on the duration of the current spike than it has on the amplitude.
- For a given VCCDA ramp-down rate, larger dies have larger amplitude and duration of current spikes

Table 2 • Effect of Ramp-Down Time on Transient

VCCDA (90% to 10%) Ramp-Down Rate (ms)	ICCA Transient (A)			ICCA Pulse Width (μs)		
	RTAX2000S	RTAX1000S	RTAX250S	RTAX2000S	RTAX1000S	RTAX250S
0.1	1.98	1.73	0.99	9	8	7
0.5	2.65	1.87	1.08	14	13	11
1.0	2.45	1.90	0.89	35	36	16
10.0	2.78	1.97	1.18	141	170	75
50.0	3.93	2.18	1.15	1120	600	300

While the width of the ICCA transient pulse follows the general trend of wider pulse as ramp rate becomes slower, the peak magnitude of the transient tends to saturate when the ramp rate slows beyond a certain point. This effect can be seen from Figure 12, where the ICCA transient saturates as the ramp-down rate approaches 50 ms. Based on this trend, approximately constant magnitude of ICCA transient current is expected when the ramp-down rate is greater than 50 ms.

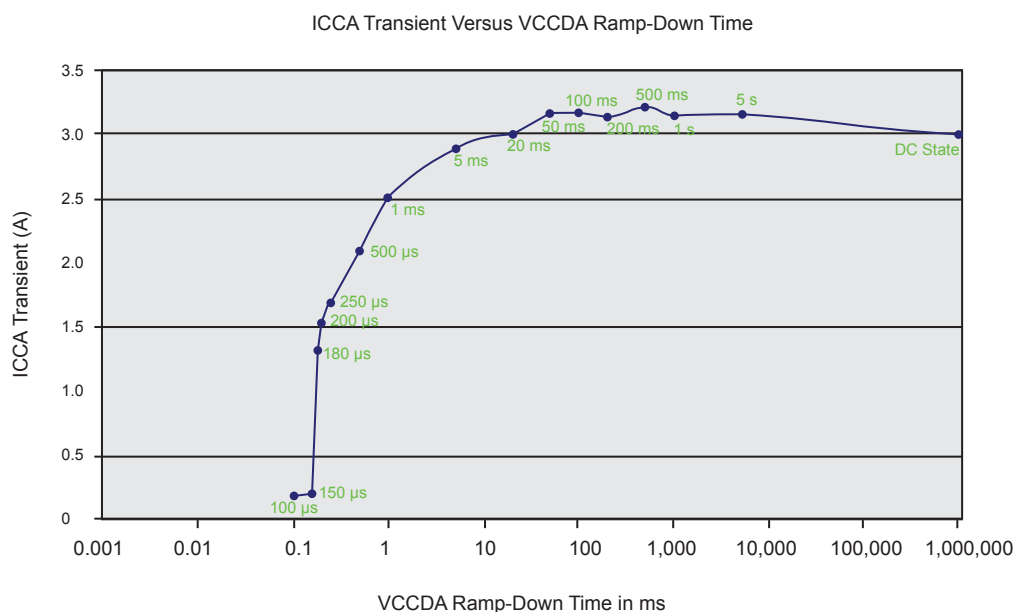


Figure 12 • ICCA Transient Versus VCCDA Ramp-Down Time (Subject to ± 5% Measurement Error)

Temperature Effects On Transient Current

Since most of the applications for RTAXS/SL devices require operating between -55°C and 125°C , it is important to understand the temperature effects on the ICCA transient. Table 3 summarizes the peak ICCA transient observed at $-55^{\circ}\text{C}/25^{\circ}\text{C}/125^{\circ}\text{C}$ across all the RTAXS/SL die types. Based on the data below, -55°C results in the highest ICCA transient current. The transient decreases with increasing temperature.

Table 3 • Temperature vs. Peak ICCA Transient (Ramp-down Rate at 45 ms)

RTAX250S	Peak ICCA Transient (A) at Temperature		
DUT	-55°C	25°C	125°C
Sample 1	2.26	2.06	1.94
Sample 2	2.14	1.86	1.72
RTAX1000S	Peak ICCA Transient (A) at Temperature		
DUT	-55°C	25°C	125°C
Sample 1	3.43	2.99	2.82
Sample 2	3.41	2.95	2.80
RTAX2000S	Peak ICCA Transient (A) at Temperature		
DUT	-55°C	25°C	125°C
Sample 1	4.04	3.68	3.30
Sample 2	3.22	2.90	2.63
RTAX4000S	Peak ICCA Transient (A) at Temperature		
DUT	-55°C	25°C	125°C
Sample 1	4.39	4.14	3.99
Sample 2	4.58	4.34	4.28

The following conclusions can be made based on the data above:

1. The current surge has its highest amplitude at the lowest temperature and it decreases as temperature increases.
2. Larger dies show higher amplitude for the transient current. However, the peak current increase does not correlate with the die size increase. Refer to the ["Maximum Core Current Spike" section on page 12](#) for more information.

Maximum Core Current Spike

Table 4 shows the expected absolute maximum ICCA transient current under the worst case conditions (defined below) across the different die sizes and temperature range when operating in region 3 (Figure 15 on page 15). This table is based on extrapolation from the existing data and makes the following assumptions for worst case conditions:

- VCCA = 1.7 V (maximum DC condition per datasheet)
- VCCDA ramp-down rate = 50 ms (ICCA transient saturates beyond 50 ms per Figure 12 on page 10)
- To be conservative, an additional margin of approximately 10% is added to the worst case extrapolated values.

Table 4 • Expected Absolute Maximum ICCA Transient Current

Die Type	Absolute Maximum ICCA Transient (A) (= 50 ms Ramp-down and VCCA at 1.7 V)		
	–55°C	25°C	125°C
RTAX250S	3.0	2.7	2.5
RTAX1000S	4.5	3.9	3.7
RTAX2000S	5.3	4.8	4.3
RTAX4000S	6.0	5.7	5.6

Extensive power-down characterization has revealed that there is no power-down sequence required and that in one unique scenario of the device power-down a transient core current spike may occur if VCCDA powers down before VCCA. This scenario is characterized by the following two conditions:

- $VCCA > 0.7 \text{ V}$
- $0.5 VCCA - 150 \text{ mV} = VCCDA = 0.5 VCCA + 150 \text{ mV}$

Outside the critical ranges of VCCA and VCCDA above, no transient current is observed. In an effort to bound the amplitude and the duration of this core current surge, repeated experiments checking the impact of the temperature, ramp-down rate, actual values of the supply voltages have been carried out. The conclusions derived from the silicon measurements are as follows:

- Amplitude of the transient core current depends on the VCCA value. Lower VCCA values result in lower transient spikes.
- Larger transients with longer durations are observed at low temperatures.
- The amplitude and duration of the current surge increase with slower ramp-down of VCCDA. However, beyond 50 ms ramp-down time, the peak amplitude of the transient current saturates and does not increase.

Reliability Analysis

Liquid Crystal¹ Analysis

To isolate the location(s) of the ICCA transient, an RTAX2000S device was de-capped to perform liquid crystal. This technique involves spreading a thin layer of liquid crystal on the die. Upon triggering a high current event, the location(s) with the highest current density heats up and aligns the scattered crystals, which manifest as hot spots.

Figure 13 shows a simplified view of the RTAX2000S/SL die, which is made up of 16 tiles. The hot spots observed are located on the tile periphery. These repetitive hot spots correlate to a common circuit called ml_buf (refer to the "Layout and Schematic Analysis" section for more information).

Note: No hot spot was observed inside the tile where the array logic, routing, and antifuses reside. This phenomenon is independent of the design programmed into the device because the hot spots are located in the common circuitry instead of specific regions where the logic array or routing tracks might be used, depending on the design.

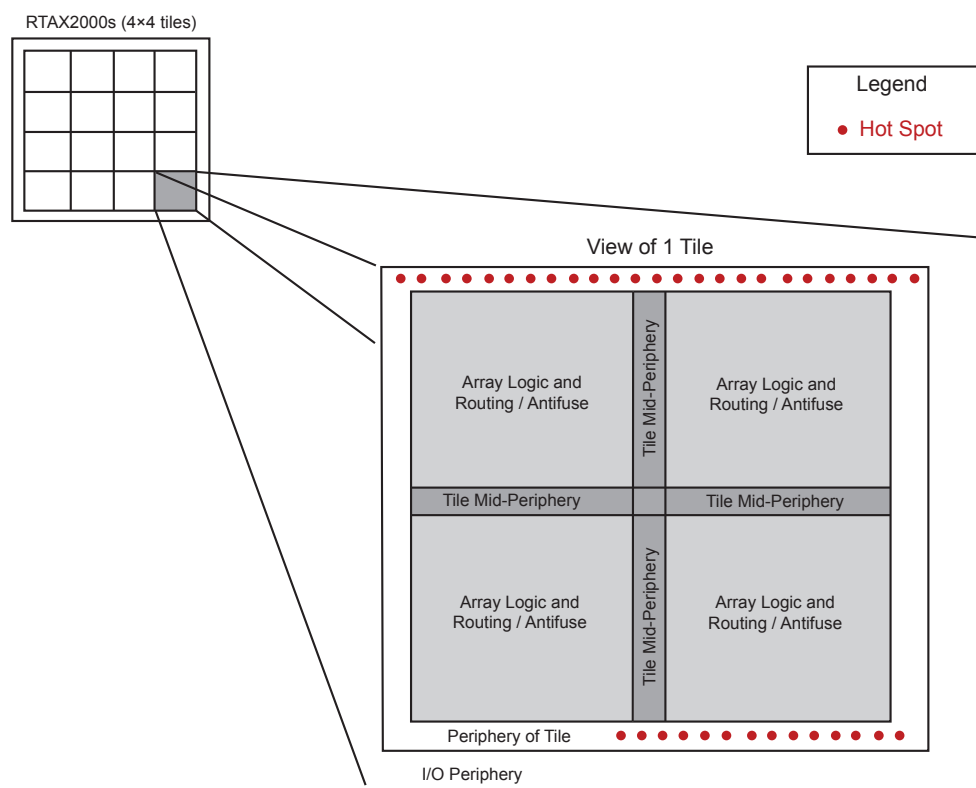


Figure 13 • Simplified Layout of an RTAXS/SL Tile and Observed Hot Spots

1. Liquid crystal is a well known technique involving the spread of a thin layer of liquid crystal on the die. It is used to locate the areas of high current density by showing these areas as hot spots.

Layout and Schematic Analysis

As indicated in the "Liquid Crystal Analysis" section on page 13, the hot spot locations correlate to the ml_buf circuit. Figure 13 shows a simplified schematic of the ml_buf. The purpose of this buffer is to act as a level shifter between VCCDA and VCCA. This buffer is biased by VCCA while driven by VCCDA at the input. When VCCA is at nominal level and VCCDA powers down, the input reaches a threshold level where both the P-channel and N-channel transistors of the first stage are turned on. This creates a resistive short path between VCCA to GND. Any subsequent stages driven by the buffer will experience the same phenomenon but for a shorter period of time, hence reducing the totem-pole effect.

Since the transient current is restricted to the resistive short path within these ml_buf circuits, there are no reliability concerns for the array logic, routing, and antifuses area. Furthermore, ml_buf controls the amount of current flowing through the resistive short path to a level below the I_{dsat} value. This is related to the HCI issue that will be discussed in the "Other Reliability Considerations" section on page 15.

Although the analysis above shows no direct reliability concerns in the ml_buf circuit, there are other secondary effects that should be considered when looking at the overall reliability impact. These effects will be further discussed in the "Other Reliability Considerations" section on page 15.

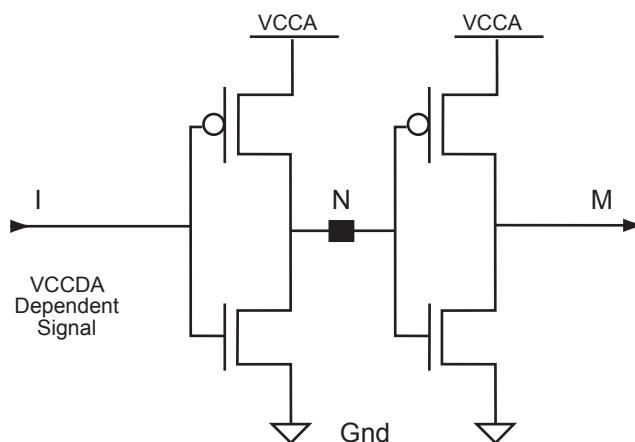


Figure 14 • Simplified Schematic of ml_buf

Spice Simulation Correlation

Spice simulation on the ml_buf circuit was performed to correlate with the data collected on bench. Figure 15 on page 15 shows the spice simulation results of the ml_buf circuit (refer to Figure 14 for the node names). The following conclusions can be made based on the simulation results:

- Peak transient current occurs when $VCCDA = \sim 0.7\text{ V}$, which is consistent with the $0.5 \times VCCA$ threshold value observed.
- The rise/fall time at the output of the first stage (node N) is much slower than the second stage (node M). This confirms the previous assumption that subsequent circuits driven by ml_buf will see negligible totem-pole effect.
- The first stage inverter draws much less current ($\sim 110\text{ }\mu\text{A}$) compared to the second stage inverter ($\sim 6\text{ mA}$). This can be attributed to the fact that the first stage inverter is made up of high voltage transistors (3.3 V) while the second stage inverter is made up of low voltage transistors (1.5 V).

- Multiplying the peak current of individual ml_buf with the number of instances results in a much higher current than bench observation. This discrepancy is due to the fact that not all ml_buf in the die reach the totem-pole threshold simultaneously because of an IR drop effect across the die. This correlates with Figure 11 on page 9, which shows the peak transient is not directly proportional to the die size.

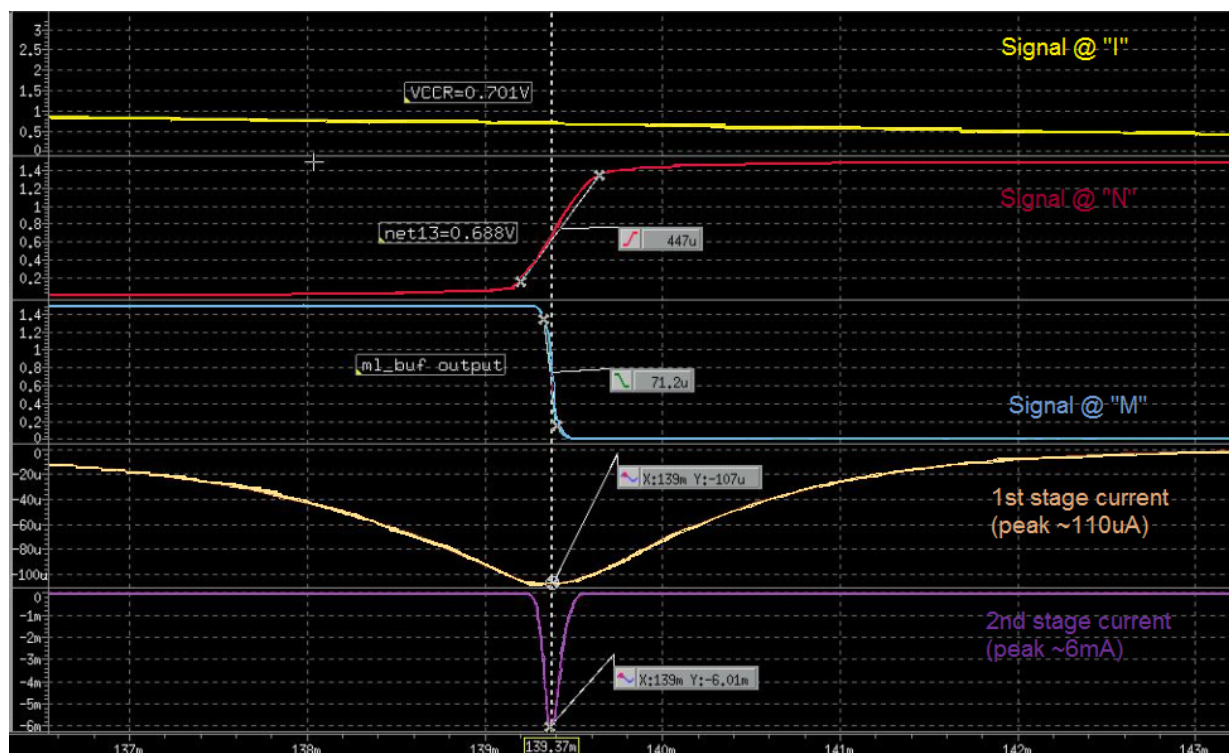


Figure 15 • Spice Simulation Results of ml_buf

Other Reliability Considerations

The following section discusses the secondary effects from the transient current that should be considered for a more thorough reliability impact analysis.

Temperature Increase and Impact

Considering the worst case of a maximum current of 4 A leads to a power dissipation of 6 W with duration in milliseconds range during device power-down. Due to the thermal mass of the die and the distributed nature of the current, the temperature could only increase a fraction of a degree. Therefore temperature related failures are not a concern.

Hot Carrier Injection (HCI)

HCI is an issue for currents at the maximum VCCA across the transistor creating hot carriers that get trapped in the oxide. In this case, the voltage is divided equally across the P-Channel and N-Channel transistors or what is often called totem-pole current, such that the effective voltage across the transistors is only half of VCCA; that is, approximately 0.75 V. At this voltage HCI is minimal. The peak current of 60 and 120 $\mu\text{A}/\mu\text{m}$ of width of the transistor is below the normal drain saturation current of 500 $\mu\text{A}/\mu\text{m}$ seen during high speed operation. Therefore, HCI is not a concern in this case.

Electro-Migration (EM)

While the local currents are low, the distributed nature of the current means that a substantial current collects on the major power buses. RTAX-S/SL devices were designed to withstand large current spikes when major portions of the core are switching at very fast rates. Voltage Storm simulations show that the RTAX2000S power buses can withstand a core current of 7 A for 20 years at a junction temperature of 125°C. Since this is almost double the worst amplitude of the short term transient spike, electro-migration is not a concern.

Summary

Following is a summary of the observations and conclusions made in the previous sections:

- No transient current is observed during power-up because RTAXS/SL devices have an internal power-up sequencing circuit that gates the VCCDA dependent signals. Hence these VCCDA dependent signals do not ramp up until the chip is fully powered.
- ICCA transient only occurs when VCCDA powers down before VCCA and reaches the region near $VCCDA = 0.5 \times VCCA$.
- Higher VCCA level results in higher transient current.
- Transient current is eliminated, if $VCCA < 0.83 \text{ V}$ (at 25°C), regardless if VCCDA powers down first. To be conservative and account for all temperature effects, $VCCA < 0.7 \text{ V}$ should be used.
- Larger dies have higher peak transients; however, the magnitude of the transient does not scale proportionally based on the die size due to an IR drop effect.
- Slower ramp-down rates on VCCDA results in higher peak transient and larger pulse width. However, the peak transient saturates as it approaches ramp-rates $> 50 \text{ ms}$, as shown in the ["VCCDA Ramp-Down Rate Effects On Transient Current" section on page 10](#).
- Peak transient current is highest at -55°C and decreases as temperature increases.
- Hot spots observed on the tile periphery correlate to the ml_buf circuit, which acts as a level shifter between VCCDA (3.3 V or 2.5 V) and VCCA (1.5 V).
- Resistive short path created in ml_buf as the VCCDA dependent input approaches $0.5 \times VCCA$ level.
- There are no reliability concerns, since transient current is distributed across the die instead of a localized spot. This current flows through the resistive short path inside ml_buf, so areas containing the array logic, routing and antifuses will not have any reliability issues.
- Analysis on the secondary effects such as temperature increase, HCI, and EM showed no reliability concerns.
- Based on the above analysis, there are no reliability concerns even under DC conditions where VCCDA and VCCA are at worst case levels resulting in maximum ICCA.

Power Supply Recommendations

1. Tie VCCDA to highest VCCIBx (refer to the [RTAX-S/SL RadTolerant FPGAs](#) datasheet, Table 2-2 and page 2-11 under the VCCDA description)
2. To prevent this transient spike condition, always power-down VCCA before VCCDA.
3. For instances where VCCDA needs to power-down before VCCA, the transient current spike can be avoided if the following are true:
 - $VCCA < 0.7 \text{ V}$
 - $VCCDA > 0.5 \times VCCA + 150 \text{ mV}$ (where $VCCA \geq 0.7 \text{ V}$)
 - $VCCDA < 0.5 \times VCCA - 150 \text{ mV}$ (where $VCCA \geq 0.7 \text{ V}$)

Conclusion

The high-speed RTAX-S/SL devices do not require any power-up or power-down sequencing in order to allow easy and flexible board power supply designs. In general there is no power-up or power-down requirement for RTAX-S/SL devices, but a spike in ICCA current is observed only at power-down when VCCDA powers down before VCCA. Data analysis indicates that the amplitude and duration of this ICCA transient depends on power supply ramp-down rates, junction temperature, and the specific RTAX-S/SL device type. Thorough analysis indicates no reliability concerns for RTAX-S/SL devices. In the event that it is not possible to arrange sequencing of the power supplies to avoid transient current spike, Microsemi encourages customers to ensure that the power supply components are capable of supplying the required current.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 1 (November 2012)	The "Brown-Out and Power-Up Voltages" section was revised (SAR 27392 and SAR 31946).	8

Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.



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