Assembly and PCB Layout Guidelines for QFN Packages

Introduction

The dual-row or multi-row QFN package is a near Chip Scale, plastic-encapsulated package with a copper leadframe substrate. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB and provides a stable ground through down bonds or by electrical connections through conductive die attach material. The design of dual-row and multi-row QFN packages allows for flexibility and enhances electrical performance to very high-speed operating frequencies.

The dual-row or multi-row QFN package utilizes an interstitial lead design that results in a staggered lead arrangement. The inner row is offset 0.5 mm, which results in a compact design that maximizes die size while not exceeding the surface mount technology (SMT) capability of a typical 0.5 mm pitch SMT process.

Actel offers QFN packages in three configurations: QN180, QN132, and QN108. The package footprint and outlines are covered under JEDEC MO-247: Plastic Quad No-lead Staggered Multi-Row Packages (with Optional Thermal Enhancements) and JEDEC Design Guide 4.19: Quad No-lead Staggered Multi-Row Packages.

QFN Package Overview

Figure 1 and Figure 2 show that the package height is minimized by having both the die and wirebond pad on the same plane. Figure 3 on page 2 illustrates the detail construction of the land pad. When mounted, the leads are directly attached to the board without the space-consuming standoff inherent in a leaded package such as a Plastic Quad (PQ) or Thin Quad (TQ). In addition, the QFN package has excellent thermal dissipation, with the die attach paddle attaching directly to the PCB. The QFN package also reduces electrical parasitics due to its efficient and compact design.

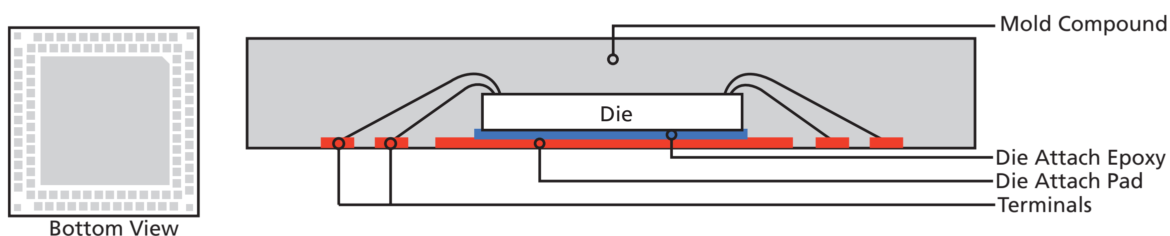

Figure 1 • **Bottom View and Cross Section of Dual-Row QFN**

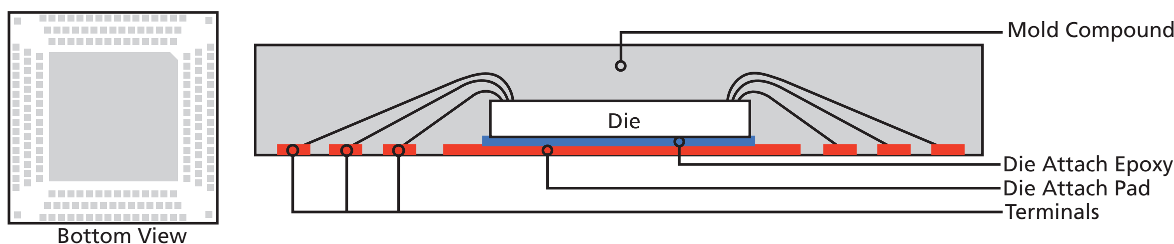

Figure 2 • **Bottom View and Cross Section of Three-Row QFN**

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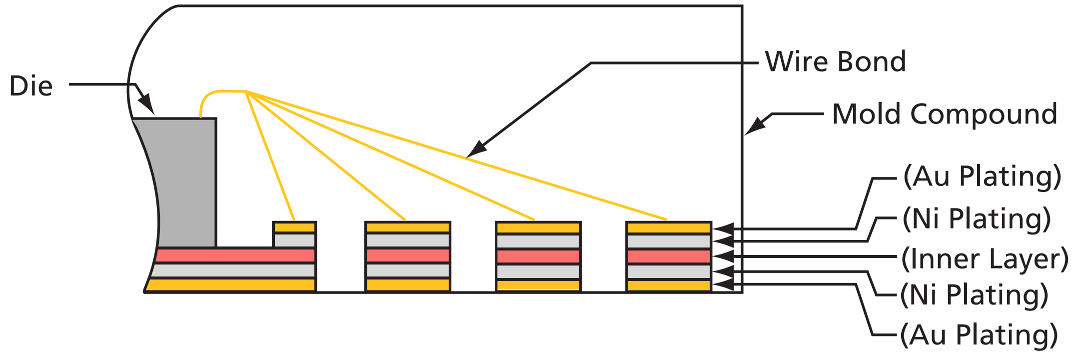

Figure 3 • **Detail Construction of Land Pad**

Table 1 shows typical reliability data.

Table 1 • **Reliability**

Test	**Result**
Moisture Sensitivity	MSL-3
Autoclave, 121°C	168 hours
Temperature Cycle, Condition C	250/1,000 cycles
Unbiased HAST, 130°C	96 hours
HTSL, 150°C	1,000 hours
Second Level, 0/1000°C	6,000 cycles failure free
Vibration Test	IPC-TM-650 Method 2.6.9
Drop Test (free fall)	IEC-68-2-32 Part 2

In order to obtain peak performance, the motherboard must be properly designed and the package mounted with special consideration. For enhanced thermal, electrical, and board-level performance, the exposed pad on the package must be soldered to the board using a corresponding thermal pad on the board. For proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region. Clearance between the inner row's leads and the thermal pad are required for vias to route the inner row signals. The amount of clearance required depends on the application. The PCB footprint design must be considered, taking into account the dimensional tolerance due to package, PCB, and board assembly.

Some of the factors that can significantly affect the mounting of the QFN package on the board and the quality of the solder joints are listed here:

- Amount of solder paste coverage in the thermal pad region
- Stencil design for peripheral and thermal pad region
- Type of vias
- Board thickness
- Lead finish on the package
- Surface finish on the board
- Type of solder pasted
- Reflow profile

This application note provides general guidelines for developing the proper board design and the surface mount process. Further study and development effort may be needed to optimize the process for a particular user's surface mount practices and requirements.

PCB Land Pad Design Guideline

This section addresses both package-level and board-level routing constraints in describing the rationale behind the recommended land pad patterns.

Three-Row QFN PCB Land Pad Design (QN132 and QN180)

Normally, the size of the thermal pad should at least match the exposed die paddle size. Due to needed clearance for vias, the thermal pad size may need to be reduced to less than the package paddle size. From a board mounting perspective, no issues have been seen when the board thermal pad is smaller than the package paddle size. Thermal pads as small as 80% of the paddle size have been mounted successfully without issue. From a thermal efficiency perspective, there is minimal efficiency loss as long as the thermal pad on the board is at least the same size as the die inside the package.

Board design rules assumptions are for a standard four-layer board using one-half ounce of copper. These assumptions were made to determine via spacing requirements. Figure 5 on page 4 and Figure 6 on page 4 give the values used in the analysis. See "Appendix I: Detailed PCB Layout" on page 11 for more information.

Special attention must be given to the traces connecting to the metal pads on the board. Trace cracking has been observed during board-level drop and bend tests of this package. This trace cracking usually occurs at the edge of the solder mask opening around the metal pad. To avoid this mode of failure, Actel recommends that the trace under the solder mask edge should be made wider than the rest of the trace. This is shown in Figure 4. Depending on the reliability requirements, the wider part of the trace might need to be as wide as 50 to 75% of the metal pad width.

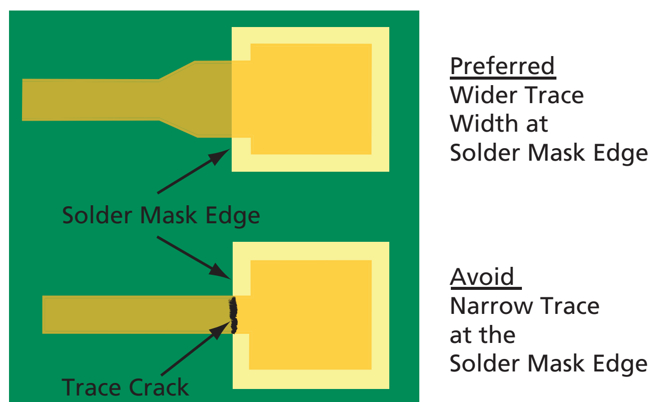

Figure 4 • **Wider Trace under Solder Mask Edge to Avoid Trace Cracking**

Option #1: Reduced Thermal Pad Design on Board

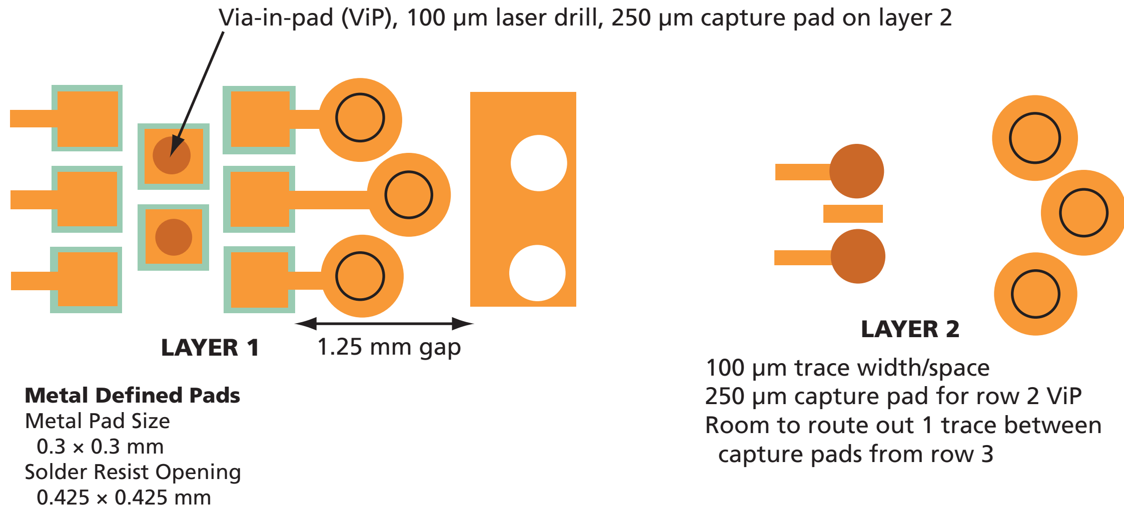

Figure 5 • **Reduced Thermal Pad Design on Board**

Option #2: Same Size Thermal Pad Design on Board

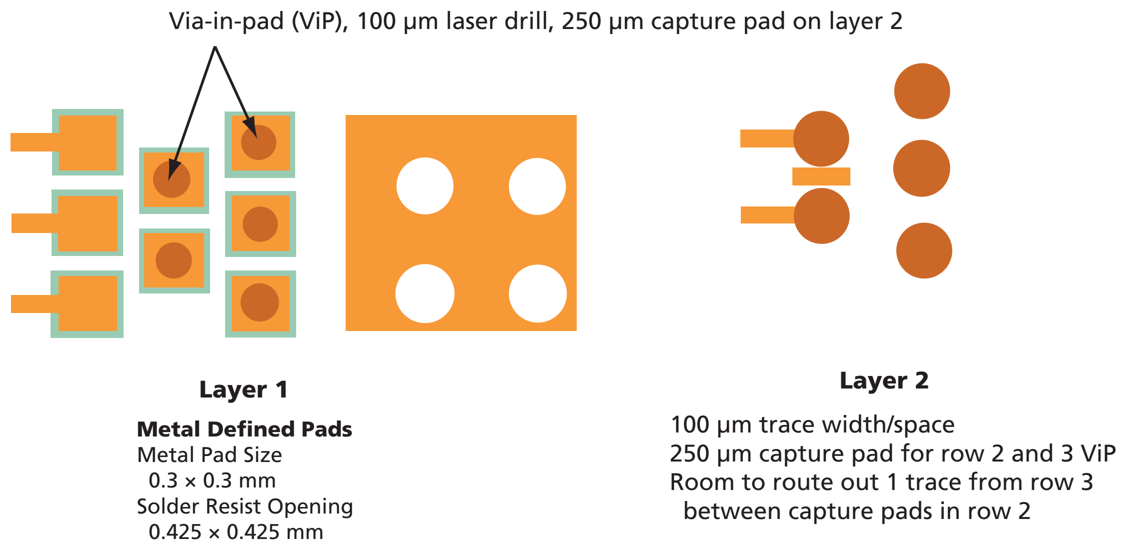

Figure 6 • **Same Size Thermal Pad Design on Board**

Thermal Pad Via Design

Dual-row and three-row QFN packages are designed to provide superior thermal performance. While a thermal pad provides a solderable surface on the top of the PCB (for soldering the package die paddle on the board), thermal vias are needed to provide a thermal path to inner and bottom layers of the PCB to remove the heat.

In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias must be incorporated into the thermal pad design. The number of thermal vias will depend on the application, power dissipation, and electrical requirements. Although more thermal vias improve the package's thermal performance, there is a point of diminishing returns where additional thermal vias may not significantly improve the performance. Based on information from subcontractors, Actel recommends incorporating an array of thermal vias at 1.0 mm to 1.2 mm pitch with via diameters of 0.3 mm to 0.33 mm. The number of vias must be determined for each application operating environment and condition.

One disadvantage of through-vias is that the solder tends to wick down the vias during the reflow process, thus reducing the solder standoff height for perimeter leads. This can be avoided by plugging or tenting the vias with the solder mask, which in turn results in voiding in the solder layer between the DAP and thermal pad (Figure 7, a)Through-Vias). Thus a compromise must be made between voiding and standoff height to determine the proper treatment for thermal vias. Although not as effective, heat transfer to inner layers can also be accomplished by using a mix of through-vias and micro-vias in the thermal pad region (Figure 7, b) Combination of Through- and Blind Micro-Vias).

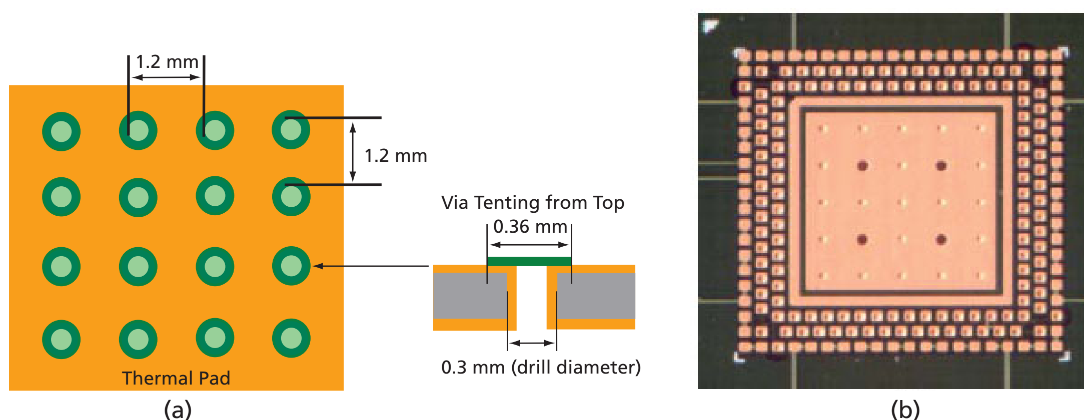

Figure 7 • **Thermal Via Options: a) Through-Vias; b) Combination of Through- and Blind Micro-Vias**

Solder Masking Consideration

Non-solder mask defined (NSMD) pads are recommended for dual-row and three-row QFN packages, since the copper etching process has tighter control than the solder masking process and improves the reliability of solder joints.

For the center thermal pad, a solder mask defined (SMD) structure is recommended.

Board Mounting Guidelines

Because of the small land surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for dual-row and three-row QFN packages. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the lands. Special considerations are needed in stencil design and paste printing for both perimeter lands and thermal pads. Since the surface mount process varies from company to company, careful process development is recommended. The "Stencil Design for Perimeter Lands and Thermal Pads" section provides some guidelines for stencil design based on Actel experience and information from subcontractors on the surface mounting of dual-row and three-row QFN packages.

Stencil Design for Perimeter Lands and Thermal Pads

The optimum and reliable solder joints on the perimeter pads should have about 50 to 70 µm (2 to 3 mils) standoff height. Stencils should be laser cut and electropolished. Polishing helps smooth the stencil walls, which results in better paste release. Actel recommends that the stencil aperture tolerance be tightly controlled, since these tolerances can effectively reduce the aperture size.

Board mounting studies on dual-row and three-row QFN packages have shown that standoff height is primarily determined by thermal pad paste coverage. The floating effects of the perimeter pads were minor and not a significant factor in determining standoff. It was also determined that not enough paste on the thermal pads could lead to inner row bridging due to the reduced standoff height. Area ratios and aspect ratios of 0.66 and 1.5, respectively, were never exceeded, to maintain proper stencil design.

- The land pattern on the PCB should be 1:1 to the land pads on QFN package.
- The thermal pad design on the PCB should have 75% paste coverage and use a hatch (Figure 8). The number of openings (D2' dimension) should be chosen such that A_H and A_W = 1.00 ± 0.15 mm. Maintaining a web thickness between openings of 0.200 mm will allow space for flux volatiles to escape, thus minimizing voids.

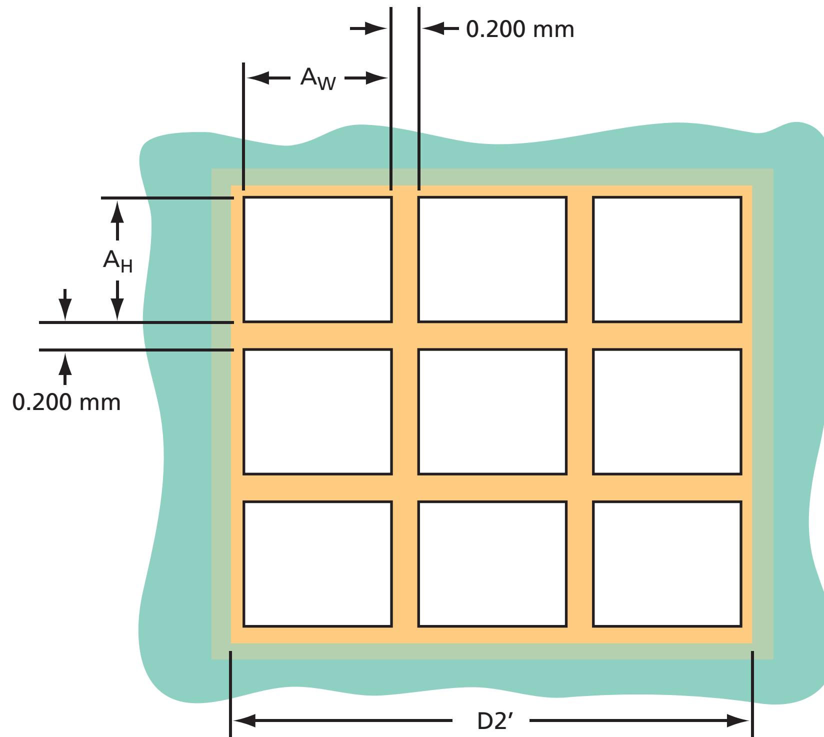

Figure 8 • **Thermal Pad Stencil Design**

Stencil Thickness and Solder Paste

The stencil thickness of 0.125 mm is recommended for 0.5 mm dual-row and three-row QFN parts. A laser-cut stainless steel stencil with electropolished trapezoidal walls is recommended to improve the paste release. Since not enough space is available underneath the part after reflow, Actel recommends that no-clean, Type 3 or Type 4 paste be used for mounting QFN packages. Nitrogen purge is also recommended during reflow.

Reflow Profile

Reflow profile and peak temperature have a strong influence on void formation. Actel strongly recommends that users follow the profile recommendation of the paste suppliers, since this is specific to the requirements of the flux formation. However, the following two profiles (Figure 9 and Figure 10) can serve as a reference for fine tuning the final profile that works for your application.

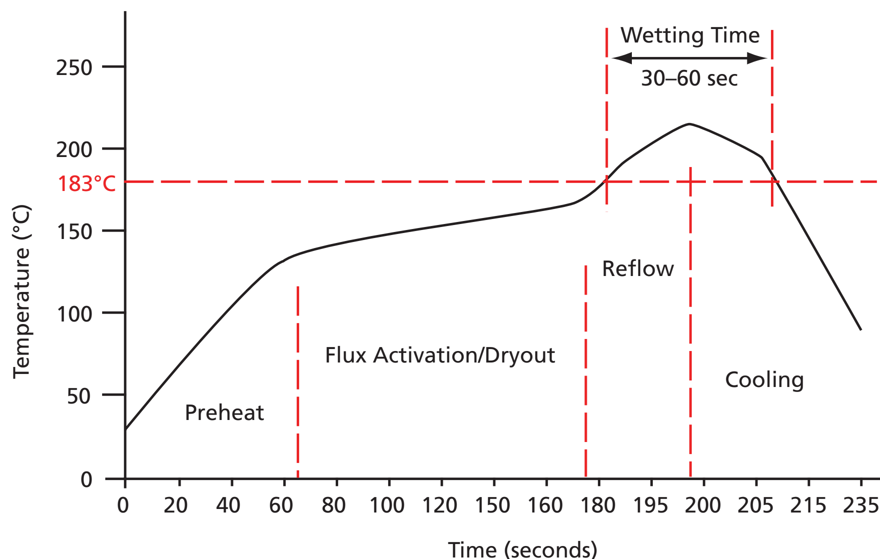

Figure 9 • **Eutectic Solder Flow Profile**

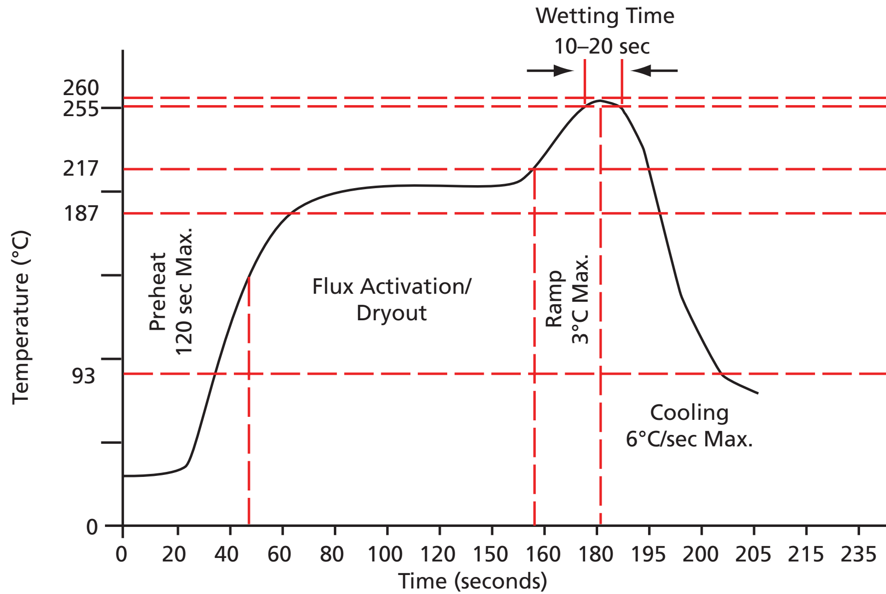

Figure 10 • **Lead-Free Solder Flow Profile**

Assembly Process Flow

Figure 11 shows the typical process flow for mounting surface mount packages to PCBs. The same process can be used for mounting the QFN, without any modifications. It is important to include post-print and post-reflow inspection, especially during process development. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80%–90% of stencil aperture volume to indicate good paste release. After reflow, the mounted packages should be inspected in a transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning may be required to determine the fillet shape and size and joint standoff height.

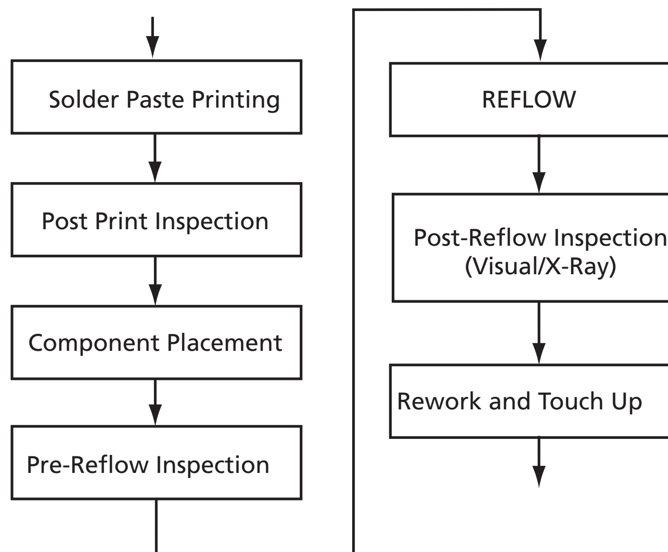

Figure 11 • **Assembly Process Flow**

Rework Guidelines

Since solder joints are not fully exposed in the case of QFNs, any retouch is limited. For defects underneath the package, the whole package has to be removed. Rework of QFN packages can be a challenge due to their small size. In most applications, QFNs will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to the handling and heating difficulties. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product-dependent complexities, the following provides only a guideline and a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement and attachment

Component Removal

The first step in removal of the component is the reflow of solder joints attaching the component to the PCB board. Ideally the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquid can be reduced as long as the reflow is completed.

In the removal process, Actel recommends that the board be heated from the bottom side using a convective heater, and hot gas or air should be used on the top side of the component. A special nozzle should be used to direct the heating in the component area. The heating of adjacent components should be minimized. Excessive airflow should also be avoided, since this may cause the CSP to skew. Air velocity of 15 to 20 liters per minute is a good starting point. Once the joints have reflowed, the vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Because of their small size, the vacuum pressure should be kept below 15 inches of mercury. This will ensure the component is not lifted if all joints have not been reflowed, thus avoiding pad liftoff.

Site Redress

After the components have been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and de-soldering braid. The width of the blade should be matched to the maximum width of the footprint and the baked temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with solvent. The solvent is usually specific to the type of paste used in the original assembly and past manufacturer's recommendations should be followed.

Solder Paste Printing

Because of their small size and finer pitches, solder paste deposition for QFNs requires extra care. A uniform and precise deposition can be achieved if a miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50X–100X magnification. The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the miniature stencil can be used to print paste on the package site. A stencil with a thickness of 125 µm and an aperture size and shape the same as the package land should be used. No-clean flux should be used because the small standoff of QFNs does not leave much room for cleaning.

Component Placement and Attachment

QFN packages are expected to have superior self-centering ability due to their small mass. The placement of this type of package should be similar to that of BGAs. As the land pads are on the underside of the package, a split-beam optical system should be used to align the component onto the motherboard. This will form an image of land overlaid on the mating footprint and aid proper alignment. Again, the alignment should be done at 50X–100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

Reliability Studies

Actel's supplier, Amkor Technology, has done extensive reliability studies for the QFN package type. Refer to the following document for more information:

Board Level Assembly and Rework Assessment of Thin Substrate Chip Scale Package (tsCSP), a Multi-Row Leadless Package (http://www.amkor.com/products/notes_papers/IMAPS_tsCSP_paper_Solectron.pdf) .

Appendix I: Detailed PCB Layout

Figure 12 shows the PCB top layer of a suggested board layout of soldered pads for QFN packages. This suggested board layout is for NSMD.

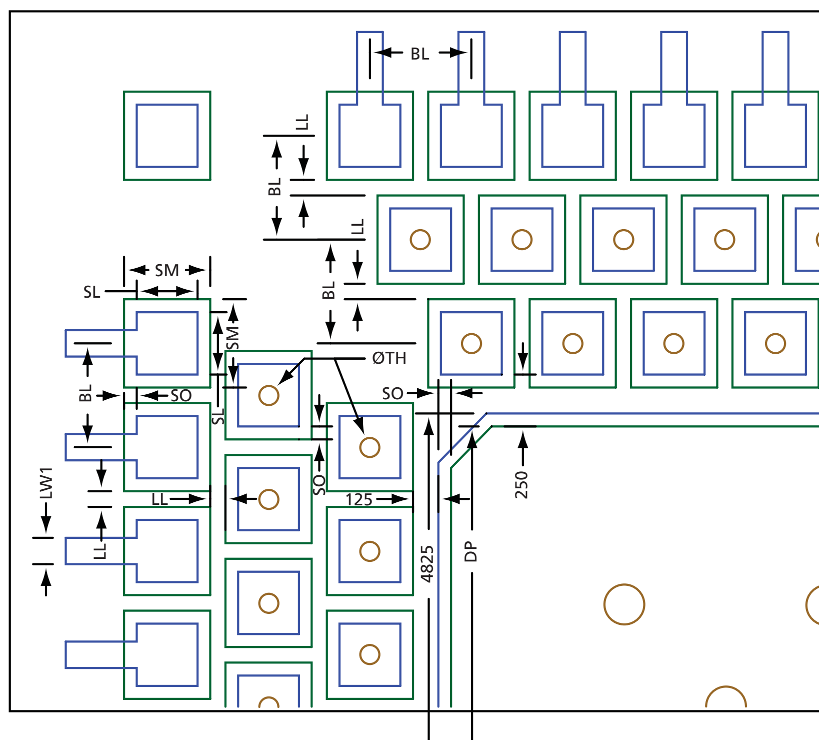

Figure 12 • **Soldered Pads for QFN Package (PCB top layer)**

Figure 13 shows the PCB lower layer of the suggested board layout.

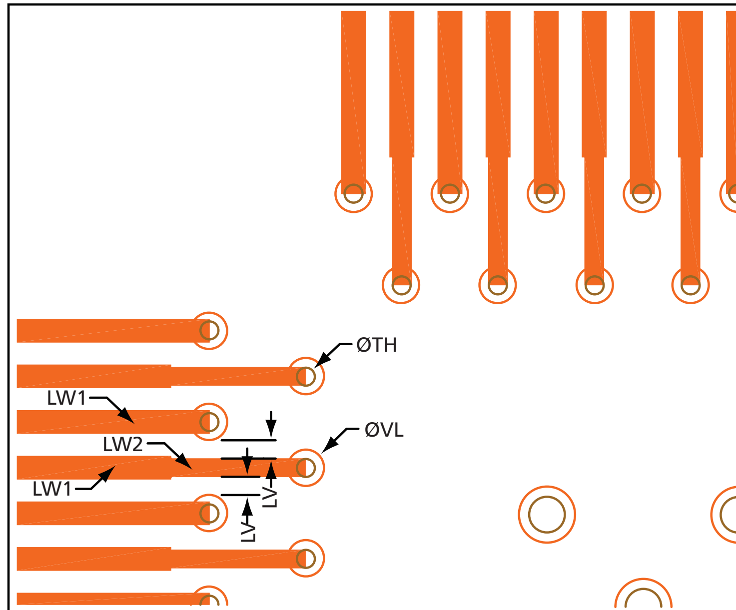

Figure 13 • **Soldered Pads for QFN Packages (PCB lower layer)**

Figure 14 shows the PCB top layer of a suggested board layout for soldered pads of QFN packages. This suggested board layout is for a reduced thermal pad, NSMD.

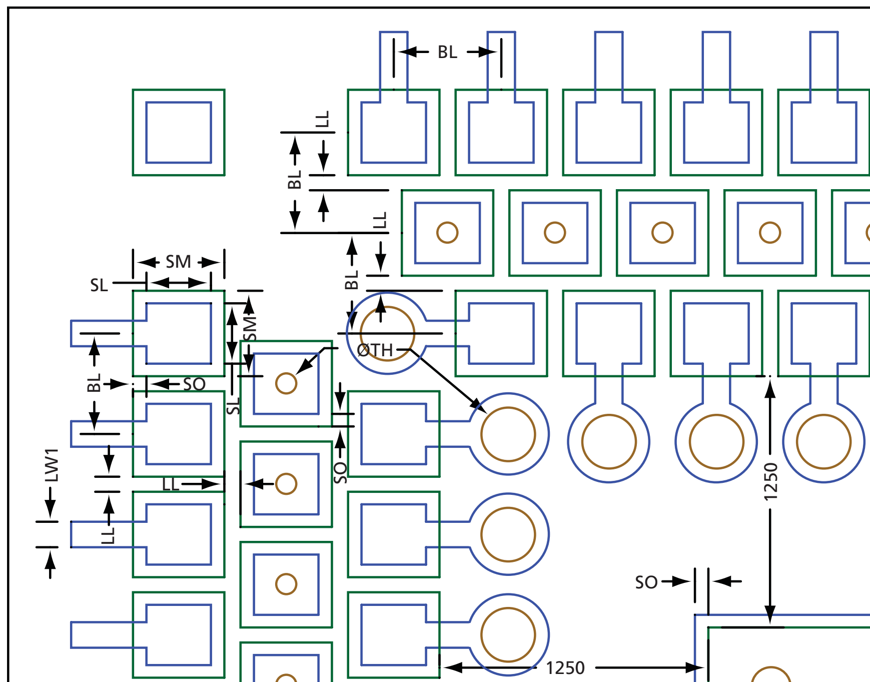

Figure 14 • **Soldered Pads for QFN Packages, Reduced Thermal Pad (PCB top layer)**

Figure 15 shows the PCB lower layer of the suggested board layout with reduced thermal pad.

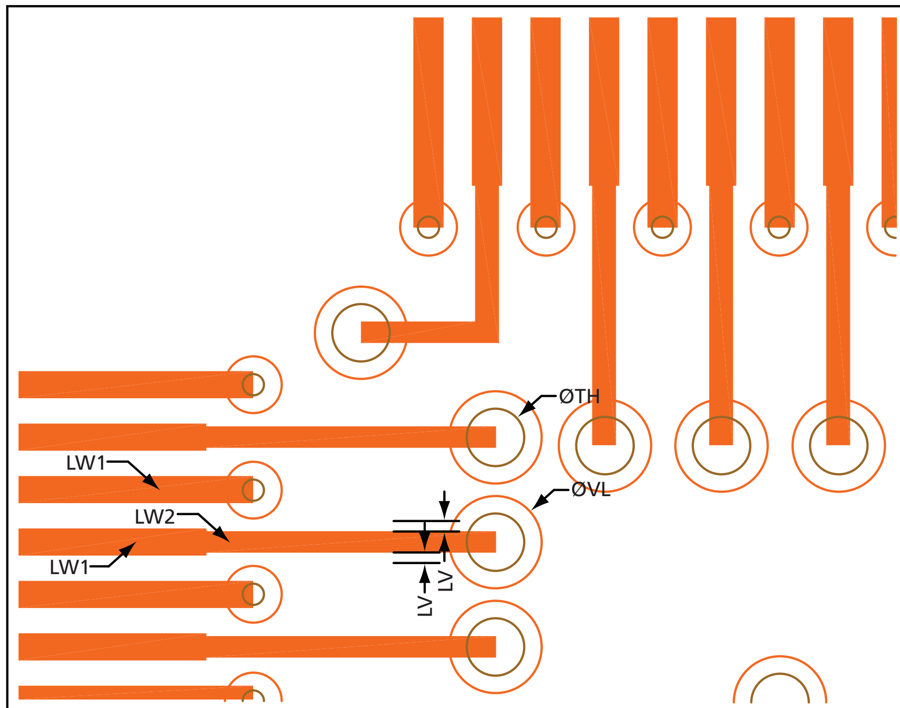

Figure 15 • **Soldered Pads for QFN Packages, Reduced Thermal Pad (PCB lower layer)**

Table 2 contains the recommended guidelines for board layout soldered pad dimensions for Actel QN packages only (0.5 mm pitch QFN).

Table 2 • **Recommended QFN Design Guidelines**

Dimension	**QN108**	**QN132**	**QN180**
Component Land Pad Diameter (SMD)	0.300	0.300	0.300
Solder Land Diameter (SL)	0.300	0.300	0.300
Solder Mask Opening Diameter (SM)	0.425	0.425	0.425
Solder Land To Solder Land (LL)	0.075	0.075	0.075
Solder Mask Overlap (SO)	0.0625	0.0625	0.0625
Solder Land Pitch (BL)	0.500	0.500	0.500
Line Width Between Via and Via Land (LW2)	0.100	0.100	0.100
Line Width Between Via outside and Via Land (LW1)	0.127	0.127	0.127
Line to Via Land (LV)	0.050–0.100	0.050–0.100	0.050–0.100
Via Land Diameter (VL)	0.250–0.400	0.250–0.400	0.250–0.400
Via Opening Diameter (TH)	0.100–0.250	0.100–0.250	0.100–0.250
Die Attach Pad (DP)	4.700 × 4.700	5.700 × 5.700	6.300 × 6.300
Pad Array	Perimeter	Perimeter	Perimeter
Body Size	8 × 8	8 × 8	10 × 10
Periphery Rows	2	3	3

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (51900172-1*)	Page
51900172-0	Color was added to Figure 3 · Detail Construction of Land Pad to clarify the layers.	2
	An additional paragraph and Figure 4 · Wider Trace under Solder Mask Edge to Avoid Trace Cracking were added to the "Three-Row QFN PCB Land Pad Design (QN132 and QN180)" section.	3
	An additional paragraph and Figure 7 · Thermal Via Options: a) Through-Vias; b) Combination of Through- and Blind Micro-Vias were added to the "Thermal Pad Via Design" section.	5
	The "Reliability Studies" section is new.	10

Note: **The part number is located on the last page of the document.*

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