Prototyping for RTAX-S/SL and RTAX-DSP

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Introduction

With the introduction of Microsemi® RTAX-S/SL and RTAX-DSP devices, you can now have access to leading-edge performance field programmable gate array (FPGA)s that have been designed for space. Building upon the success of the RTSX-SU family, the RTAX-S/SL and RTAX-DSP devices offer higher densities, higher performance, and new features such as integrated RAM blocks, Mathblocks, and increased I/O count and standards.

Prototyping verification is an important step in system integration where accurate behavioral simulation and static timing analysis are crucial. Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, Microsemi developed various prototyping options for RTAX-S/SL and RTAX-DSP. For early design development and functional verification, Microsemi offers the commercial Axcelerator devices (RTAX-S/SL only). For final flight design verification in hardware, Microsemi offers RTAX-S PROTO devices that have the same form, fit, and function as the flight silicon. For RTAX4000S/SL and RTAX-DSP devices, since there are no equivalent commercial devices, the preferred prototyping method is to use RT PROTO units. For more information on RT PROTO, refer to the www.microsemi.com/soc/documents/RTPROTO_Description.pdf.

The prototyping flow presented in this application note is provided to simplify the roadmap to production. The document describes the main architectural differences between the families and how to address the conversion issues that can occur as a result of these differences. Furthermore, this document also describes the software flows available to further simplify the prototyping process when going from the RTAX-S/SL design to the commercial Axcelerator.

Differences Between RTAX-S/SL, RTAX-DSP, and Axcelerator

As RTAX-S/SL and RTAX-DSP devices are derived from the Axcelerator family, the basic architecture remains the same. With reliability in space being the overriding concern, all key RTAX-S/SL and RTAX-DSP features are hardened against radiation. Any Axcelerator features that could not be hardened to meet the stringent radiation requirements are removed. The only exceptions to this are the Axcelerator's RAM FIFO controllers and the JTAG Boundary Scan Chain, which are still available in the RTAX-S/SL and RTAX-DSP. These are not hardened and they will not affect silicon reliability provided that they are not used.

Table 1 provides an explicit list of changes made in the RTAX-S/SL and RTAX-DSP devices. Refer to the www.microsemi.com/soc/documents/RTAXS_AX_Features_AN.pdf application note discussing in more details the differences between RTAX-S/SL, RTAX-DSP, and Axcelerator features.

Table 1 • **Major Architectural Differences Between RTAX-S/SL, RTAX-DSP, and Axcelerator**

Features	Modification from Axcelerator
Flip-flops	D-type flip-flops in R-modules and I/O modules are implemented with triple module redundancy (TMR) to ensure data bits stored within are single event upset (SEU)-resistant.
Clock Lines	Clock lines and global signals are hardened to be SEU-resistant.
PLLs	The eight PLLs have been removed from the RTAX-S/SL and RTA-DSP.
LP Enable Mode	Low power enable mode is removed from the RTAX-S/SL and RTA-DSP.
Clock Input Delays	The input delay switch is disabled for clock inputs only. Input delay is available for RTAX-S/SL and RTAX-DSP regular inputs.
Packaging Pins	The pins dedicated for PLLs will be no connect (NC) pins to ensure backward compatibility with future Axcelerator hermetic devices. The GND/LP pin is changed to GND.
RAM Blocks	While these remain unchanged in the silicon, an error detection and correction (EDAC) IP core is available through the Microsemi Libero® System-on-Chip (SoC) Catalog. Refer to the Microsemi website for application notes discussing EDAC.
FIFO Controller	The internal RAM FIFO controllers are not radiation hardened. When left unused, these controllers do not interact with the rest of the device.
Others	Changes to any AC parameters, timing, and operating limits resulting from design modifications can be obtained by comparing the Axcelerator and RTAX-S/SL and RTAX-DSP datasheets.

Synthesis tools do not prevent you from instantiating unsupported features such as PLLs, since the RTAX-S/SL, RTAX-DSP, and Axcelerator devices share the same features library for synthesis. However, the unsupported features will be detected during design compilation within Microsemi Libero SoC software. Also, the features such as clock input delays and TRST pin selection are grayed out in Microsemi Libero SoC software to reflect their fixed status. Finally, the architectural differences between the two devices will yield different internal timing, which must be taken into consideration.

In addition to the safeguards that are built into the software tool, you should adhere to the following two recommendations for a successful design:

- Do not include any unsupported macros; in RTAX-S/SL or RTAX-DSP designs. Refer to Table 1 for the unsupported features
- Use synchronous design techniques shown in the "Synchronous Design Methodology" section on page 3 in order to reduce the risk of timing errors when prototyping.

Non Radiation Hardened Features

The following features are not radiation-hardened:

- The built-in RAM FIFO controllers are not SEU-enhanced for RTAX-S/SL and RTAX-DSP devices. Microsemi does not recommend using them in devices that will be exposed to radiation. While they are fast and do not consume user gates, these RAM FIFO controllers are vulnerable to upset. You should be aware that an SEU can result in the loss of the RAM FIFO counting state, or flag errors that can only be corrected by clearing the FIFO. In addition, the memory implemented using these controllers are subject to SEU since they do not use EDAC. If you use built-in FIFOs in your design, you will be warned by Microsemi Libero SoC software during design netlist compilation. You are encouraged to use EDAC IP techniques to mitigate the SEU in the RAM blocks and to implement a FIFO controller using user gates. This will help to ensure that the RAM/FIFOs and associated memory are resistant to SEU.

- The JTAG circuitry is duplicated from the Axcelerator architecture and is not hardened against radiation. You must keep the extended TRST pin hardwired to GND during flight to hold the JTAG circuitry in reset and cannot utilize the JTAG boundary-scan logic during flight.

For more information, refer to the RTAX-S/SL Family FPGAs datasheet.

Synchronous Design Methodology

Although RTAX-S/SL and RTAX-DSP devices are library-compatible with Axcelerator devices, architectural differences between the two devices make their internal timing significantly different. An asynchronous RTAX-S/SL and RTAX-DSP design where its timing verified in the software will run faster in an Axcelerator prototype, which might cause race conditions or other such violations, rendering the prototype device useless for board-level verification. This also explains why RTAX-S/SL and RTAX-DSP internal performance cannot be gauged through board-level verification in an Axcelerator prototype. Consider these factors when mixing timing differences with asynchronous designs.

To minimize such timing-related issues, Microsemi recommends to implement fully synchronous designs and make use of both dynamic timing simulation tools and static timing analysis to diagnose any timing problems. Commercial design automation tools are generally optimized towards fully synchronous methodologies and do not account for potential asynchronous timing violations or glitches.

Fully synchronous designs follow three basic rules:

1. All registers that share the same data path should be connected to a common, low-skew, high-drive global clock network, as shown in Figure 1. Axcelerator, RTAX-S/SL, and RTAX-DSP devices have eight global clock networks that are accessible from special clock pins. These clock networks are the four hardwired clocks, HCLKA/B/C/D, and the four routed clocks, CLKE/F/G/H. All eight networks can also be accessed from special internal clock routing macros.
2. Every element running on the same clock should be triggered on the same clock edge (either rising or falling). This practice removes any dependencies on the duty cycle of the clock.
3. If multiple clock domains are used and data must cross between these domains, the data should be resynchronized between the different clock domains using one or two registers to ensure that the data is always in a known state. This is illustrated in Figure 2 on page 4.

Implementing fully synchronous design techniques may use slightly more resources on the device, but the advantage is a more stable circuit with shorter debug time. You can obtain complete, reliable, and accurate data from timing verification and analysis in less time, since worst-case static timing analysis will suffice in most cases.

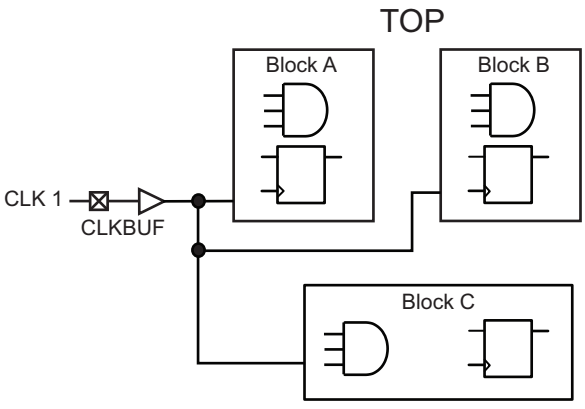
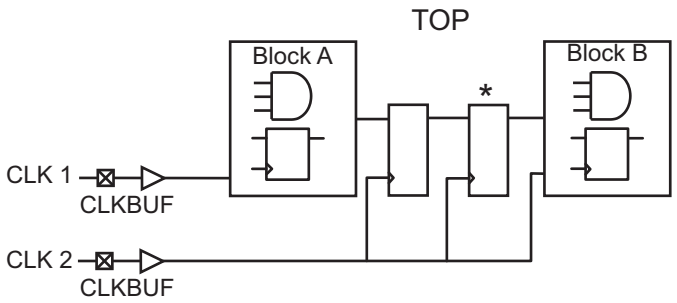


***Figure 1* • Using the Same Clock Network for Each Element**



*Note: *If the metastability settling time is relatively small compared to the clock period, you may want to eliminate the second flip-flop.*

***Figure 2* • Synchronous Data Between Clock Domains**

Common Violations

Clock or Register Enable

Implementing a gated clock by using an AND gate to enable a clock is not recommended because it could result in a glitch on the clock signal (Figure 3). The registers available in Axcelerator, RTAX-S/SL, and RTAX-DSP are implemented with an active low enable. Use this enable to gate the register instead of trying to modify the clock signal, as shown in Figure 4.

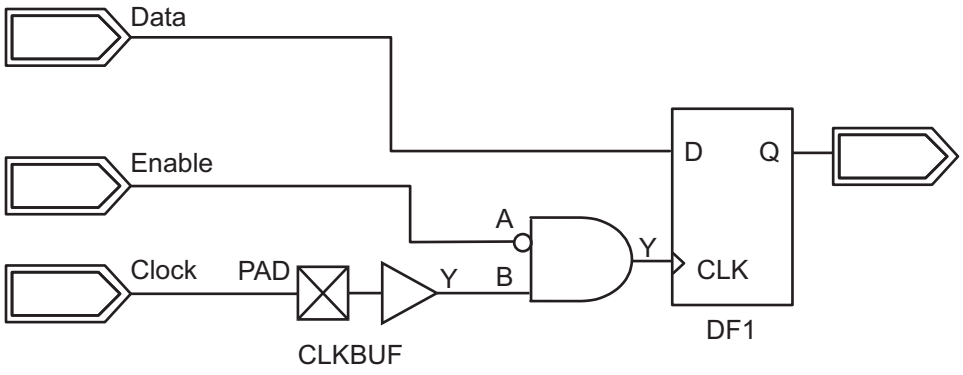


***Figure 3* • Unrecommended Practices of Using an AND Gate as an Enable**

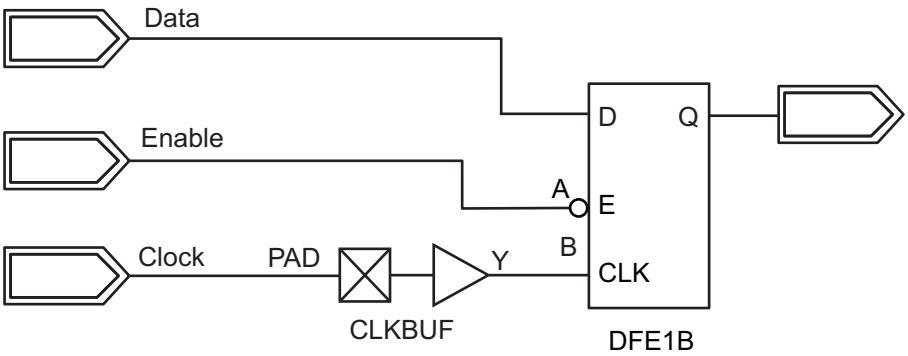


***Figure 4* • Proper Use of Built-In Register Enable**

Using Combinatorial Logic to Drive a Clock

Another common practice is to drive a clock using combinatorial logic, as shown in Figure 5. A problem occurs when the decoding of combinatorial logic generates glitches. A safer approach is to use a system clock to drive the clock signal of the register and use the combinatorial logic as an enable, as shown in Figure 6. There is no risk of a glitch being interpreted as a clock in this case.

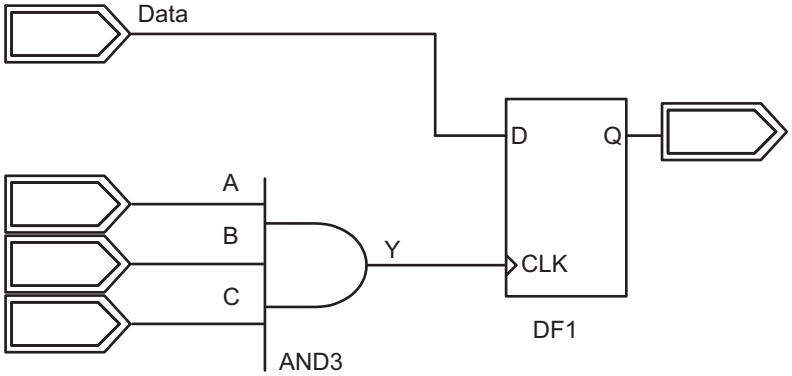


***Figure 5* • Glitch-Prone Combinatorial Logic Used as a Clock**

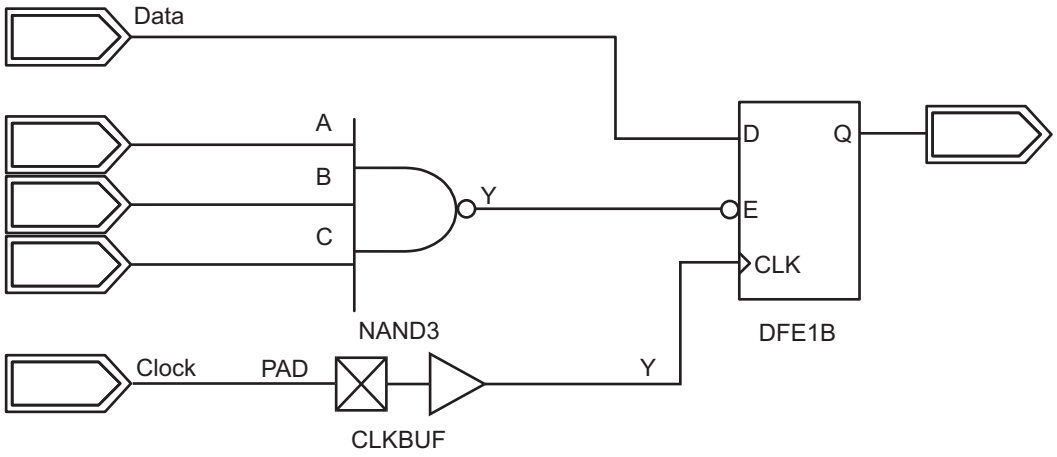


***Figure 6* • Using Combinatorial Logic as Enable with a System Clock**

Using a Divided Clock

A common way to divide a clock is to use a register and an inverted buffer for feedback. This method is acceptable for dividing an incoming clock as it enters the device and redistributing it on a local routing or a global clock network. This method causes a problem, however, if there are many small divided clock networks that share data or merge data back to the original clock (Figure 7 on page 6). Since there is a limit to the number of internally routed clock networks each device includes, many smaller divided clocks may not be able to use the global routing resources. In this case, the skew incurred by using normal routing resources and the delay incurred by dividing the clock makes the integration and analysis of these clock domains very difficult.

A preferable method in this case is to use the divided clock as an enable signal while clocking the registers from the original routed clock (Figure 8 on page 6). This allows the same system clock to be used throughout the circuit and reduces the number of global clock networks required for this section of the circuit.

Although more resources are required, the speed of the circuit and the ease of analysis may improve.

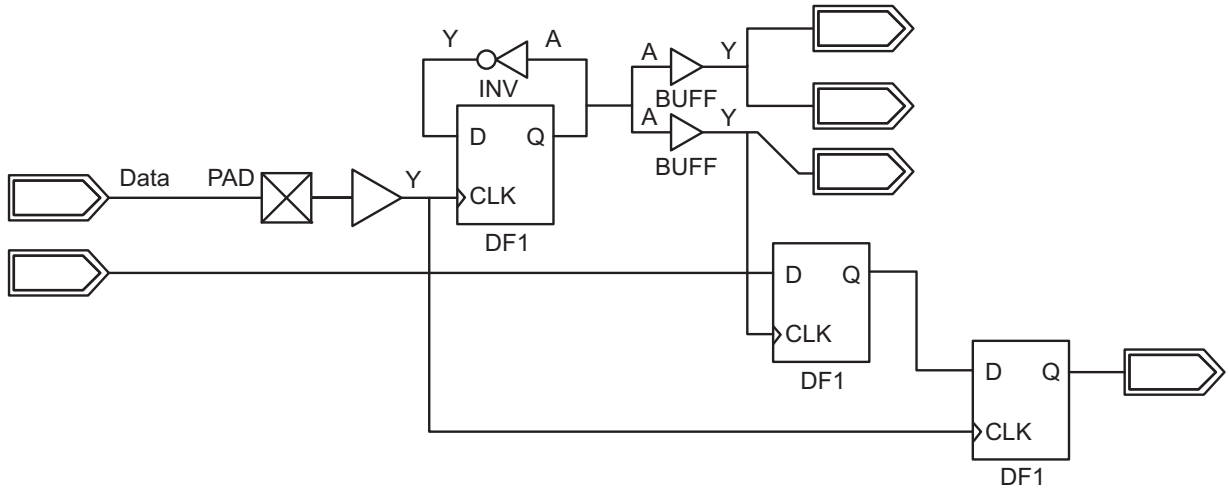


***Figure 7* • Merging Clock Domains Back to the Original Clock**

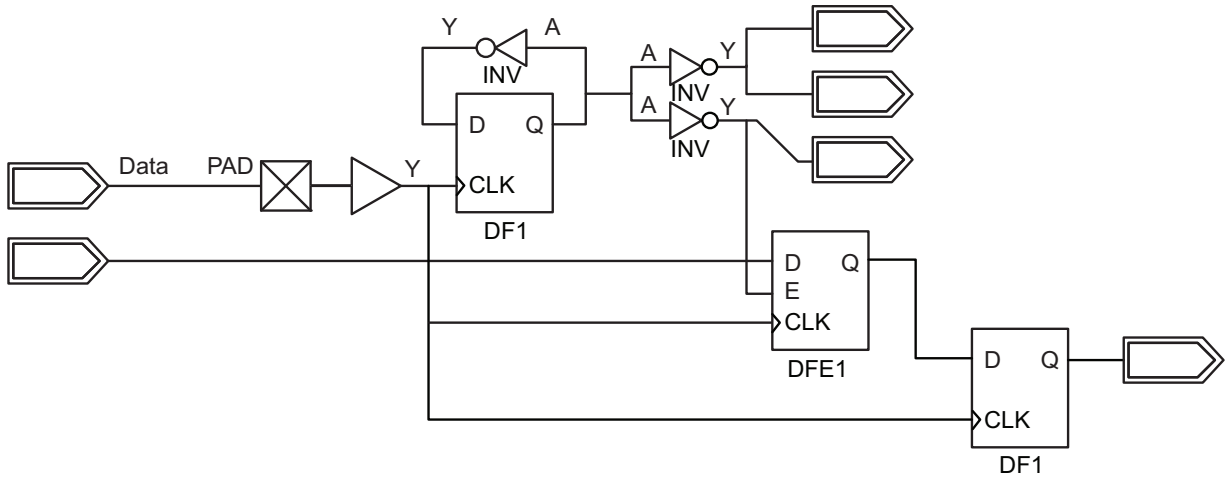


***Figure 8* • Using a Single System Clock with Divided Clock Signals**

Asynchronous Feedback Loops

Variations in timing delays may make asynchronous feedback circuits unreliable. Microsemi recommends replacing these circuits with ones that change with the system clock (Figure 9 on page 7).

Note: The circuit shown on the left side of Figure 9 on page 7 may glitch when the count changes from 0111 to 1000.

A reliable timing analysis that proves the absence of a glitch to the asynchronous clear is close to impossible to obtain. The circuit on the right side of Figure 9 shows a reliable replacement for the circuit shown on the left.

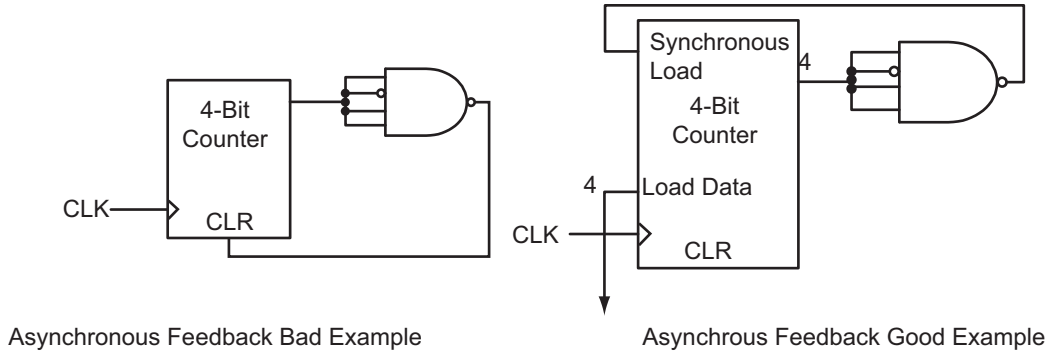


***Figure 9* • Asynchronous Feedback Circuits**

Asynchronous One-Shot Circuits

Asynchronous one-shot circuits are susceptible to timing problems similar to those of the asynchronous feedback loop, as shown in Figure 10.

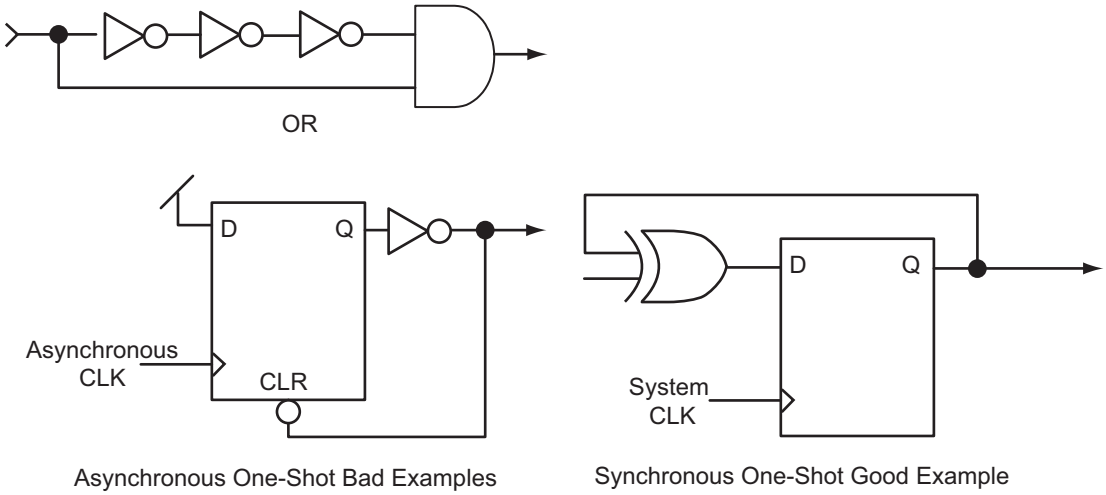


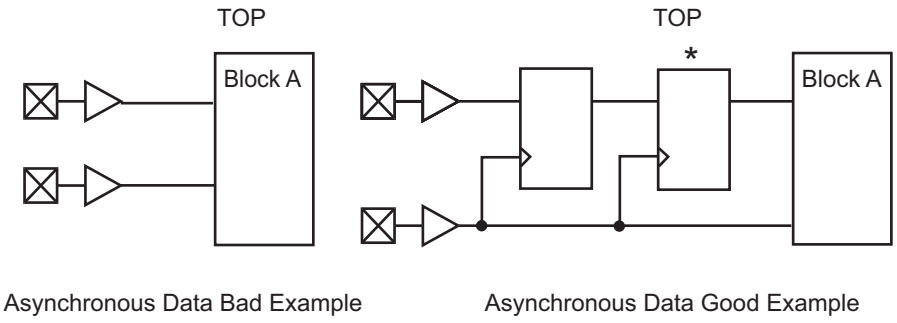
***Figure 10* • Asynchronous One-Shot Circuits**

Delay Insertion

Because of variations in routing and process parameters, the use of delay-specific circuits should be avoided. Circuits that depend on a specific module or buffer delay are vulnerable to routing, process, temperature, and voltage variations. Additionally, the use of delay circuits is not advisable because most EDA tools optimize out any redundant delay circuits.

Asynchronous Data Sampling

The problems associated with sampling asynchronous data are similar to those encountered when transferring data from one clock domain to another. The use of one or two registers to buffer the data is recommended, as shown in Figure 11.



*Note: *If the metastability settling time is relatively small compared to the clock period, you may want to eliminate the second flip-flop.*

***Figure 11* • Asynchronous Data Sampling**

Synchronous Preset and Clear

If the circuit on the left in Figure 12 is preset, and data is clocked on the same clock edge, the circuit could suffer from metastability problems.

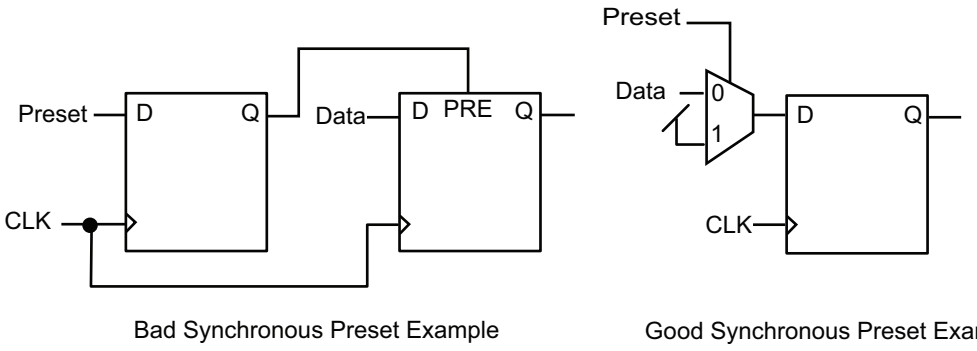


***Figure 12* • Preset and Clear**

RTAX-S/SL and RTAX-DSP Prototyping Flow

RTAX-S/SL uses the same design flow and tools as other Microsemi antifuse devices. Microsemi Libero SoC software generates a programming file for RTAX-S/SL that can be used to program the commercial Axcelerator® prototype device (Figure 13 on page 9) with the latest version of Silicon Sculptor software.

This flow ensures that the design accurately reflects RTAX-S/SL and eliminates the risk of incorporating removed features or falling short of timing requirements. In addition, the flow ensures that any errors are discovered early, instead of late in the design flow after the board-level verification is already completed. Preventing re-layout and the subsequent re-verification facilitates quick time-to-market. Therefore, it is essential that the design, pin assignment, place-and-route, timing verification, and simulation are done using the RTAX-S/SL device.

Microsemi Libero SoC software converts the RTAX-S/SL design to a compatible Axcelerator device and package. The reverse flow is not permitted.

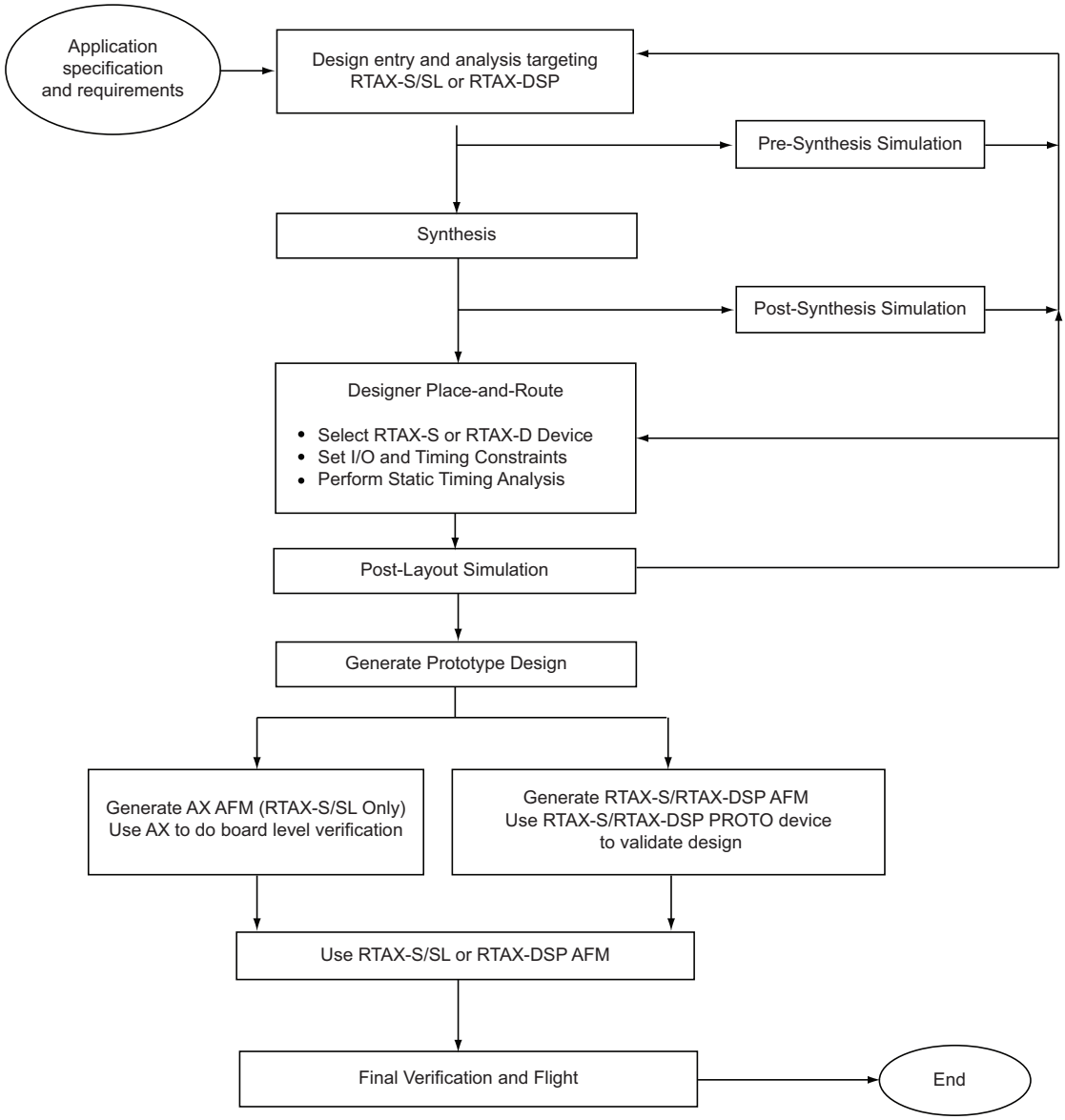


Figure 13 • **The RTAX-S/SL and RTAX-DSP Prototyping Flow**

Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, Microsemi has developed various prototyping options for RTAX-S/SL. For early design development and functional verification, Microsemi offers the commercial Axcelerator devices; for final flight design verification in hardware, Microsemi offers RTAX-S PROTO devices that have the same form, fit, and function as the flight silicon. For RTAX4000S/SL and RTAX-DSP devices, since there are no commercial equivalent devices, the preferred prototyping method is to use RT PROTO units.

The following is a summary of the available prototyping options:

- Commercial Axcelerator devices for functional verification (RTAX-S/SL only)
- RTAX-S/SL PROTO and RTAX-DSP PROTO devices with same functional and timing characteristics as flight unit in a non-hermetic package
- Low-cost reprogrammable prototyping solution for functional verification.

Prototyping with Commercial Axcelerator Devices (RTAX-S/SL only)

Prototype verification is an important step in system integration where accurate behavioral simulation and static timing analysis are crucial. Since the enhanced radiation characteristics of radiation-tolerant devices are not required in this prototyping phase of the design, commercial Axcelerator devices can be used.

The prototyping solution using the commercial Axcelerator devices consists of two parts:

- An easy software design flow that allows you to target an RTAX-S/SL design to the equivalent commercial Axcelerator device.
- A set of Microsemi extender circuit boards that map the commercial device package to the appropriate RTAX-S/SL package footprint.

Software Design Flow

After the design has passed functional and post-layout simulation in RTAX-S, you can generate an afm file for the Axcelerator prototyping device. This automatic flow prevents you from accidentally incorporating features exclusive to the Axcelerator device into the prototype device.

This methodology provides you with a cost-effective solution while maintaining the short time-to market associated with Microsemi FPGAs.

To generate the Axcelerator afm file, after saving the design database (.adb) file, select **Generate Prototype…** from Tools menu, as shown in Figure 14. For RTAX4000S/SL and RTAX-DSP devices, the preferred prototyping method is to use RT PROTO units since there are no commercial equivalent devices.

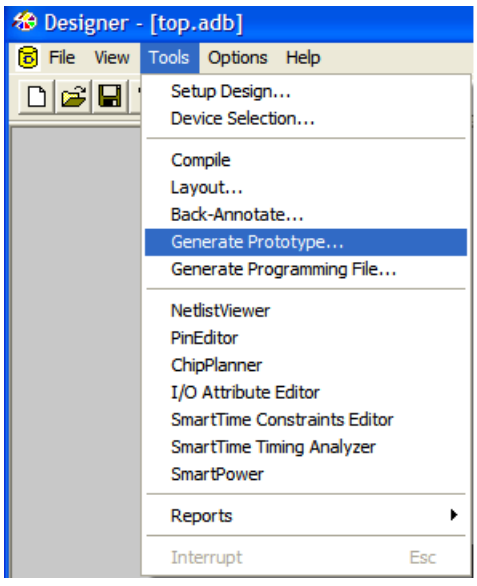


Figure 14 • **Tools Menu Showing the Generate Prototype Option**

The dialog box in Figure 15 opens. Select the options and click **OK** to generate the prototype .afm file. For more information regarding each option, refer to Libero SoC online help

Designer software tools runs through the process of creating the prototype files and generates the afm for the selected commercial Axcelerator die/package. After the prototype flow is complete, designer automatically returns to the RTAX-S project.

You must open the new prototyping design adb file manually to verify it. The prototyping adb is generated into the Output directory specified in Figure 15. To open the adb, from the File menu select Open and browse to the Output directory and select the prototyping adb.

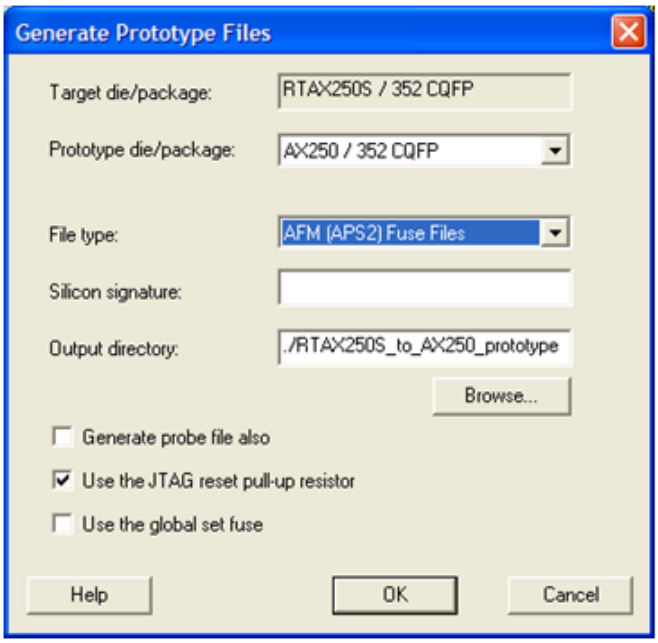


Figure 15 • **Generate Prototype Files Options**

Table 2 shows the commercial equivalent AX device that must be used to prototype for the equivalent RTAX-S/SL product type. The table shows a one-to-one mapping from RTAX-S/SL to Axcelerator without using any adapter except when it is noted. The prototype die/package option shown in Figure 15 reflects the valid only equivalent commercial Axcelerator die/package that can be used for prototyping. Those valid options are shown in Table 2.

Table 2 • **RTAX-S/SL to Commercial Axcelerator Mapping**

RTAX Targeted Device	RTAX Targeted Package	Prototype Device	Prototype Package
RTAX250S/SL	CQ208B/E/V	AX250	PQ208M
			CQ208M
	CQ352B/E/V	AX250	CQ352M
			FG484M*
	CG624B/E/V	N/A	
RTAX1000S/SL	CQ352B/E/V	AX1000	CQ352M
			FG896M*
	CG/LG624B/E/V	AX1000	CG/LG624M
			FG896M*
*Note: *Requires adapter socket. Refer to Table 3 on page 12 for more information.*			

Table 2 • **RTAX-S/SL to Commercial Axcelerator Mapping (continued)**

RTAX Targeted Device	RTAX Targeted Package	Prototype Device	Prototype Package
RTAX2000S/SL	CQ256B/E/V	AX2000	CQ256M
			FG896M*
	CQ352B/E/V	AX2000	CQ352M
			FG896M*
	CG/LG624B/E/V	AX2000	CG/LG624M
			FG896M*
	CG/LG1152B/E/V	AX2000	FG1152M
RTAX4000S/SL	CQ352B/E/V	RTAX4000S_PROTO	CQ352
			CG/LG1272
RTAX4000S/SL	CG/LG1272B/E/V	RTAX4000S_PROTO	CG/LG1272

*Note: *Requires adapter socket. Refer to Table 3 on page 12 for more information.*

Migration Path and Package Extender

Since the RTAX-S/SL packaging uses the ceramic column grid array (CCGA), and the Axcelerator uses the fine ball grid array (FBGA), the board must include a prototype adapter with the appropriate footprints to accommodate prototyping. Table 3 lists the package migration path available and the part number for the associated extender. Contact your local Microsemi sales representative for ordering information.

Table 3 • **Package Migration Path Using Microsemi Extender**

From	To	Extender Part Number
RTAX250S/SL 352 CQFP	AX250 484 FBGA	SK-AX250-CQ352RTFG484S
RTAX1000S/SL 352 CQFP	AX1000 896 FBGA	SK-AX1-AX2-KITTOP and SK-AX1-CQ352-KITBTM
RTAX2000S/SL 256 CQFP	AX2000 896 FBGA	SK-AX2-CQ256-KITTOP and SK-AX2-CQ256-KITBTM
RTAX2000S/SL 352 CQFP	AX2000 896 FBGA	SK-AX1-AX2-KITTOP and SK-AX2-CQ352-KITBTM
RTAX1000S/SL 624 CCGA (applies to columns from BAE and Six Sigma)	AX1000 896 FBGA	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM
RTAX2000S/SL 624 CCGA (applies to columns from BAE and Six Sigma)	AX2000 896 FBGA	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM

For more information on adapter sockets, refer to the following application notes:

CCGA to FBGA Adapter Sockets

CQFP to FBGA Adapter Sockets

Prototyping Using the RTAX-S PROTO Units

The RTAX-S and RTAX-DSP PROTO units offer a prototyping solution that can be used for final timing verification of the flight design. The PROTO prototype units have the same timing attributes as the RTAXS/SL and RTAX-DSP flight units.

Prototype units are offered in non-hermetic ceramic packages. The prototype units include "PROTO" in their part number, and "PROTO" is marked on the devices to indicate that they are not intended for space flight. They also are not intended for applications which require the quality of space-flight units, such as qualification of space-flight hardware. RT-PROTO units offer no guarantee of hermeticity, and no MILSTD-883B processing. At a minimum, you should plan on using class B level devices for all qualification activities.

The RT-PROTO units are electrically tested in a manner to guarantee their performance over the full military temperature range. The RT-PROTO units are offered in -1 or standard speed grades which enables you to validate the timing attributes of your space designs using actual flight silicon. RT-PROTO units are also available in low power (-L) option which can help users to achieve low static power to comply with the stringent board power supplies requirements.

The prototype units will be marked "NOT TO BE USED FOR FLIGHT", and must not be used for flight. For more information, refer to Prototyping for Space-Flight Designs with Microsemi RT-PROTO FPGAs.

Prototyping with ProASIC3E Reprogrammable Units

ProASIC3E prototyping solution by Microsemi offers the unique advantage of reprogrammability, resulting in cost savings while providing faster functional verification of designs in prototype stage. This methodology uses a footprint compatible adaptor board and an EDIF netlist and pinout convertor for easy migration. This prototyping solution is available through our partner Aldec.

Aldec provides the software that remaps antifuse primitives to flash which reduces design time and cost. In addition, the hardware adaptor is foot-print compatible with RTAX-S/SL, and therefore, a customer does not need to redesign a new board for prototyping. For more information, refer to www.microsemi.com/soc/products/solutions/milaero/rtaxsproto.aspx.

Moving to Production

When board-level verification is completed and the design functions as expected, simply open the RTAX-S/SL or RTAX-DSP design database (adb) file in Microsemi Libero SoC software and generate an AFM file to program the radiation-tolerant part. If you have used the PROTO units for prototyping, no further timing verification is necessary, since this was already done before the board-level verification.

Conclusion

Designers using Microsemi RTAX-S/SL devices have three distinct advantages over those using radiation-tolerant ASICs:

- Begin by employing commercial design techniques and readily-available EDA software.
- Cost savings through prototyping with equivalent commercial devices.
- Thorough screening before shipping to ensure quality and reliability of the silicon.

RTAX-S/SL and RTAX-DSP devices, derived from the commercial Axcelerator family, share the same architecture and use the same design tools. Making it very easy to move from design conception to prototyping and then to full production.

Also, you have an option now to conduct full hardware verification of your space application by using the RTAX-S/SL and RTAX-DSP PROTO units. The RTAX-S PROTO units provide full functional and timing verification of a flight design and are available in a non-hermetic ceramic package. The PROTO units cannot be used for actual flight and are marked as "NOT TO BE USED FOR FLIGHT" on the top of the package.

Provided you adhere to the design flow and other guidelines described in this application note, any potential conversion issues can be easily mitigated, greatly reducing the amount of time required for the design cycle.

Related Documents

Datasheets

RTAX-S/SL Family FPGAs

www.microsemi.com/soc/documents/RTAXS_DS.pdf

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 5 (January 2013)	Figure 13 was updated (SAR 43863).	9
Revision 4 (October 2012)	Updated the Application Note based on the inputs provided (SAR 32610 and SAR 24246) and the following sections are affected. • Updated "Introduction" section. • Added "Differences Between RTAX-S/SL, RTAX-DSP, and Axcelerator" section. • Added "Non Radiation Hardened Features" section. • Added "RTAX-S/SL and RTAX-DSP Prototyping Flow" section. • Updated "Prototyping with Commercial Axcelerator Devices (RTAX-S/SL only)" section. • Revised Table 3. • Updated "Prototyping Using the RTAX-S PROTO Units" section. • Added "Prototyping with ProASIC3E Reprogrammable Units" section.	N/A
Revision 3 (August 2007)	RTAX250S/SL information was added to Table 3.	12
Revision 2 (June 2007)	Figure 8 was updated. The previous version showed the incorrect graphic. This has been corrected in this version of the application note.	6
Revision 1 (April 2003)	This document was updated to include RTAX-SL information.	N/A
	The "Prototyping Using the RTAX-S PROTO Units" section is new.	13
	Table 3 was updated.	12
	Table 7 •RTAX-S/SL PROTO Units is new.	NA

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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