Abstract

This paper explores the performance benefits gained by digital techniques for current limiting in switch-mode power supplies. The necessary control architecture is described along with the several possible modes of operation. Characteristics of several actual supplies using these techniques are presented.

Summary

Techniques for protecting switching power supplies against excessive output current demands have traditionally borrowed the analog approaches of linear voltage regulators. In many instances, the resulting performance has been unsatisfactory. Problems such as degraded load regulation, poor response to overloads, and oscillation at the crossover point between constant voltage and constant current output are frequently encountered.

A brief analysis of the properties of two coupled closed-loop control systems provides some insight into the basic limitations of the analog approach to current limiting. Specific examples using several currently available pulse width modulator circuits are shown.

An evaluation of the benefits of a digital approach shows that with the proper control architecture, all of the limitation imposed by analog techniques can be removed, with subsequent benefits to the power semiconductors. The impact on power device load lines and improvement in current limit characteristics are examined. Waveforms from operational switching supplies illustrate the practical applications of the principles discussed in this paper.

Background

The architecture of almost all fixed-frequency, constant output voltage switch-mode power supplies can be reduced to the simple configuration in Figure 1. A saw tooth waveform is compared with the output voltage from an error amplifier, which in turn continuously compares a fraction of the supply output voltage with a precision reference voltage. The comparator output is a fixed-frequency, variable duty cycle pulse which drives a power switch.

The power switch in turn chops the DC input voltage at some ultrasonic frequency. An output filter smooths the bursts of energy into a low ripple DC voltage at the output terminals.

![Figure 1. Basic Architecture of a Constant Voltage Switching Power Supply.](image-url)
Despite the popularity of this technique, experience has shown that there are significant problems which result in degraded output regulation when compared to ideal current limiting characteristics. As shown in Figure 4, the supply voltage should be constant over the full range of rated output current. At some excess current level, the supply should make a sharp transition to a current source. In actual practice with an analog current

**Examples**

This method has been a popular solution to the problem of providing overcurrent protection. Figure 3 shows the control architecture of four integrated PWM circuits, all of which employ this analog approach.

In this configuration, a voltage amplifier with a fixed threshold or offset voltage derives a differential input signal from a current sense resistor in series with the supply output terminal. As the output current approaches the pre-determined limit, the amplifier enters its linear gain region, and its output voltage becomes increasingly negative. Diode D2 begins to conduct, clamping the error amp voltage to a low value and reducing the duty cycle of the pulse width modulator.

**Figure 2.** The Basic Switching Supply Modified for Analog Current Limiting.

**Figure 3.** Four Pulse Width Modulator Circuits with Analog Current Limiting

A. Silicon General SG1524

B. Texas Instruments TL494

C. Ferranti ZN1066

D. NEC Electron µPC1042C
loop, load regulation is degraded as the output current approaches the maximum rating. Furthermore once transition to current limiting has occurred, appreciable excess current can flow under short circuit conditions.

If the ratio of chopper frequency to the cutoff frequency of the output filter is at least 20, then the pulse width modulator may be modeled simply as a linear gain block. Its transfer function is given by:

$$ a(s) = \frac{a(0)}{(1-s/s_c)^2} $$

(Eq. 1)

where $s$ is the complex frequency variable $\sigma + j\omega$

$a(0)$ is the DC open-loop voltage gain

$s_c$ is a double pole at $s = -\frac{1}{\sqrt{LC}}$

A. ERROR AMPLIFIER

$$ a_c(s) = a(0) \frac{(1-s/s_a)}{(1-s/s_A)} $$

WHERE $s_A$ IS A POLE AT $s = -\frac{1}{R_0 C_1}$

WHERE $s_B$ IS A ZERO AT $s = -\frac{1}{R_1 C_1}$

B. PULSE WIDTH MODULATOR

$$ a(s) = \frac{a(0)}{(1-s/s_c)^2} $$

WHERE $s_c$ IS A DOUBLE POLE AT $s = -\frac{1}{\sqrt{LC}}$

C. CURRENT LIMIT AMPLIFIER

$$ a(s) = \frac{a(0)}{(1-s/s_d)} $$

WHERE $s_d$ IS THE SINGLE DOMINANT OPEN-LOOP POLE

The reason for this non-ideal behavior is found in the finite loop gain of the current limit amplifier. Not only must the loop gain of the voltage control be opposed, but also the non-abrupt conduction of the clamp diode must be compensated. Higher gain can narrow the difference between actual and ideal performance, but at the risk of oscillation at the crossover point between constant voltage and constant current. To understand why this is true, we must analyze the frequency behavior of the gain elements in the two control loops.

Analysis of the Stability Problem

The three gain elements are the error amplifier, pulse width modulator, and current limit amplifier. The following notation is used: open-loop gains and frequencies are designated by lower case letters ($a(s)$, $s_1$). Closed-loop gains and frequencies are denoted by upper case letters ($T(O)$, $S_1$). The frequency compensation connections shown apply to the SG1524 and other transconductance amplifiers. The same compensation principles, however, also apply to low-impedance output amplifiers, where the feedback network is connected between the output and the inverting input terminal.
When feedback is applied around the regulator, the poles move in complex frequency space along the trajectory shown. For low values of loop gain, the dominant poles remain real. When the loop gain $T(O) > \frac{1}{4a_2}$, the poles become complex. They then follow a path parallel to the $j\omega$ axis as $T(O)$ increases.

Note that the poles of the closed-loop transfer function always lie on the left hand plane, and so there is no stability problem. However, if $Q$ is much greater than unity the transient response may be unacceptable because of severe ringing.

At the transition point between voltage regulation and current regulation, the situation is quite different. The two feedback loops are now coupled together and oppose one another. A three pole system now exists, since the current limit amplifier now contributes a pole at $s_d$, so the positions of the poles in the $s$-plane are altered. If the bandwidth of the current limit amplifier is designed to be large (and ideally it should be to obtain rapid response time) then the paths of the poles $s_a$ and $s_c$ in the voltage loop will curve towards the $j\omega$ axis, as shown in Figure 7. It can be seen that the net effect of coupling is that, for sufficiently high loop gain, the closed-loop poles $S_1$ and $S_2$ will cross over into the right hand plane, resulting in oscillation at the supply output.

The error amplifier open-loop response is determined by external components $C_1$ and $R_1$ (Figure 5), since it is a transconductance amp with output impedance $R_o$. To obtain maximum closed-loop bandwidth for the voltage control loop, the designer must compensate the amplifier so that it exhibits an open-loop zero which cancels one of the poles of the low pass filter in the pulse width modulator.

One method frequently used to stabilize the supply is to narrowband the current limit amplifier. For the case where

$$s_d = \frac{2}{s_a + s_c}$$

the closed-loop poles are forced away from the $j\omega$ axis as the loops become coupled together, and no instability occurs. This condition is shown in Figure 8.

To summarize the situation, the switching power supply designer is faced with a dilemma. He can design the current limit circuitry for high gain to obtain a sharp limiting knee, and large bandwidth to obtain fast response time, at a substantial risk of oscillation.
Alternately he can avoid instability by designing for low gain, with resulting poor limiting characteristics: or he can slow the amplifier and risk destruction of the power switching devices. Clearly a new approach to the problem of current limiting is necessary to obtain better performance.

ANALOG CURRENT LIMITING

- Slow
- Degrades Load Regulation
- Potential Oscillation at Crossover
- Inflexible

A Digital Approach

A solution that bypasses all these difficulties is to monitor output current on a pulse-by-pulse basis. If an overcurrent condition is sensed during power switch conduction, the pulse is immediately terminated. The process is repeated at the beginning of each conduction cycle. To obtain the fastest possible reaction time, a digital node within the PWM architecture is chosen to inhibit the output pulse. Figure 9 illustrates one realization.

A voltage comparator with fixed input offset voltage switches from a logical HIGH state to a LOW state when the selected current threshold is exceeded. Since both logic inputs to the AND gate must be HIGH to enable the output pulse, the pulse width can be narrowed by the current limit comparator independently of the voltage control loop.

One further refinement is necessary to ensure that multiple pulses cannot occur during one oscillator period. The block diagram as presently defined only inhibits the output during overloads, but does not prevent the pulse from turning on again when the overcurrent condition is removed. Switching noise could cause the comparator output to switch back and forth erratically, forcing the power semiconductors to switch many times through a high-power-dissipation load line during one oscillator cycle. The insertion of a data latch which is reset by a clock pulse from the saw tooth oscillator solves this difficulty. The data latch is designed so that a PWM pulse may ripple through asynchronously, but the trailing edge will lock up the flip-flop and prevent any further output until reset at the beginning of the next oscillator period. This final configuration is shown in Figure 10.

The theoretical performance of this configuration is shown in Figure 11. As load current increases from no-load to maximum load, no triggering of the current limit comparator occurs. The output voltage is affected only by the regulation of the voltage control loop. When the current limit threshold is reached, the comparator terminates each output pulse and the output voltage begins to decrease. As the load on the output increases, the over current threshold point is reached earlier in each oscillator cycle. The pulse width will decrease to a minimum value determined by the propagation delay through the current limit loop. The storage time of the power switch is usually the dominant factor in this delay. Switch mode supplies which utilize power MOSFETs will exhibit the smallest pulse width due to the lack of any appreciable storage time. When the minimum pulse width is reached, the output current will increase as the load resistance decreases, since constant energy is being delivered to the LC output filter.

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**Figure 9.** Current Limiting by Inhibiting the Output from the PWM Comparator.

**Figure 10.** Addition of a Data Latch to Obtain Pulse-by-Pulse Current Limiting.

**Figure 11.** Theoretical Current Limiting with Bipolar and Power MOSFET Devices.
The excess current “tail” may easily be eliminated by foldback current limiting. This technique pre-biases the current limit comparator away from the threshold point with a fraction of the supply output voltage (Figure 12). As the supply voltage goes into current limit, the output voltage falls, reducing the bias on the comparator. Less current is then required through $R_{SC}$ to maintain limiting. Finally, at full short circuit only a fraction of the full output current is available, even with the “tailing” phenomenon.

During turn-on, distributed capacitance in the transformer primary winding causes current overshoot. During turn-off, leakage reactance contributes some collector voltage overshoot.

The design equations for foldback limiting are straightforward:

\[ I_{\text{MAX}} = \frac{V_{\text{TH}} + V_{\text{OUT}}}{R_{\text{SC}}} \left( \frac{R_1 + R_2}{R_{\text{SC}}} \right) \]  

(Eq. 4)

where $V_{\text{TH}}$ is the comparator threshold voltage

\[ I_{\text{SC}} = \frac{V_{\text{TH}}}{R_{\text{SC}}} \]  

(Eq. 5)

Impact on Load Lines

Pulse-by-pulse current limiting also has a beneficial effect on switching device load lines. Data was collected on load line excursions of a 40kHz forward converter, with line results shown in Figure 13. The forward configuration was chosen rather than a flyback design because the output current is always in phase with the conduction of the principal power transistor. Thus load changes at the supply output are instantaneously reflected back to the load line excursion.

The normal load line trajectory indicates some deviation from the theoretical path due to non-ideal transformer characteristics.

During a switching cycle where an overload exists, the collector current rises rapidly due to the low collector load impedance reflected from the power transformer secondary. Before the current can reach a destructive level, the conduction cycle is terminated, protecting the switching device from catastrophic failure due to damaged metalization or vaporized wire bonds. However, the collector voltage overshoot during turn-off is now greater due to the increased energy stored in the leakage reactance at higher current levels.

It can be concluded from the foregoing that pulse-by-pulse current limiting will protect the power devices from failure due to excessive current levels, but it offers no protection against abnormal leakage reactance voltage spikes. Their magnitude may be limited due to the imposition of a maximum value of current at turn-off, but some type of snubber network or other transient suppressor may still be required.

It is also apparent that device power dissipation is higher than normal during overload conditions. To avoid thermal damage an eventual transition from pulse-by-pulse limiting to “hiccup” mode current limiting may be desirable. “Hiccup” mode limiting occurs by discharging the PWM soft-start timing capacitor, causing the controller to turn off for several hundred milliseconds before resuming operation. An elegant method for controlling this transition by “fault counting” will be described at the end of this paper.
A Bipolar Example

To verify the actual limiting characteristics of a switch mode supply with digital current limiting, the 30 kHz buck converter in Figure 14 was constructed. Almost all the control circuitry is contained within two integrated circuits and a power hybrid. The SM625 is a 60 V, 15 A bipolar switch with matched commutating diode. It is controlled by an SG1524 pulse width modulator. The 2N2222 transistor provides constant current drive to the power switch over a wide range of input voltage.

Pulse-by-pulse current limiting is provided by an SG1549 Current Sense Latch. This circuit consists of two voltage comparators and a set/reset latch with Q and Q digital outputs. Both comparators have a 100 mV threshold voltage. One device has full differential inputs with a common mode range from +2 V to +40 V. The second comparator has its 100 mV threshold referred to ground, and is intended for sensing the voltage in an emitter resistor. This current sense configuration is desirable in forward and push-pull converters where secondary current overloads can be sensed by the reflection to the primary of the transformer. The two comparator outputs are ORed together at the SET terminal of the latch. A clock pulse from the oscillator output of the SG1524 is used to reset the latch. Maximum turn-off speed is obtained in this circuit by disabling the 2N2222 at its base with the open-collector LOW output of the SG1549.

Figure 15 shows the output voltage/current curve obtained with this regulator. The data points agree remarkably well with the theoretical curve for bipolar devices shown in Figure 11. The supply exhibits excellent load regulation (20 mV) all the way to maximum load current, with a sharp, well-controlled transition to current limiting.

A MOSFET Example

To further illustrate the performance obtainable with present high performance switch mode power supply components, a 100 kHz off-mains supply was designed with full input-output isolation, power MOSFETs, and an SG1526 pulse width modulator IC which incorporates the digital current limiting principles discussed earlier.

The block diagram of the PWM circuit (Figure 16) illustrates the differential voltage comparator, AND gate, and data latch that compromise the components for pulse-by-pulse current limiting. The comparator has a 100 mV threshold and 20 mV of hysteresis to minimize jitter at the decision point. The data latch allows only one pulse to pass through per each oscillator cycle. The memory flip-flop provides the double-pulse suppression logic. If the PWM pulse is gated off for more than one cycle, the flip-flop remembers which driver was the source for the last pulse. When the output is again enabled, the first pulse is automatically routed to the other driver. This prevents two pulses in succession from one driver, minimizing the possibility of transformer core saturation in push-pull configurations.
The complete schematic of the power supply is shown in Figure 17. A half-bridge configuration was chosen to minimize the drain-source breakdown voltage requirements on the power MOSFETs when operating from the rectified 220 V European mains. Power for the SG1526 pulse width modulator is derived from a small (3 W) 50 Hz power transformer. This arrangement maximizes supply efficiency and allows the voltage regulation loop to be referenced to the output ground. The two MOSFETs are driven from the secondary of a small ferrite pot core isolation transformer. The primary of the transformer is connected directly to the totem-pole output drivers of the SG1526. The oscillator is programmed for 200 kHz by \( R_T \) and \( C_T \), and the current sense network is designed to give a 7 to 1 foldback ratio.

The propagation delay through the overcurrent control loop is of major importance when attempting pulse-by-pulse limiting at 100 kHz. As Figure 19 indicates, the response time through the SG1526 from comparator to driver output is only 300 ns. Since this represents only 6% of the maximum duty cycle at 100 kHz, a large foldback ratio is possible.

Data taken on the current limiting characteristics of this supply are shown in Figure 20. As expected, the output voltage regulation was completely unaffected by the current limit circuit until maximum load current had been exceeded. Also, the available output current steadily decreased as the overload increased, as would be expected from Figure 12. However, there was no current “tailing” effect from the loop propagation delay. The explanation appears to be that under prolonged pulse-by-pulse current limiting the power dissipation in the power MOSFETs is sufficient for the negative temperature coefficient of transconductance to override the effect of loop delay.

Operational waveforms for the supply when operating under partial load are shown in Figure 18. The two traces show the unipolar gate drive signals at the pulse width modulator; these become bipolar when observed on the secondary of the isolation transformer. Transition edges are sharp and clean due to the totem-poles’ ability to source or sink 200 mA peak for charging and discharging the power MOSFET gate capacitance.
Fault Counting Technique

Fault counting may be utilized to reduce power dissipation in the power switch during prolonged current limiting. One implementation is illustrated in Figure 21, using an inexpensive CMOS ripple counter and an even less expensive timer circuit. The 14-bit binary counter accumulates pulse-terminating commands from the SG1526 comparator. The output of the 14th stage will go high after $2^{13}$ or 8192 counts have been accumulated. At 200 kHz (an overcurrent SHUTDOWN pulse can occur during either phase of the output) this represents 41 milliseconds of delay. When the counter output goes HIGH, the soft-start timing capacitor of the SG1526 is discharged. The SG555 timer is connected as an oscillator to periodically reset the accumulated count in the MC14020B, which allows a soft-start cycle to begin. A period greater than 41 ms should be used.

![Figure 21](image)

*Figure 21. Using CMOS Logic as a Fault Counter to Control Transition from Pulse-by-Pulse Current Limiting to "Hiccup" Mode Current Limiting*

Obviously this technique can be extended even further. A second counter could accumulate “hiccup” cycles and shut the supply off until manual reset or power recycle. This is easily accomplished with the SG1526 since the SHUTDOWN and RESET terminals are compatible with both TTL and CMOS logic.

**DIGITAL CURRENT LIMITING**
- Fast
- No Load Regulation Degradation
- Clean Crossover from Voltage to Current Output
- Multiple Current Limiting Modes Possible

**Conclusion**

The use of digital current limiting techniques provides enhanced load regulation, a sharp transition to constant current, and faster protection to the power semiconductors in a switch-mode power supply when compared to analog methods. It also offers the designer flexibility in the choice of crossover criteria from pulse-by-pulse mode to “hiccup” mode to total shutdown. The net benefit to users will be enhanced reliability and increased performance from switch-mode power supplies.

**References**

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