A NEW VERSATILE PWM CONTROL CIRCUIT FOR SWITCHING POWER SUPPLIES

Abstract

A new control circuit for pulse-width-modulated switch-mode power supplies is described. This device offers improved electrical and functional performance over earlier designs, while retaining the familiar pin-out of the industry-standard SG1524. Innovative circuit design techniques and optimized control architecture result in improved reference accuracy, protection against inadequate supply voltage, elimination of harmful output switching transients, improved current limiting, and higher voltage and current capabilities from the output transistors. A 50 kHz power supply utilizing the new controller is described, and performance characteristics are analyzed.

Introduction

Since the introduction of the first monolithic control chip for switchmode power supplies in 1976, and its subsequent wide acceptance as the basic building block for high-efficiency regulator designs, the semiconductor industry has found itself in a bit of quandary when attempting to define an improved device. On the one hand, the initial device, being rather simple and straightforward, had a number of deficiencies when its capabilities were compared with the total requirements of most switchers. As a result, new, complex controllers were introduced with improved reference accuracy, protection against inadequate or fluctuating supply voltage, improved current limit circuitry, fault suppression logic, and a host of other features.

On the other hand, the new controllers, while enthusiastically accepted first by aerospace designers for sophisticated high-performance supplies and later by major computer and instrumentation manufacturers, lacked the familiar pin-out of the earlier device. As a result it has not been possible until recently to easily upgrade the performance of an existing design by simply plugging in a more intelligent pin-for-pin substitute.

The circuit to be described has been under development at Microsemi for more than two years, and represents an attempt to fit as much function as possible within the constraints of the original device pin-out. Designated the SG1524B, the device block diagram is shown in Figure 1.

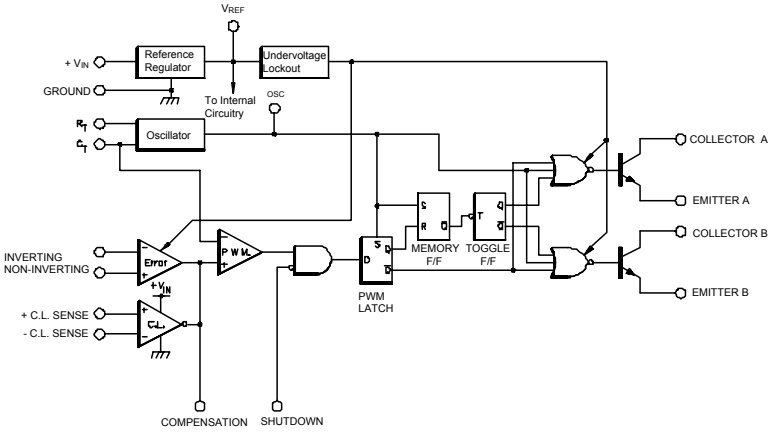

Figure 1. Block Diagram of the SG1524B Pulse Width Modulator

Functional Description

A precision +5 V reference trimmed to an initial ±1% accuracy provides a voltage standard for the regulation loop. It also powers most of the internal control circuitry, eliminating adverse effects due to fluctuating supply voltage. A high gain error amplifier compares the reference voltage with the switchmode supply output voltage, and generates a PWM control voltage at Pin 9. This voltage is compared against a periodic linear ramp generated by the oscillator circuit.

Oscillator frequency is determined by an external timing resistor and capacitor, R_T and C_T. The comparator output is a fixed-frequency, variable pulse-width logic signal which passes through routine logic to one of the two high current output transistors if the Shutdown pin is LOW.

A current limit amplifier within the IC overrides the PWM control voltage when the voltage differential at the Current Limit Sense inputs reaches 200 mV. This built-in threshold permits direct sensing across an external current sampling resistor. On-chip undervoltage lockout circuitry protects the power semiconductors in the switchmode supply by guaranteeing orderly start-ups and shutdowns as supply voltage is switched on and off.

Each control section of this new PWM controller has been either redesigned for improved performance, or is a completely new function compared to the original SG1524 design. A detailed description of each section follows to highlight the major improvements.

Bandgap Reference Regulator

The precision reference uses the predictable base-emitter voltage of NPN transistors to generate the +5 V reference voltage, rather than a zener diode[1,2]. The advantages of this design approach are: lower noise due to elimination of the shot noise associated with an avalanche device, low turn-on drift, better long term stability, and operation from a lower supply voltage. The primary disadvantages are that the bandgap requires more components, and thermal matching of key devices is necessary for realizing low thermal drift.

	ZENER REFERENCE	BANDAGE REFERENCE
Minimum Supply Voltage	8 V	7 V
Output Noise Voltage	75 µVrms	25 µVrms
Long Term Stability	20 mV/1000 hrs	5 mV/1000 hrs
Turn-on Drift	5-35 mV	2 mV

Table 1. Comparison of Zener and Bandgap Reference Typical Parameters

The ability of the PWM controller to be fully functional with a 7 V supply enhances its usefulness in portable instrumentation applications, where six-cell Ni-Cad battery voltage is defined as end-of-life before recharge.

Undervoltage Lockout

The undervoltage lockout circuitry prevents spurious turn-on commands to the external power transistors when the supply voltage to the integrated circuit is too low for proper operation. When the reference voltage is less than +4.5 V, the output transistors are forced to an OFF or non-conducting state. Additionally, the output of the error amplifier is clamped to ground. When the supply voltage rises to +7 V, the output drivers are enabled and the amplifier output is released. Since compensation capacitance is usually present at Pin 9, this provides a measure of built-in soft start.

During the power-up period of the controller, when the undervoltage lockout is achieved, bias current is freely supplied to all the internal control circuitry. This insures that all control functions have stabilized in the proper state when the turn-on voltage is reached, and it prevents the possibility of start-up glitches.

The lockout circuitry monitors the reference voltage rather than $+V_{IN}$ to allow the SG1524B to be used with +5 V supplies in the same manner as the original SG1524. If the $+V_{IN}$ pin is connected to the V_{REF} pin and +5 V ±10% is applied, the control chip will function normally. When the undervoltage sense circuitry monitors the $+V_{IN}$ pin, this type of operation is not possible due to the 2 V to 3 V drop across the internal regulator.

To provide jitter-free turn-on and turn-off points, the lockout circuitry has been designed with approximately 500 mV of hysteresis. This provides rejection of 120 Hz ripple on the $+V_{IN}$ line and reduces capacitive filtering requirements on the controller supply voltage.

Error Amplifier

The error amplifier of the SG1524B was designed with three principle goals in mind: a common-mode range extending from +2.5 V to $+V_{REF}$, excellent supply voltage and common-mode noise rejection characteristics, and a minimum voltage gain of 60 dB at +125°C. Like its predecessor, it is a transconductance amplifier with a high-impedance output to permit external soft-start circuitry.

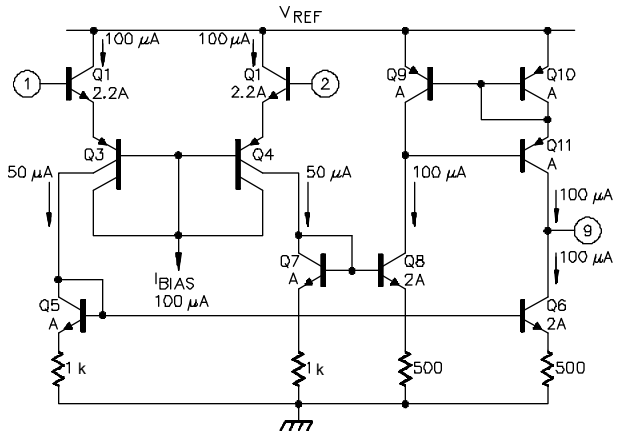

Figure 2. Schematic Diagram of the SG1524B Error Amplifier

Input transistors Q1 and Q2 are connected as emitter-followers with their collectors tied to the +5 V reference supply. This configuration provides the required common-mode range, even with $+V_{IN}$ connected to V_{REF} for operation from a +5 V supply. It also provides current gain to reduce input bias current, and produces a low impedance source to drive level shifters Q3 and Q4.

These PNP devices operate at a forced beta of 1.0, and are connected common base to maximize frequency response. Input stage operating current is set up by the 100 µA bias supply to the common base. Frequency response is further improved by the low impedance collector loads Q5 and Q7. These two devices are diode-connected and form the input sides of two precision 2-to-1 current mirrors, which provide additional current gain. The output current of Q6 provides the pull-down or sink current for the amplifier output. The collector current of Q8 is referenced to the +5 V supply rail by the Wilson current mirror consisting of Q9, Q10, and Q11. The collector current of Q11 provides the pull-up or source current for the amplifier output. It can be seen from the symmetry of the circuit that a differential input voltage is converted to an output current, with a maximum of ±200 µA available. The open-loop voltage gain can be shown to be[3]

$$A_V = gm\ R_L = I_S \frac{q}{kT} R_L = .001\ R_L \text{ at } +25°C$$

Since R_L is the parallel combination of the output impedances of Q6 and Q11, and is typically 4 MΩ an open-loop voltage gain of 72 dB is obtained.

The circuit design of the output stage insures that the maximum positive output swing never exceeds +4.3 V. This is important when considering loop recovery from momentary overloads which drive the PWM to maximum duty cycle. The peak value of the saw-tooth oscillator waveform is +3.4 V, and the error amplifier must slew from positive full scale to less than this voltage to reduce the duty cycle from maximum. Some error amplifier designs clamp the output voltage with a 6.3 V zener diode, nearly tripling the recovery time from overload. Since all the voltage gain of the error amplifier takes place at the output pin, the amplifier can be easily frequency compensated at this node with shunt reactance to ground. The uncompensated amplifier exhibits an open loop pole at 350 Hz and a typical unity-gain bandwidth of 2 MHz.

Current Limit

The current limit amplifier has been redesigned to eliminate the two most common complaints about the original SG1524: limited input voltage range and slow response time. In the original design the ±1 V common-mode range restricted current sensing to the supply return line only. In many systems, ground returns cannot be separated, making the current limit function unusable. Also, the internal frequency compensation provided freedom from oscillation at the expense of response time.

In the new design, input transistors Q1 and Q2 allow common mode voltages as low as -0.3 V over the operating temperature range, allowing sensing in the ground line for configurations that require it. The upper limit is restrained only by the value of $+V_{IN}$, to which the level-shifter current sources I1 and I2 are referenced. The voltage drop across R2 creates a 200 mV offset voltage at the amplifier input which provides the current sense threshold. The positive 0.2%/°C temperature coefficient of R_2 is balanced by a negative tempco for I2, effectively canceling effects of temperature on the current sense threshold.

Since both the allowable common-mode and differential voltages are much greater with this design, higher current foldback ratios can be achieved compared to the maximum of 3 or 4 possible with the earlier part. Also, the bias currents are a factor of 10 lower, resulting in more consistent limiting thresholds from unit-to-unit when foldback is employed.

Because there is no internal compensation capacitor, stability in the current limit mode will depend on external components. Due to the controller architecture, in which the output of the current limit amplifier overrides the error amplifier, these external frequency compensation networks may either be shared with the error amplifier or optimized for the current limit amplifier. The two choices are shown in the figures. In either case, the designer now has the freedom to optimize bandwidth for his particular switcher configuration.

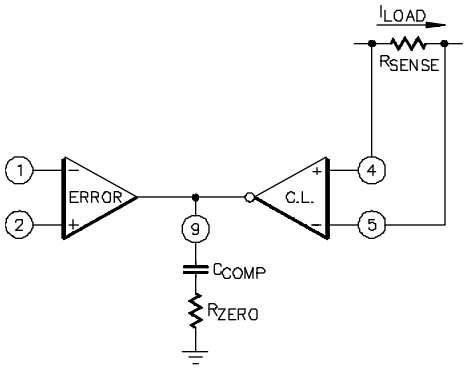

Figure 4. Current Limit Compensation in Common With Error Amp

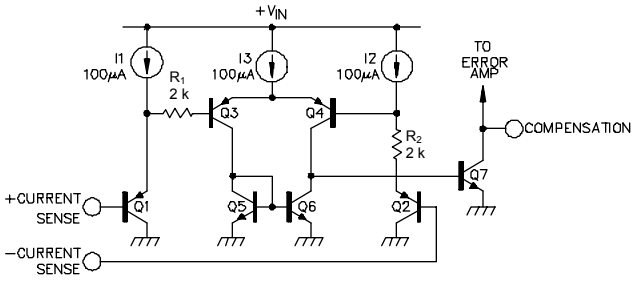

Figure 3. High-Gain Current Limit Amplifier

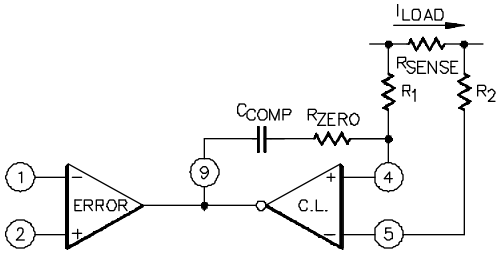

Figure 5. Current Limit With Optimized Frequency Compensation

Oscillator

The saw-tooth oscillator circuitry of the SG1524B incorporates the same design improvements recently applied to the SG1524. These result in greatly improved external drive and synchronization capability, together with reduced saw-tooth undershoot at high frequencies. In the original SG1524 design, an external synchronization pulse applied to the OSC pin did not generate a self-sustaining discharge cycle. The extent of the discharge of C_T depended on both the amplitude and duration of the external pulse. As a result, it was possible to generate erratic saw-tooth waveforms with partial discharge cycles and pulse-to-pulse modulation of waveform endpoints. The frequency result was audible noise from sub-harmonics, transformer saturation, and destruction of the power transistors.

In the improved design, and external sync pulse which meets the minimum threshold requirements triggers a positive feedback circuit. This circuit drives the oscillator to end-of-discharge even if the external pulse is very narrow. Due to the feedback, there exists no in-between or quasi-synchronized state; the oscillator switches smoothly between free-running and synchronized modes as the external pulse amplitude is varied through the trigger threshold.

The positive feedback also effectively bootstraps the comparator gain, providing enhanced voltage swing and output current at Pin 3 to drive peripheral circuits. The improved oscillator design, together with a fast, DC-coupled toggle flip-flop, permits operation beyond 500 kHz. However, the limitations associated with single-transistor outputs put a practical upper limit of 400 kHz on the device.

Full Double-Pulse Suppression Logic

The PWM logic in the SG1524B insures that the output pulses always alternate from side to side, regardless of the action of the shutdown circuit. This is very important in push-pull switcher configurations where two pulses in succession on one side of the power transformer primary will cause core saturation and instantaneous failure of the power transistor.

The logic consists of two sections: a PWM latch circuit and a memory flip-flop. The latch allows only one pulse through per oscillator cycle. Once a PWM pulse is terminated, whether due to the normal PWM process or due to SHUTDOWN going high, the pulse cannot start again until the beginning of the next oscillator cycle. Pulse-by-pulse current limiting is easily accomplished now because of the latch feature and the completely digital (and therefore very fast) shutdown circuitry.

The memory flip-flop insures that output pulses always alternate from the output transistors. This is accomplished by generating a clock to the toggle flip-flop only if a PWM pulse was generated during the previous cycle. In the original SG1524, the toggle flip-flop changes state with every oscillator pulse, irrespective of what the outputs are doing.

Figure 6 and 7 illustrate the difference in performance between two PWM control ICs, one with only a data latch and the other with the full double-pulse suppression logic described above. The triple-trace photos in each example show an alternating output pulse sequence interrupted by a SHUTDOWN command, followed a short time later by resumption of outputs from Emitters A and B. Oscillator frequency is 40 kHz for each device, so 20 kHz is obtained at the output transistors.

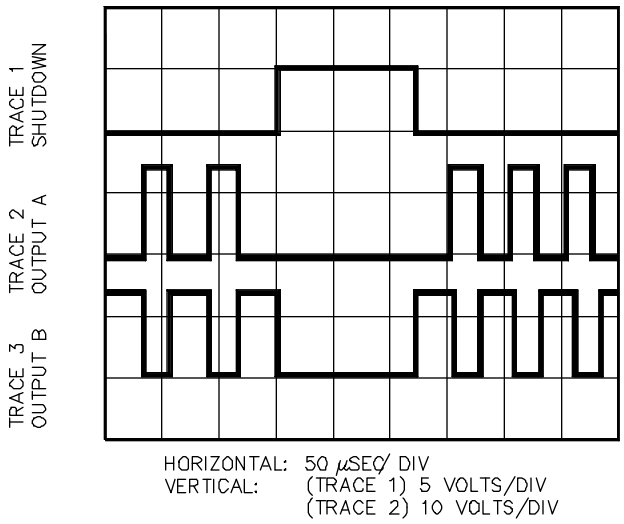

Figure 6. Output Sequence Without Double Pulse Suppression

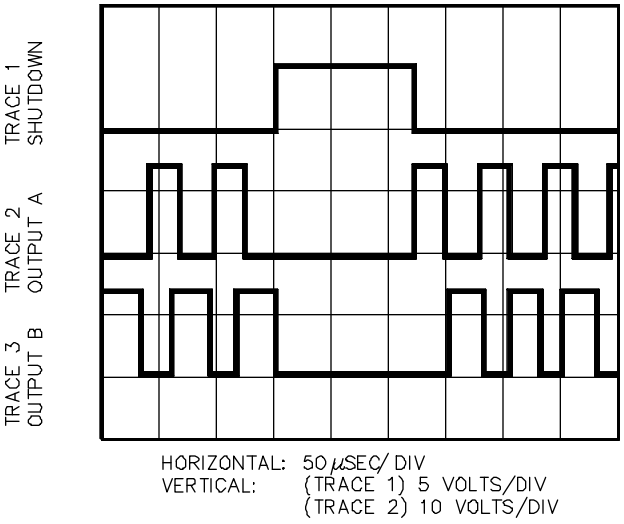

Figure 7. Output Sequence With Double Pulse Suppression

In the first case, the PWM pulses are alternating can BABAB when a SHUTDOWN signal inhibits the outputs for five oscillator cycles. When output resumes, the output sequence begins BABAB...Two pulses have occurred in succession from Emitter B.

With the second control IC, the PWM pulses are again alternating BABAB when a SHUTDOWN signal is received, again inhibiting output for five oscillator cycles. When SHUTDOWN is removed, output resumes but with an ABABA...sequence. The potential double-pulse from Emitter B has been eliminated by the internal pulse-steering logic.

This side-by-side pulse-routing problem exists for any PWM control IC with push-pull architecture and a fully digital shutdown function. In the original SG1524 design, recovery from shutdown was fairly slow since the error amplifier output was pulled to ground for turn-off. Turn-on was limited by the 100 µA output current of the error amp, the internal compensation capacitor in the current limit circuitry, and any external frequency compensation components. This created an inherent soft-start characteristic. With digital shutdown, the error amp voltage is not immediately affected; the first pulse out after shutdown can be the same width as before shutdown, making pulse-routing logic an absolute necessity to guarantee the safety of the power switches.

Output Transistors

In response to requests for greater output drive capability, the output transistors were redesigned for both higher breakdown voltage and more current.

In a PWM controller with a single-transistor output structure, the load driven is frequently one end of a center-tapped transformer primary winding. Since the maximum collector voltage is 2 x V_{CC}, the absolute maximum rating of 40 V for the earlier device restricted the supply voltage to 20 V. Consideration given to the effects of transformer leakage reactance would reduce this voltage still further. The SG1524B output transistors carry BV_{CEX} ratings of 60 V, high enough for use on a standard +28 V supply bus.

Output device geometry was scaled up to allow reliable operation at continuous collector currents of 100 mA. This represents a factor of two improvement over the earlier device, which was characterized at only 50 mA. As a further aid to the designer, the data sheet for the new device specifies maximum saturation voltage at two continuous current levels: 10 mA and 100 mA. The maximum peak current capability of the output transistors is 200 mA for 1 µs.

The anti-saturation clamp circuit around the output transistors found in the earlier PWM controller has been retained in the SG1524B to enhance switching speed. Each output transistor is also guarded against excessive current by protective circuitry which limits the maximum continuous current to 150 mA at +25°C.

Design Example

The functional usefulness of a new device is best demonstrated by study of an actual switcher design. The circuit described illustrates full control of a power supply with a single integrated circuit, resulting in reduction of overall cost and an increase in supply reliability through reduction of component count.

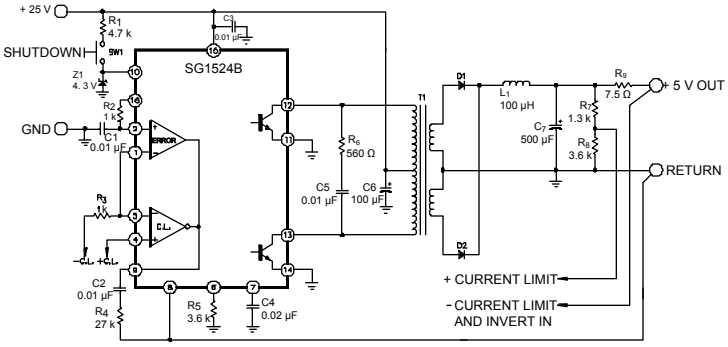

Figure 8. A Single IC 50 kHz Push-Pull Converter

The circuit illustrated in Figure 8 is a push-pull, +28 V to +5 V converter operating at 50 kHz. The power supply is unique in that the only active component is the SG1524B regulating pulse width modulator; the only other semiconductors required are diodes. The DC-coupled push-pull configuration was chosen because it is most sensitive to PWM controller anomalies which cause side-to-side imbalance. These include start-up problems such as output from only one driver until the toggle flip-flop begins to be correctly clocked by the oscillator. During normal operation, side-to-side imbalance of volt-second product due to unequal propagation delays in the IC can cause the onset of sore saturation. Finally, as outlined earlier, when the digital Shutdown control is activated, double-pulse sequencing can drive the excursion of the transformer core flux past the saturation knee of the BH loop.

Capacitor C3 acts as a high-frequency bypass for the IC supply line, while C6 is the high current reservoir for the power stage. The oscillator is set for 100 kHz with C4 and R5. When divided by two by the action of the internal toggle flip-flop, this becomes 50 kHz at the power transformer. The +5 V reference is filtered against high frequency noise pick-up by R2 and C1, and applied to the non-inverting input of the error amp. The inverting input is connected to the power supply output terminals to form the negative feedback loop required for regulation. R3 minimizes the effects of input offset bias current by equalizing the source impedance seen by each error amp input terminal. Closed loop stability is provided by frequency compensation components R4 and C2, using the common technique of cancelling one of the two poles of the LC output filter with a open-loop zero in the error amplifier.[4]

In the power section of the supply, the two output transistors are used to directly drive a center-tapped transformer. A snubber network consisting of C5 and R6 modifies the inductive load line seen by each transistor. The transformer itself is wound on a small ferrite core; turns ratio is 3:1. Rectifier diodes D1 and D2 are Schottky junction devices to maximize efficiency at +5 V output. Filtering is provided by L1, wound on a permalloy powder toroid, and C7.

The improved common mode range of the current limit amp is used to good advantage here; current sensing is done directly in the output line. A foldback ratio of 7.5 to 1 is obtained with the given values R7, R8, and R9. The divider formed by R7 and R8 applies a back-bias of 1.3 V, or 6.5 times current limit threshold, when the supply output is at +5.0 V. Peak output current before onset of current limiting is 200 mA, and short-circuit current is only 25 mA. Rapid turn-off of the control circuit is accomplished by closing SW1. R1 and Z1 limit the maximum voltage applied to the Shutdown terminal to less than +5 V.

While capable of only limited output power due to thermal limitations of the 16 pin Cerdip package, the supply amply illustrates the controller ability to perform all the major control functions required both during start-up, normal regulation, and overload.

Conclusion

In the past it was often necessary to incorporate additional components around the SG1524 pulse-width modulator to enhance its capabilities, and to guard against various functional anomalies. Economically this was feasible due to the relative cost of the control device compared to the cost of the peripheral components.

With the occurrence of the usual price decline characteristic of most integrated circuits, the economic balance has shifted. Many users now pay more for the necessary support circuitry than for the SG1524 itself.

The availability of the SG1524B now gives the designer another option. In many instances costly additional support components can be eliminated and a functionally superior device may be plugged directly into an existing design, with the benefit of simplicity, greater reliability, and reduced overall cost.

References

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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