ZLAN-327

Network Clock Translators/Synchronizers Power Supply Decoupling and Layout Practices

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1.0 Introduction

This document details the recommended power supply decoupling and device layout practices for the ZL30161, ZL30162, ZL30163, ZL30165 and ZL30361, ZL30362, ZL30363, ZL30365.

2.0 Power Supply Decoupling and Layout Practices

Jitter levels on the ZL30161, ZL30162, ZL30163, ZL30165 and ZL30361, ZL30362, ZL30363, ZL30365. output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the devices should be isolated from noise on power planes connected to its power supply pins as shown in Figure 1 for the ZL30161, ZL30162, ZL30163, ZL30165 and ZL30361, ZL30362, ZL30363, ZL30365.

The following common layout practices are recommended for improved power rail noise rejection.

- Six “power islands” should be created for the device. Four of the power islands are for 3.3V power supply, two of them are for 1.8V power supply. A power island is a local copper area, separated from the main power plane by a series passive component. Its purpose is to provide improved isolation from noise on the board power planes. Ferrite beads provide additional suppression of digital switching noise generated by other integrated circuits connected to the main power planes. Ferrite beads should have high resistance of several hundreds ohms at 100MHz and should be able to handle maximum current of corresponding supply input. For instance, Murata BLM18PG471SN1 or similar ferrite bead could be used. Note that beads have some DC resistance which increases the minimum required supply voltage for the device (by about 1% for the above bead). The ferrite beads can be replaced with resistors if less stringent jitter performance is required.
- A 0.1 µF decoupling cap (ceramic X5R or X7R) must be allocated for each power pin(except pin E2) and placed as close as possible to the via connected to the power pin. The smallest available package size should be used. Each decoupling cap should be connected directly to only one power pin(except pin H9 and pin J9), and should not share vias to power or ground with other caps.
- A bulk cap of 10 µF with low ESR must be allocated for each power Island. Ceramic provides the lowest ESR but tantalum may also be acceptable. This capacitor is used to filter low frequency (up to several hundreds KHz) noise that originate from switching power supplies. The 10 µFcapacitor can be placed close to the ferrite bead or resistor. For Pin E2, a 1 µF low ESR ceramic X5R or X7R capacitor should be in parallel with the 10 µF bulk cap closed to the ferrite bead or resistor.

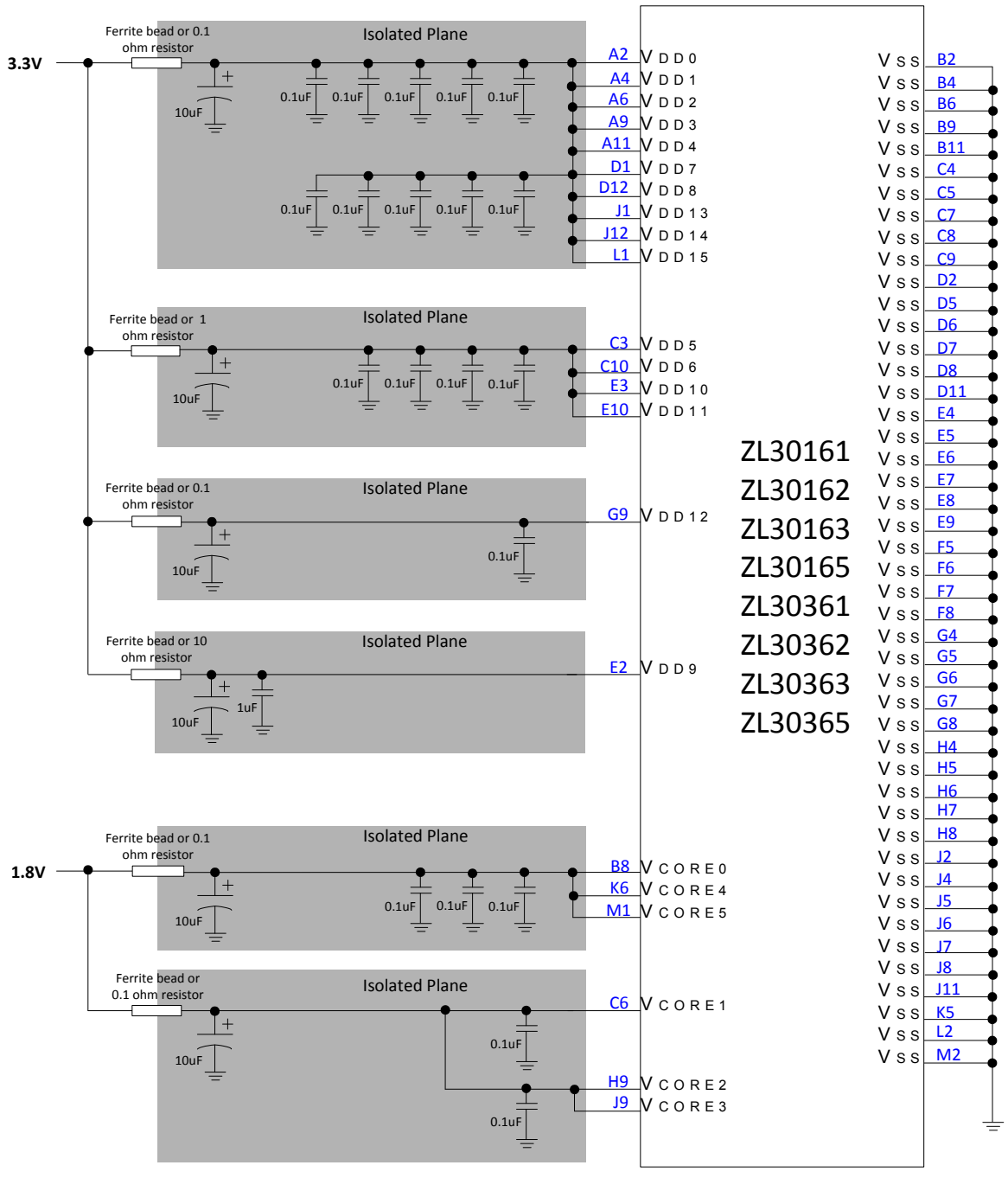

Figure 1 - Decoupling for ZL30162 and ZL30362