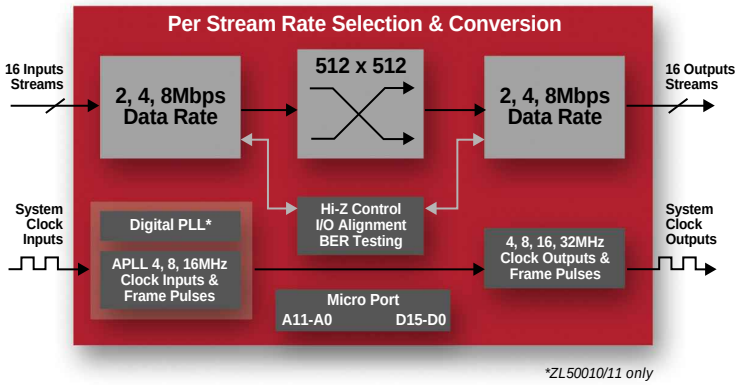
DIGITAL SWITCHES
ZL50010/11/12

ZL50010/11/12 Simplified Block Diagram



The ZL™ 50010, ZL50011 and ZL50012 digital switches (Time Slot Interchange) are designed for small-to-medium size multi-service access platforms, IP-PBXs and CPE equipment. All three devices provide 512 x 512 channels of non-blocking switching capability and per-stream programmable data rate selection. The family also delivers a full range of per-stream and per-channel programmable features as well as integrated timing options that ensure the most cost-effective route to adding functionality to network access platforms.

- The ZL50010 switch integrates an enhanced digital phase locked loop (DPLL), providing a complete digital switch and Stratum 4E compliant timing solution with holdover mode.
- The ZL50011 switch delivers digital switching and Stratum 4 timing capability to applications where holdover mode is not required.
- The ZL50012 digital switch offers a full range of per-channel and per-stream programmable features.

Applications

- Small and medium multi-service switching platforms
- IP-PBX/PBX
- Remote Access servers
- Computer telephony integration
- Digital loop carriers
- Data/voice multiplexers

At a Glance

- **Package:** 160 pin LQFP, 144 ball LBGA
- **Volume Production:** December 2002

System Design Flexibility

- Per-stream and per-channel programmable features include message mode, input delay offset, output advancement offset.
- Per-stream programmable input and output data rate selection of 2.048Mb/s, 4.096Mb/s or 8.192Mb/s to optimize bandwidth management.
- Dedicated high-impedance output control pins allow multiple buses to share streams.
- BER Pseudo-Random Binary Sequence (PRBS) to test system connectivity without external components.

Embedded Stratum 4E DPLL

- Integrated Stratum 4E DPLL ensures precise synchronization when the timing source is lost.
- Provides holdover mode with 0.07 frequency stability.
- Offers an MTIE circuit with less than 21ns per reference switch.
- Reduces component count for easier board layout and cost reduction.
- Programmable output clocks: 4.096, 8.192, 16.384, 32.768MHz.

Standards Compliant

- Telcordia GR-1244-CORE
- Telcordia GR-499-CORE
- Stratum 4 Enhanced timing standard
- IEEE-1149.1 (JTAG) standard

Complimentary Products

- MT9072, MT9076, MT92210/20, ZL50211

Customer Support

The new digital switching ICs are supported by an evaluation board, software drivers, reference design, applications notes, IBIS models and BSDL files.

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Applications

The following example represents a IP-PBX application using a centralized TDM switching architecture to route simultaneously over 500 voice calls between the local IP network to other PBXs and the PSTN.

The IP phone traffic is terminated into the TDM-to-IP processor that converts the VoIP packets to TDM Traffic. Zarlink's digital switching ICs effectively manage this traffic with the broadest range of per-stream and per-channel programmable features and integrated timing options.

A centralized TDM switching card that interfaces with devices running at different TDM rates is simplified when designing with the ZL50010/11/12 ICs. The input and output streams rate can be independently selected at 2, 4 and 8Mb/s while rate conversion allows the channels to be switched between streams. The devices also offer per-stream input delay and output advancement of channels, bits and sampling points, with respect to the TDM frame boundary. These features offer designers the flexibility required to compensate for inter stream delays caused by different trace capacitance and length of buses, thus eliminating the need for external glue logic.

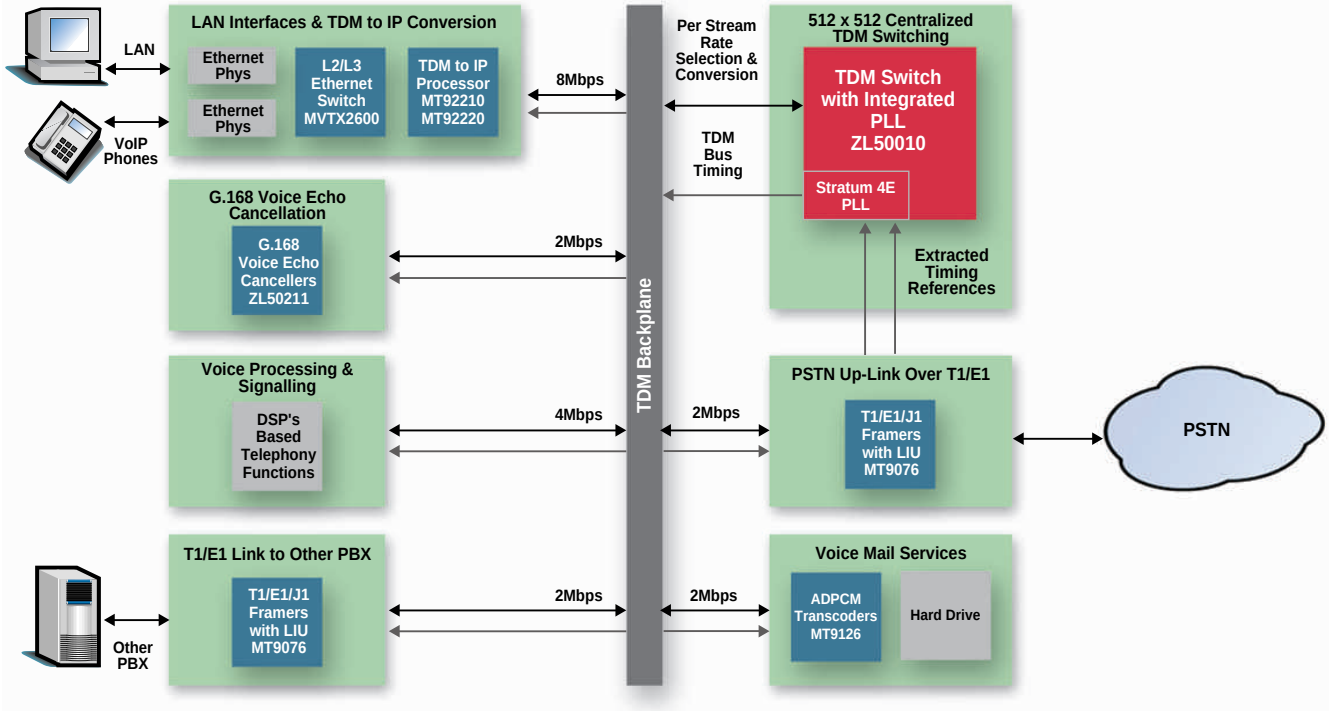
To support Quality of Service for mixed voice and data packets, such as video on TDM bus, the devices allow constant throughput delay to ensure data integrity, and per-channel message mode for testing and control. In addition, high-impedance output control authenticates that traffic is efficiently switched between streams when multiple devices are sharing the same backplane.

In applications that require transient free timing performance, the ZL50010 provides an integrated Digital PLL with holdover capabilities and time interval error correction.

When impairment affects the primary reference source from the PSTN network, the device maintains the system timing accuracy within 0.07 ppm, and automatically switches to a secondary reference source without any phase hit on the TDM bus timing.

By taking advantage of the high flexibility and integrated timing options, system OEMs can ease system design, reduce board space and complexity, and lower the Bill of Materials.

ZL50010/11/12 in "Voice Over IP" PBX Application



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