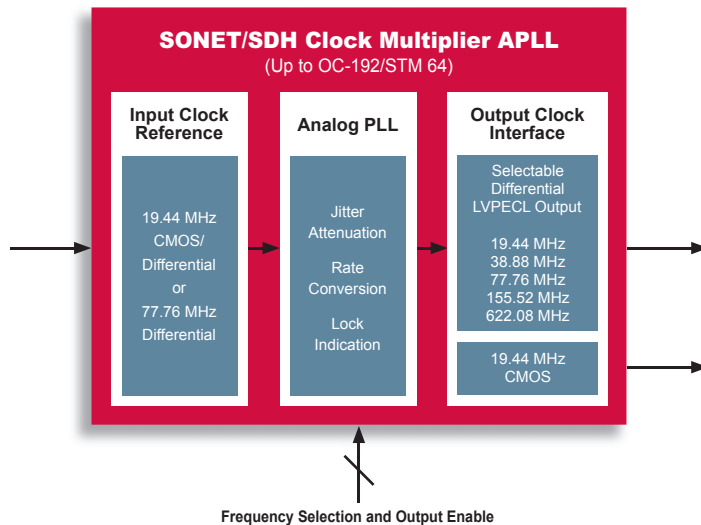




ZL30416 Simplified Block Diagram



The ZL™30416 is an analog phase locked loop (APLL) that performs jitter attenuation and rate conversion for SONET (synchronous optical network) and SDH (synchronous digital hierarchy) equipment. The APLL is specifically designed to meet the feature and performance requirements of line card applications from OC-3/STM-1 up to OC-192/STM-64.

The ZL30416 accepts a single-ended CMOS reference at 19.44 MHz or a differential LVDS, LVPECL, or CML reference at 19.44 or 77.76 MHz, and generates a frequency selectable LVPECL output clock, as well as a 19.44 MHz CMOS output clock. Zarlink's ZL30416 seamlessly interfaces with framers, mappers and SERDES devices eliminating external circuitry to save cost, board space and design resources. With ultra-low jitter, the ZL30416 provides designers with confidence in meeting Telcordia and ITU-T specifications.

High Performance from OC-3 to OC-192

- Ultra-low jitter generation of 0.52 ps rms (50 kHz to 80 MHz) surpasses world-wide system requirements
- Surpasses Telcordia GR-253-CORE, from OC-1 to OC-192 rates
- Surpasses ITU-T G.813 options 1 and 2, from STM-1 to STM-64 rates

Design Flexibility

- Accepts a single-ended CMOS reference at 19.44 MHz or a differential LVDS, LVPECL, or CML reference at 19.44 MHz or 77.76 MHz
- Differential LVPECL output clock is frequency selectable to 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, or 622.08 MHz
- Single-ended CMOS output clock at 19.44 MHz

Simplifies Design

- Seamlessly interfaces to framers, mappers and SERDES
- LVPECL output clock eliminates need for external translation circuitry, saving board space, cost and design effort
- Input/output frequencies are selectable through the control pins
- Does not require external crystal oscillator

Applications

- SONET/SDH line cards
- SONET/SDH timing cards

Packaging and Availability

- Package: 64-ball CABGA (8 mm x 8 mm)
- Available now in production quantities

Complementary Products

- ZL30106 SONET/SDH/PDH Network Interface DPLL
- ZL30407 SONET/SDH Network Element Digital PLL

Customer Support

The ZL30416 is supported by a customer evaluation board (ZLE30416) and Zarlink's network of field application and design engineers.

ZL30416

SONET/SDH CLOCK MULTIPLIER ANALOG PLL

VOICE/DATA



Ultra-Low Jitter, Frequency Selectable APLL Reduces Cost, Simplifies Design

The diagram below demonstrates how the outputs of the ZL30416 can be used to drive framers, mappers and SERDES devices in OC-3/STM-1 up to OC-192/STM-64 line card applications.

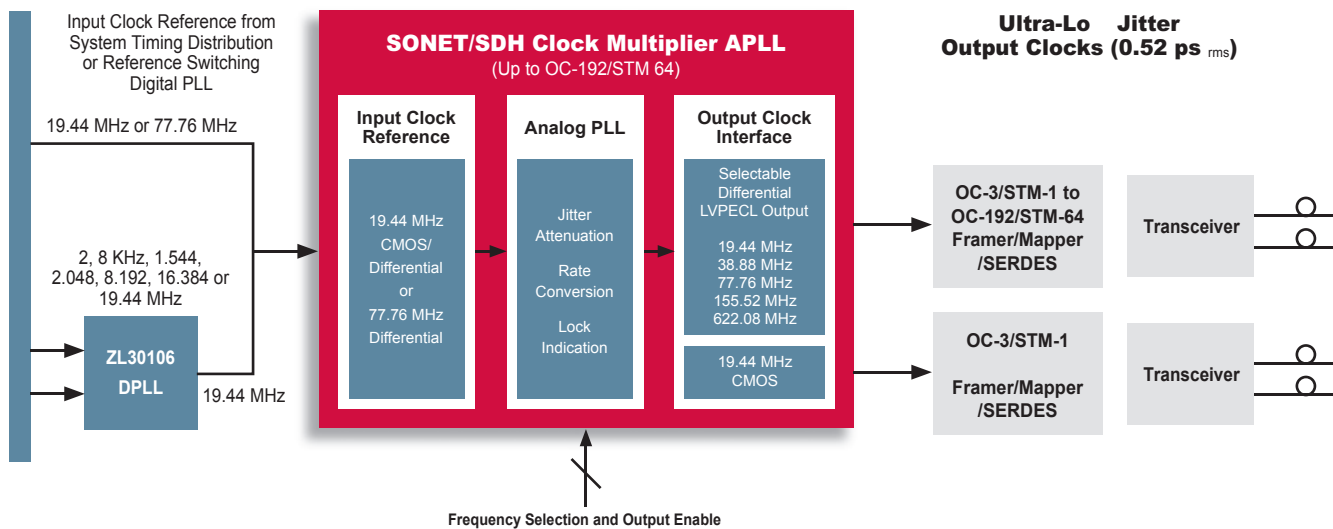
In this application the ZL30416 accepts a single input reference (19.44 MHz or 77.76 MHz) directly from the timing card represented by the system timing distribution bus. When reference switching or advanced timing functionality are required on the line card, a digital PLL such as Zarlink's ZL30106 is used to provide the reference. The ZL30416 performs jitter attenuation and provides one LVPECL output clock that is frequency selectable to 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz or 622.08 MHz, and one CMOS output clock at 19.44 MHz.

The ability to support multiple output clock frequencies allows the device to be used in any SONET/SDH system. Frequencies are selected using the control pins, allowing designers to use the ZL30416 in multiple line cards without changing the layout.

Since the ZL30416 is able to support LVPECL output clocks up to 622.08 MHz, no external circuitry is required to interface to framers, mappers, SERDES, or other surrounding devices. Eliminating external translation circuitry reduces bill of materials cost, board space and design time.

By simplifying the design of high-performance clocks, Zarlink enables OEMs to focus resources on the design of value-added features for the line card.

ZL30416 SONET/SDH Line Card Application



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