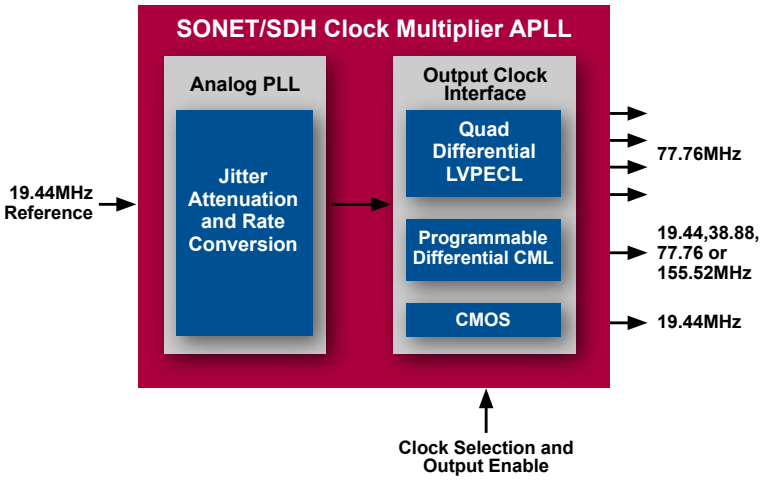
ZL30406

SONET/SDH CLOCK MULITPLIER APLL

VOICE/DATA

ZL30406 Simplified Block Diagram



The ZL™30406 is the world's first SONET (synchronous optical network) and SDH (synchronous digital hierarchy) clock multiplier analog phase locked loop (APLL) to provide six output clocks from a single device with jitter performance that surpasses OC-48 and STM-16 system requirements. This unique level of integration and performance allows designers of SONET and SDH networking equipment to meet stringent timing requirements.

The ZL30406 APLL accepts a single reference input at 19.44MHz and generates ultra-low jitter clock outputs in compliance with ITU-T and Telcordia jitter generation requirements for SONET/SDH equipment. With multiple clocks supporting CMOS, CML and LVPECL outputs, the ZL30406 eliminates external circuitry to save cost, board space and design resource requirements.

The ZL30406 positions Zarlink as the only supplier with both analog and digital PLLs enabling flexible and feature rich solutions for SONET/SDH applications.

Applications

- SONET/SDH Line Cards
- Network element timing cards

At a Glance

Package: 64-pin TQFP
Volume Production: Now

High Performance

- Ultra-low jitter generation of 0.46 ps $_{(rms)}$ surpasses world-wide system requirements.
- Meets Telcordia GR-253-CORE, from OC-1 to OC-48 rates.
- Meets ITU-T G.813 options 1 & 2, from STM-1 to STM-16 rates.

Multiple Clock Outputs

- Provides four differential LVPECL output clocks at 77.76MHz.
- Differential CML output clock programmable to 19.44MHz, 38.88MHz, 77.76 MHz, and 155.52MHz.
- Single-ended CMOS clock at 19.44MHz.

Simplifies Design

- Enables glueless interface to SONET/SDH devices such as framers, mappers and SERDES.
- Multiple LVPECL output clocks eliminate external circuitry for level conversion and fanout, saving board space, cost and design effort.
- Simultaneously generates up to three different output frequencies from a standard CMOS reference input at 19.44 MHz.
- Independent power down control of all output clocks optimizes power consumption.

Complementary Products

- MT9046 T1/E1 System Synchronizer Digital PLL
- MT90401 SONET/SDH System Synchronizer Digital PLL
- ZL30407 SONET/SDH Network Element Digital PLL

Customer Support

The ZL30406 is supported by a customer evaluation board (ZLE30406) and Zarlink's network of field application and design engineers.

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Applications

The following diagram represents a generic SONET/SDH Line Card application where the output clocks of the ZL30406 are used to drive framers, mappers and SERDES at various standard clock frequencies.

In this application the ZL30406 accepts a single 19.44MHz CMOS reference input directly from the timing card represented by the system timing distribution bus. When reference switching or advanced timing functionality are required on the line card, a digital PLL such as Zarlink's MT9046 is used to provide the reference.

The ZL30406 filters jitter and multiplies the reference to common SONET/SDH frequencies available on six outputs. With a combination of fixed and programmable outputs, the device can simultaneously produce up to three different clock frequencies.

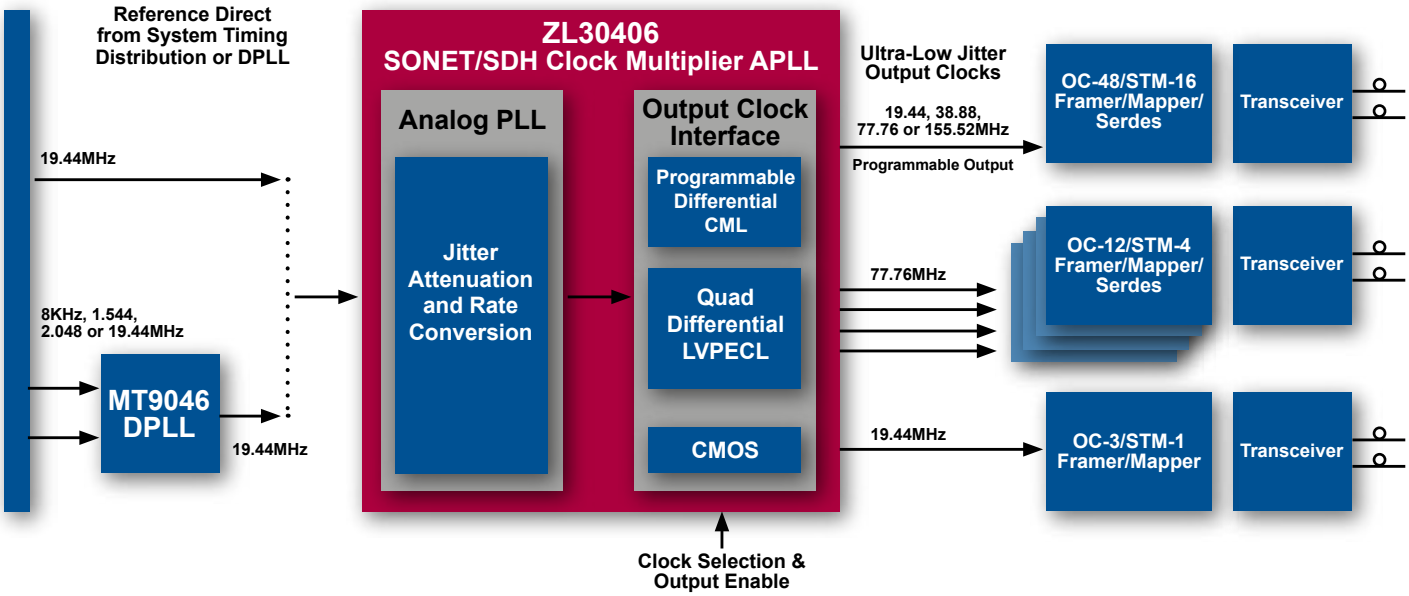
Each output clock of the ZL30406 can be individuallyenabled or disabled, allowing designers to support the number of clocks required for specific system requirements. Un-needed clocks can be powered down optimizing power consumption.

The ability to support multiple, individually controlled output clocks substantially eases design compared to alternative solutions. The four LVLECL differential output clocks at 77.76 MHz interface directly to SONET/SDH devices eliminating external circuitry for level translation, fanout and enable/ disable control. This reduces the bill of materials as well as the design effort required to consider and provision for the impact of this circuitry on clock signal and jitter performance.

The ZL30406 also reduces board space compared to VCO-based modules by up to 75 percent, and simplifies design versus discrete PLL implementations.

By simplifying the design of high-performance clocks, Zarlink enables OEMs to focus resources on the design of value-added features for the line card.

Application Diagram



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