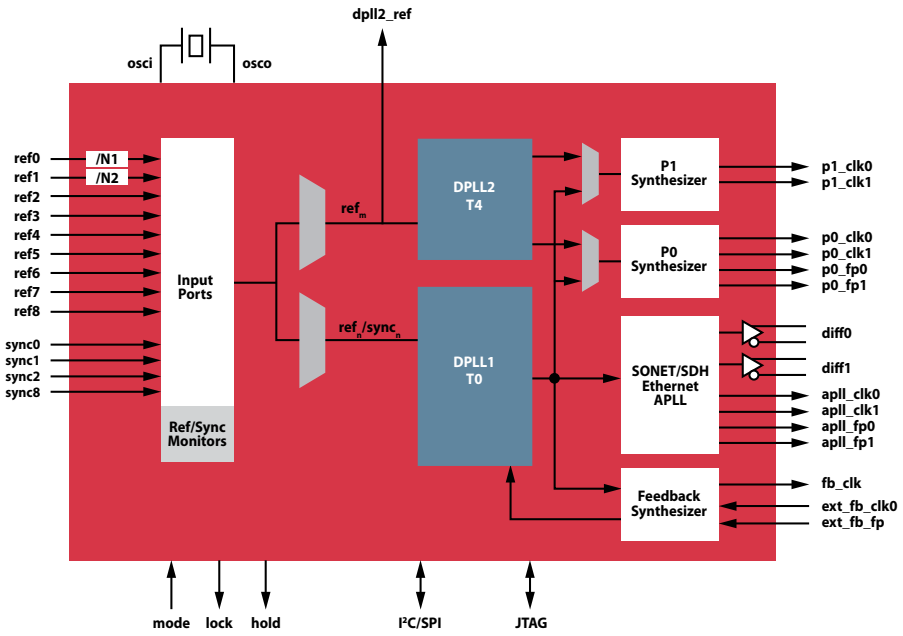
SyncE SONET/SDH G.8262/Stratum3 System Synchronizer/SETS **ZL30143**

PRODUCT PREVIEW

Zarlink's ZL30143 phase locked loop (PLL) is part of the Company's market-leading portfolio of single-chip Synchronous Ethernet solutions. The highly integrated products allow manufacturers to easily upgrade or design networking equipment that supports accurate end-to-end transmission of voice, video, data and mobile applications and services over IP-based wired and wireless networks.

Targeting central timing card applications in carrier-grade networking equipment, the ZL30143 chip integrates analog and digital phase locked loops (APLL/DPLL). The device provides two independent DPLLs for applications that require independent transmit and receive timing paths. Delivering high performance at a considerably lower cost versus the competition, the ZL30143 product requires only an inexpensive temperature controlled crystal oscillator (TCXO) to achieve full compliance with ITU-T Recommendation G.8262.

Zarlink is the only supplier offering single-chip Synchronous Ethernet solutions in full compliance with all relevant synchronization over packet standards.



Applications

- ITU-T G.8262 system timing cards that support 1 GE and 10 GE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 3 System Timing Cards
- System Timing Cards which support ITU-T G.781 SETS (SDH Equipment Timing Source)

Highly Integrated SyncE Solution for Timing Cards

- Supports the requirements of ITU-T G.8262 for synchronous Ethernet equipment slave clocks (EEC option 1 and 2)
- Supports the requirements of Telcordia GR-1244 Stratum 3 and GR-253, ITU-T G.813, and G.781 SETS
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
- Meets the SONET/SDH jitter generation requirements up to OC-48/STM-16
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Supports composite clock inputs (64 kHz, 64 kHz + 8 kHz, 64 kHz + 8 kHz + 400 Hz)
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Gigabit Ethernet PHYs
- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz
- Generates several styles of telecom frame pulses with selectable pulse width, polarity and frequency
- Provides two DPLLs which are independently configurable through a serial interface
- Internal state machine automatically controls mode of operation (free-run, locked, holdover)
- Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
- Provides automatic reference switching and holdover during loss of reference input
- Supports master/slave configuration and dynamic input to output delay compensation for AdvancedTCA
- Configurable input to output delay and output to output phase alignment

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ZL30143 SyncE SONET/SDH G.8262/Stratum3 System Synchronizer/SETS

APPLICATION

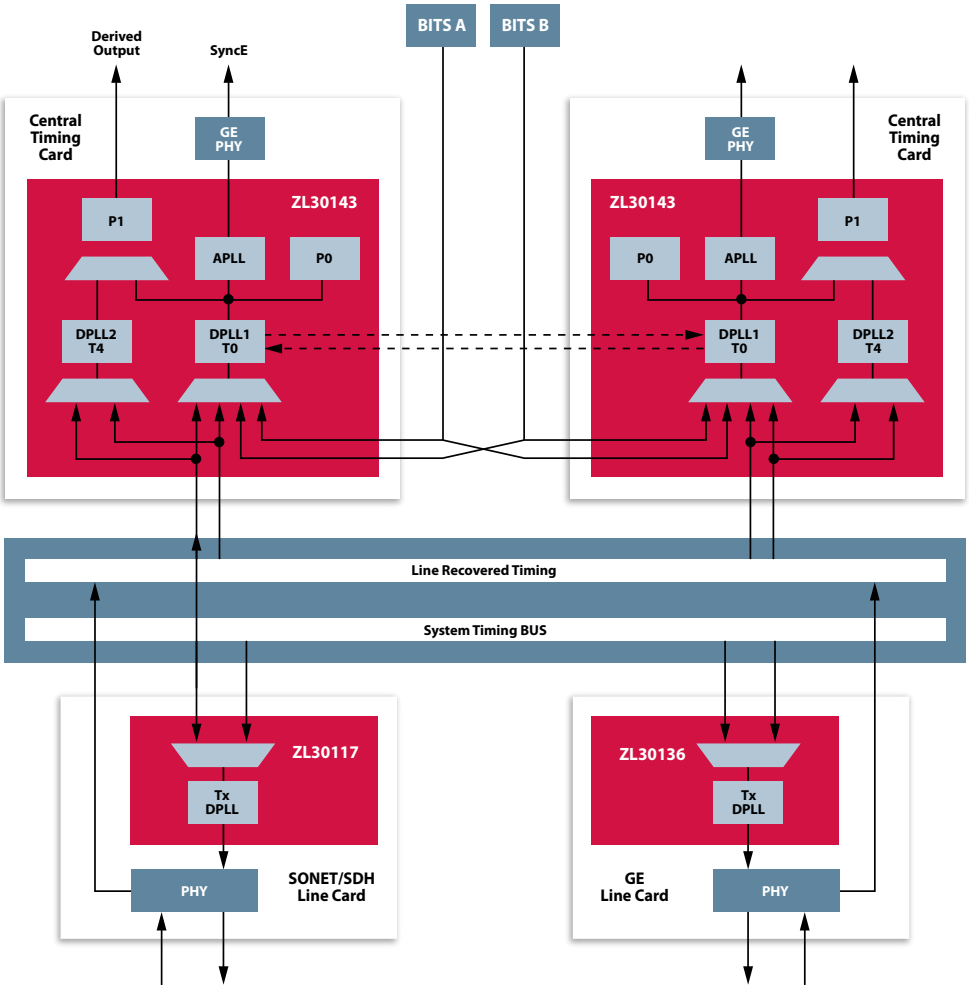
Timing Cards in Carrier-Grade Network Equipment

The ZL30143 System Synchronizer and SETS device is a highly integrated device that provides all of the functionality that is required for a central timing card in carrier grade network equipment. The basic functions of a central timing card include:

- Input reference monitoring for both frequency accuracy and phase irregularities
- Automatic input reference selection
- Support of both external timing and line timing modes
- Hitless reference switching
- Wander and jitter filtering
- Master/slave crossover for minimizing phase alignment between redundant timing cards
- Independent derived output timing path for support of the SETS functionality

In a typical application as illustrated below, the main timing path uses DPLL1 to synchronize to either an external BITS source or to a recovered line timed source. DPLL1 monitors all references and automatically selects the best available reference based on configurable priority and revertive properties. DPLL1 provides the wander filtering function and the P0 synthesizer generates a jitter filtered clock and frame pulse for the system timing bus which supplies all line cards with a common timing reference.

The APLL is used to generate a reference clock for an Ethernet PHY which can be used to synchronize remote equipment. A derived output timing path using DPLL2 is available to support the SETS function. In this case DPLL2 uses a filter above 10 Hz to prevent it from filtering wander.



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