SONET/SDH TIMING CARD SYNCHRONIZER **ZL30116/21**

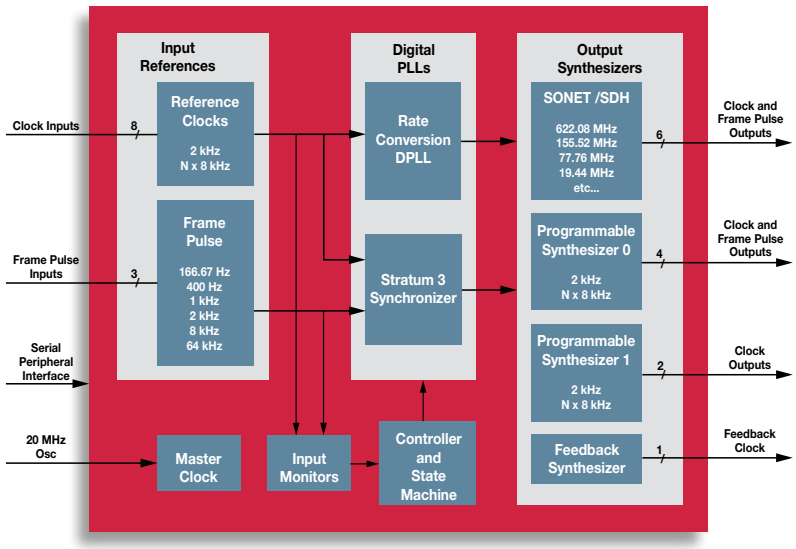
PRODUCT PREVIEW

Zarlink's ZL30116 and ZL30121 chips are SONET Stratum 3/G.813 compliant system clock management device for AdvancedTCA™ systems, multi-service provisioning and edge platforms operating at up to OC-192/STM-64 speeds.

Highly integrated and compact devices, the ZL30116/121 PLLs combine the network synchronization capabilities of a digital PLL with the jitter performance of an analog PLL. The ZL30116 and ZL30121 are pin compatible and software compatible devices differentiated by jitter performance. With ultra-low jitter performance of less than 1ps the ZL30116 can be used in applications up to OC-192/STM-64. The ZL30121 limits jitter to less than 3ps and can be used for applications up to OC-12/STM-16. The ZL30116/121 PLLs deliver all of the clocks and clock formatting required to allow existing SONET/SDH infrastructures to carry new Ethernet, VoIP and Fiber Channel services.

The ZL30116/121 PLLs integrate SONET Stratum 3/G.813 capabilities including an integrated rate conversion PLL, master/slave redundancy functions, ultra-low jitter SONET/SDH clock synthesis, programmable clock synthesis and clock formatting in a single chip measuring just 9 x 9 mm.

ZL30116/21 Simplified Block Diagram



Applications

- AdvancedTCA™ systems
- Multi-Service Edge Switches and Routers
- Multi-Service Provisioning Platforms
- Add-Drop Multiplexers
- Wireless base stations
- DSLAM & next-generation DLCs
- Core routers

Integrated Chips for SONET/SDH Timing Cards

- Pin compatible and software compatible single-chip devices integrate network synchronization functions of a DPLL with jitter generation of an APLL
- Meets GR-253-CORE SONET Stratum 3 and ITU-T G.813 requirements
  - ZL30116 meets jitter requirements up to OC-192/STM-64
  - ZL30121 meets jitter requirements up to OC-12/STM-16
- Provides two independently configurable DPLLs:
  - DPLL1 provides all features for generating SONET/SDH compliant clocks
  - DPLL2 generates independent, general purpose clocks
- Supports master/slave clock redundancy configurations
- Programmable phase delay adjustment compensates for static delays
- Optional external feedback path provides dynamic delay compensation
- Operates in free-run, normal and holdover modes and provides automatic hitless reference switching
- Eight reference inputs supporting clock frequencies in any multiple of 8 kHz up to 77.76 MHz and 2 kHz
- Selectable output clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz) eliminate need for external dividers & clock multiplying DPLLs
- Programmable output synthesizers generate clock frequencies from any multiple of 8 kHz up to 77.76 MHz in addition to 2 kHz
- Programmable frame pulse formatter replaces CPLD or FPGA gates

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ZL30116/21 SONET/SDH TIMING CARD SYNCHRONIZER

APPLICATION

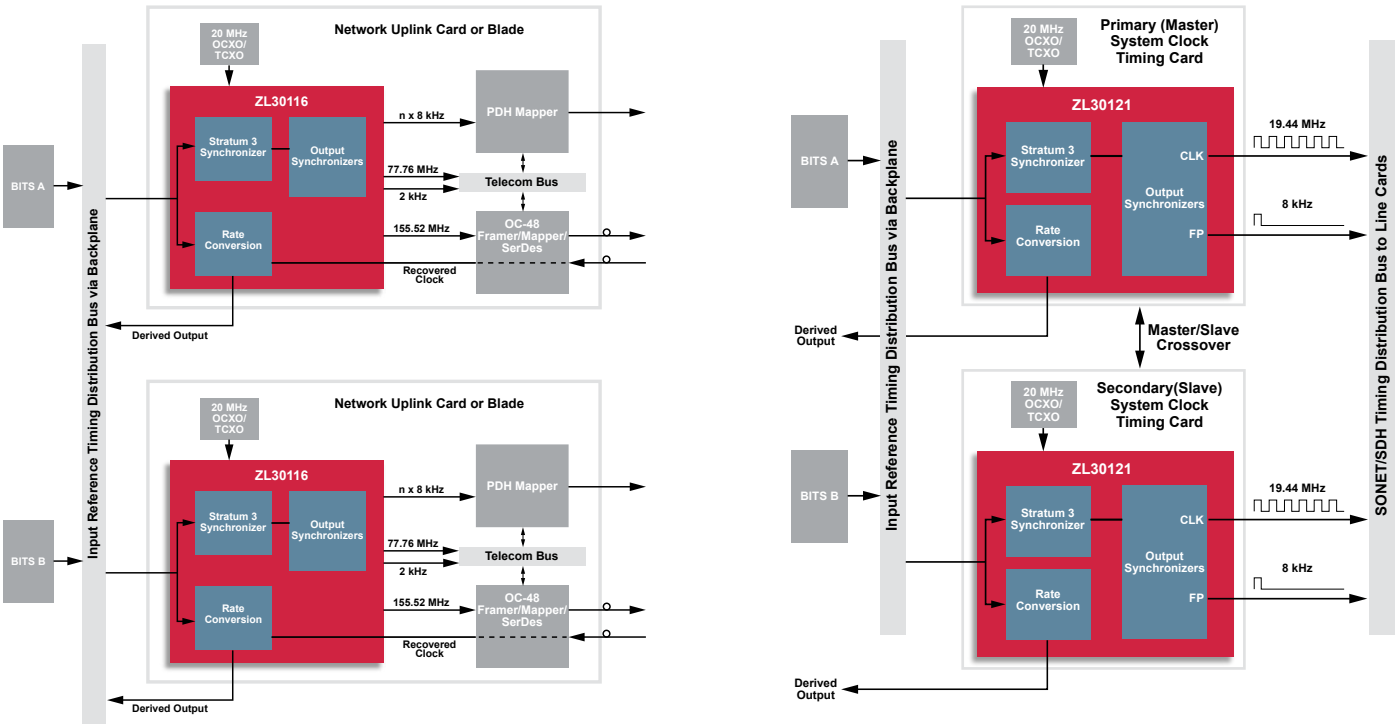
SONET/SDH Timing Card Synchronization

Zarlink's ZL30116 and ZL30121 are compact, highly integrated SONET Stratum 3/G.813 compliant system synchronizers and clock management devices for next-generation multi-service provisioning and edge products. Incorporating digital and analog PLLs, a single chip manages SONET/SDH network synchronization functions up to OC-192/STM-64 speeds. The ZL30116 and ZL30121 are pin compatible and software compatible devices differentiated by jitter performance. With ultra-low jitter performance of less than 1ps the ZL30116 can be used in applications up to OC-192/STM-64. The ZL30121 limits jitter to less than 3ps and can be used for applications up to OC-12/STM-16. Competing two-chip or module approaches are more than twice the size of the ZL30116/121 and require external devices to manage high-speed network timing.

As illustrated below, the ZL30116 can be used as the sole timing device for a blade or network uplink card operating at speeds up to OC-192/STM-64. The ZL30116 provides the network synchronization functions necessary to comply with SONET Stratum 3/G.813 and the clocks and jitter performance to time OC-192/STM-64 uplinks. The ZL30116 can be substituted with a ZL30121 for uplink cards requiring jitter performance up to OC-12/STM-16.

The ZL30121 is shown on the primary and secondary system clock timing cards in a system implementing a centralized timing architecture. In this configuration two ZL30121 devices can be connected in a redundant (master/slave) configuration. A dedicated crossover link, combined with programmable phase delay adjustment, allows for very close phase alignment between master and slave output clocks.

With leading integration, flexibility, programmability and performance, the device's network synchronization functionality and ultra-low jitter SONET/SDH output clocks deliver a complete single-chip timing solution.



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