SEGMENTATION & REASSEMBLY (SAR)

PRODUCT OVERVIEW

The MT90520 and MT90528 are AAL1 (ATM Adaptation Layer 1) segmentation and reassembly (SAR) devices designed to optimize performance and cost efficiency of TDM-to-ATM conversion applications. The devices are the first AAL1 SARs with on-chip per-port PLLs that provide a total clock solution. This, combined with low latency performance, eliminates up to six components at the system level, thereby delivering dramatic savings in board space and cost.

The MT90528 supports simultaneous processing of up to 896 bi-directional VC (virtual channel) connections through 28 independent DS1/T1/E1 ports. The device is ideal for digital loop carriers and multi-service WAN switches.

The MT90520 is an 8-port solution ideal for equipment like IADs (integrated access devices), which require low port count interfaces. The device supports 256 bi-directional VC connections.

Applications

- ATM edge switches
- Multi-service switches
- Carrier-class gateways
- Broadband digital loop carriers
- ATM voice and media gateways
- Integrated access devices

Highly Integrated Processors Reduce Board Space & System Cost

- On-chip per-port PLLs synchronize inputs to different network clocks, eliminating up to four external framers, in UDT (unstructured data transfer) mode
- Integrated SRAM buffers cell payloads on chip, eliminating external memory requirements in UDT mode
- Independent inputs programmable to UDT, SDT (structured data transfer), E1 or T1 modes allows multiple system specifications to be met without additional components
- Minimal latency reduces requirements for external VECs (voice echo cancellers)

Enhances Quality of Service

- Per-port clock management for synchronous, adaptive, or SRTS operation optimizes network synchronization
- Reduces processing delay to less than 375 us from TDM to ATM, and less than CDV+250 us ATM to TDM

Flexible

- Support for UDT, unstructured CES (circuit emulation services) and structured CES with CAS data transfer modes
- Flexible aggregation capabilities, Nx64Kbps, for any combination of CES service
- Supports UTOPIA level 1 and level 2, of 8- or 16-bit mode at clock rates up to 52Mhz
- Offers ATM, PHY and multi-PHY modes
- Standard Motorola/Intel microprocessor interface for multiplexed or individual address and data lines
- Master and slave TDM backplane bus clock operation
- TDM bus supports bi-directional serial streams at 1.544, 2.048 or 4.096 MHz

Customer Support

The MT90520 and MT90528 are supported with reference designs and application programming interface software, supplied with software drivers and source code.

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SEGMENTATION & REASSEMBLY (SAR) APPLICATION

Structured & Unstructured AAL1 Circuit Emulation Services in ATM Edge Switch Application

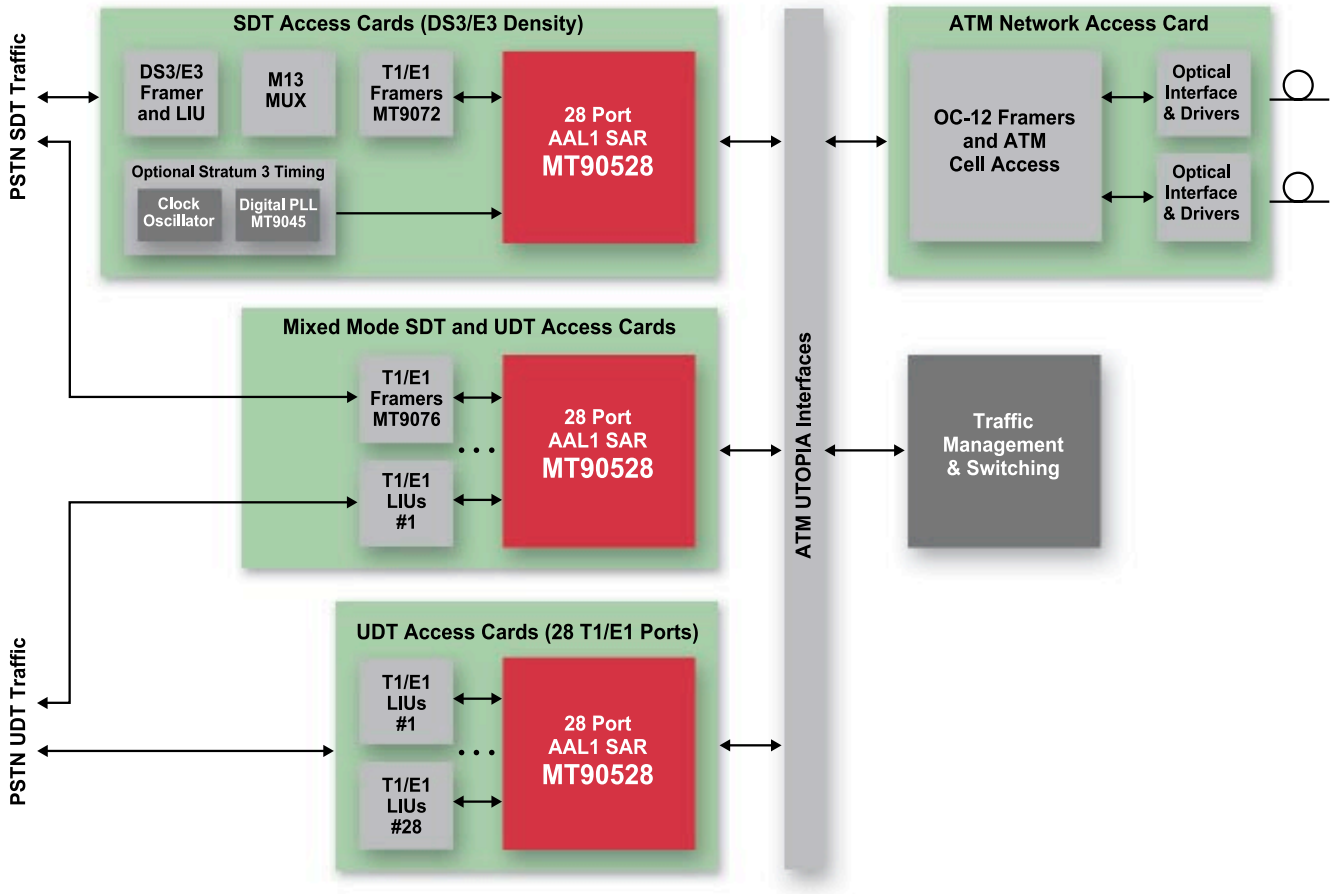
The following diagram illustrates an ATM edge switch, which serves as a high-bandwidth interface for providing ATM network access to various types of voice and data traffic. In this application, where large volumes of voice and data are exchanged, it is typical to use UDT (also called unstructured CES) mode for TDM-to-ATM data conversion.

With an extremely high level of integration, the MT90528 provides the industry's most effective processor for UDT operation. As shown, the MT90528 receives CBR (constant bit rate) traffic from 28 independent DS1/E1 ports operating at 1.544/2.048 Mbps and converts it to 53-byte cells for transport over ATM networks.

The MT90528 is a complete TDM-to-ATM processor solution, integrating the TX/segmentation, RX/Segmentation, clock module, TX SAR engine, RX SAR engine, microprocessor interface, and external memory controller.

In addition, on-chip per-port PLLs enhances UDT performance by enabling each input to be synchronized to a different network clock. Able to support SRTS, adaptive, or synchronous clock modes, the device eliminates the requirement for up to four external framers. This results in a simplified design, allowing the device to connect directly to the DS1 or E1 LIUs on the TDM side.

The device also features on-chip SRAM, which enables cell payloads assembled in UDT operation to be buffered on chip. This allows efficient design by eliminating external memory requirements for UDT applications. Using the MT90528 eliminates up to six components from the system-level BOM, thereby providing dramatic savings in board space and system-level cost.



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