ZARLINK SEMICONDUCTOR

# Guide to New Designs

## Enabling 5.0 V QSLAC™ Device (Am79Qxxx) to 3.3 V QLSLAC™ Device (Le58QLxxx) Transitions

### Application Note

*This document is a guide for new linecard designs using Zarlink's QSLAC™ device. The guide offers design suggestions to enable a smooth transition from the QSLAC device to the newer QLSLAC™ device. One objective of this document is to provide guidance for developing a design that is fully software compatible for both SLAC™ devices with a minimal number of hardware modifications. Considerations are given for linecard designs using Zarlink's solid state Subscriber Line Interface Circuits (SLIC) device as well as transformer SLIC device designs.*

## 1.0 COMPARISON BETWEEN QSLAC™ DEVICE AND QLSLAC™ DEVICES

The QLSLAC device was designed to be a lower voltage, pin and package compatible version of the QSLAC device. As such, the QLSLAC device is virtually identical to the QSLAC device. However the QLSLAC device uses a +3.3 V power supply, compared to the +5.0 V power supply of the QSLAC device. The lower voltage requirement results in a few other minor differences between the two devices.

### 1.1 Device Similarities

Internally, both SLAC devices use the same Canonical Signed Digit (CSD) based DSP. Each has the same transmission filters with the same filter structure and sample timing. Each is equipped with the same programmable supervision capability, such as debounce timers and software thresholds to operate on signaling data.

The microprocessor commands for programming the QLSLAC device remain the same, as do the microprocessor interface (MPI) timing requirements. Besides being pin compatible, all digital inputs for both SLAC devices are 5.0 V tolerant and have the same logic high ($V_{OH}$) and low ($V_{OL}$) threshold levels. Each SLAC requires a Frame Synchronization (FS) pulse train of 8 kHz to be applied to the FS pin, which identifies time slot 0 of the system's PCM frame.

### 1.2 Device Differences

The QLSLAC device has different digital and analog power supply requirements as well as a different maximum voltage at the digital outputs. The substrate of the QSLAC device is connected to VCCA and VCCD, whereas the substrate of the QLSLAC device is connected to AGND and DGND. This means that AGND and DGND must have a very low impedance connection between the two pins. The QLSLAC device can tolerate a voltage difference between AGND and DGND of 10 mV, compared to VCCA and VCCD which can tolerate as much as 50 mV difference. The reverse is true of the QSLAC device.

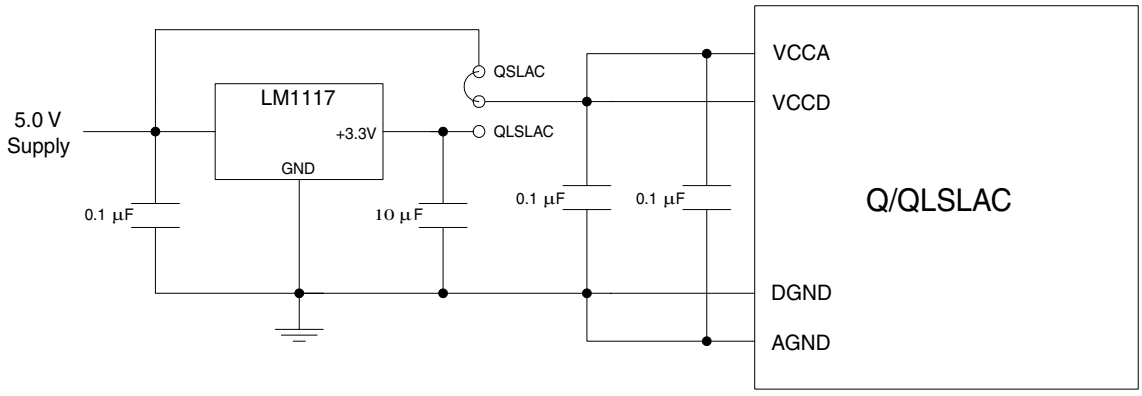
Unlike the QSLAC device, the QLSLAC device has hysteresis on the digital inputs for improved noise immunity. With the low power device, more of the circuit is left running in the low power mode (LPM), because the QLSLAC device has inherently less dynamic digital power consumption. This enables the QLSLAC device to be programmed at full speed even when the LPM bit is set to 1. The internal reference voltage, $V_{REF}$, has decreased from 2.1 volts for the QSLAC device to 1.5 volts for the QLSLAC device. The difference in the $V_{REF}$ voltage should not directly effect a design unless $V_{REF}$ is used as a reference voltage externally to the SLAC device. In addition, the $V_{OUT}$ analog output range is decreased from ±1.585 $V_{PK}$ to ±1.02 $V_{PK}$. This range difference requires modifications to the SLIC circuit to compensate for receive signal levels. For the QLSLAC device there is a default input analog gain of -3.82dB which compensates for the fact that the input analog range is the same.

## 2.0 POWER SUPPLY CONSIDERATIONS

The QSLAC device requires a 5.0 V power supply for the digital and analog VCC within a tolerance of ±5%. This 5.0 V supply should be able to provide at least 55 mA of current per QSLAC device. In contrast, the QLSLAC device requires a 3.3 V (±5%) power supply for VCCA and VCCD, and should also be able to source 55 mA of current per device. Some back planes may have both 5.0 V and 3.3 V supplies available, in which case a simple jumper would give the line card the necessary flexibility to convert from the QSLAC device to the QLSLAC device.

In cases where only a 5.0 V supply is available, a single design can accommodate both the QSLAC device and QLSLAC device if a 5.0 V to 3.3 V regulator plus a jumper are included. Figure 1 shows a schematic of the DC-to-DC voltage regulator, jumper, and SLAC device. Note that the design should have a low impedance connection between AGND and DGND and between VCCA and VCCD in order for the design to accommodate each SLAC device.

**Figure 1. Powering the QSLAC™ Device or QLSLAC™ Device**




One example of such a voltage regulator is National Semiconductor Corp.'s LM1117-3.3 (www.national.com; DS100919), which costs $0.32 per unit, and can source as much as 800 mA of current. A single LM1117 would be sufficient to handle a 32 channel line card at $0.01 per line. Other possible voltage regulators include Analog Devices Inc.'s ADP3335 (www.analog.com; Rev 0, 04/00), National Semiconductor Corp.'s LM2931 (www.national.com; DS005254), and Maxim Integrated Product's MAX8867 (www.maxim-ic.com; 19-1302, Rev 2, 03/01). Most of these voltage regulators require at least 10 µF of capacitance at the output. The LM1117, for instance, requires at least a 10 µF tantalum capacitor with low equivalent series resistance (ESR). Kemet Corporation (www.kemet.com, F-3102F-TA) supplies tantalum capacitors that can be used in this type of application.

If only a 3.3 V power supply is available, a 3.3 V to 5.0 V regulator would be necessary to power the QSLAC device before switching to the QLSLAC device. Also, the regulator's 5.0 V output would likely be necessary to power a Zarlink SLIC device or possibly operational amplifiers used in a transformer SLIC device design. If a 3.3 V to 5.0 V regulator is needed, the output of the regulator should be capable of supplying the QSLAC device plus additional current budget required for the SLIC device's VCC.

## 3.0 SUBSCRIBER LINE INTERFACE CIRCUIT CONSIDERATIONS

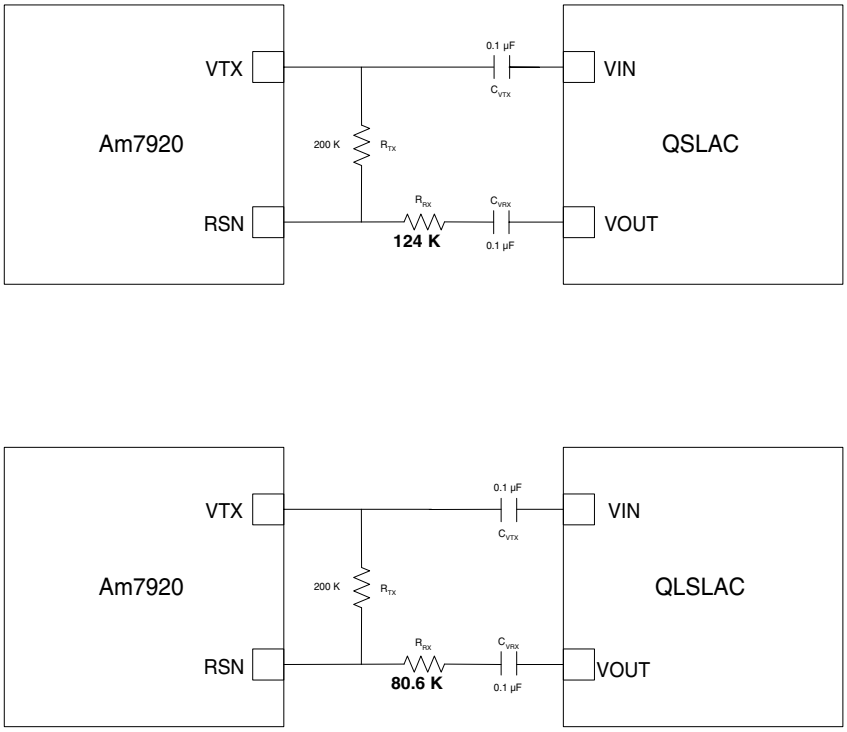
The subscriber line interface circuit could be comprised of a variety of circuit elements including Zarlink's monolithic solid state SLIC device family components, discrete circuit elements, transformers, or other solid state devices. Whether a Zarlink SLIC device plus discrete components or a transformer design is used, the behavior of the hybrid can be characterized by a set of "G parameters". The G parameters represent the SLIC device's magnitude and phase response of the 4-to-2-wire gain, the 2-to-4-wire gain, the 4-to-4-wire gain, and the 2-wire output impedance. Characterizing the SLIC device design in terms of G parameters is a useful step in designing the line card and developing the necessary filter coefficients for the SLAC device. Consult Zarlink's *WinSLAC™ Software User's Guide* (www.zarlink.com; order # 080268) for more discussion of G-parameters.

## 3.1 Design with Zarlink's Solid State SLIC Devices

Most of Zalrink's monolithic solid state SLIC devices require a 5.0 V VCC power supply. Since the QLSLAC device is a 3.3 V part, using a Zarlink SLIC device with the QLSLAC device may require that a 5.0 V supply be derived from a 3.3 V power supply. Zarlink SLIC devices are combined with external, discrete components to perform the entire SLIC device functionality. The block diagram at the top of Figure 2 is an example of a design using Zarlink's QSLAC device with the Am7920 SLIC device and external components. Note that the application network shown here does not assume default filter coefficients. In general, the 124 kΩ resistor in the receive path is referred to as the $Z_{RX}$ network, while the 200 kΩ resistor is designated as the $Z_{TX}$ network.

The G parameters of the SLIC device circuit in Figure 2 are a function of the SLIC device gains and the $Z_{RX}$ and $Z_{TX}$ network impedances. (See the appropriate SLIC device data sheet for the precise relationships). Selecting the proper components for the $Z_{RX}$ and $Z_{TX}$ networks is important for achieving appropriate transmission levels, two wire output impedance and return loss requirements. The $Z_{RX}$ impedance is inversely proportional to the 4-to-2-wire gain, which has direct bearing on the power level of the receive signal.

**Figure 2. Connection of an Am7920 SLIC Device with a QSLAC™ Device and QLSLAC™ Device**



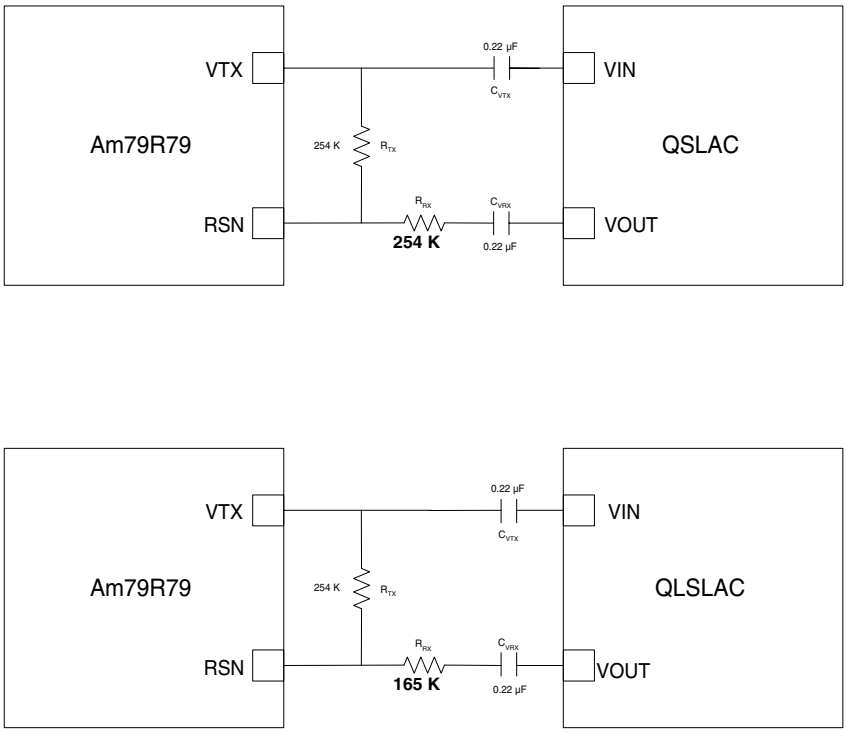

Because of differences in the Vout signal level, the receive path relative level at Tip-Ring will be affected when replacing a QSLAC device with a QLSLAC device, unless otherwise compensated. The modification with the least impact on the software/hardware design would be to scale the $Z_{RX}$ impedance by a factor of 1.02/1.584. For example, when converting the reference design of Figure 2 to a QLSLAC/Am7920 design, the relative receive level could be maintained approximately the same by substituting an 80.6 kΩ resistor in place of the 124 kΩ. The 80.6 kΩ resistor is the closest E96 standard value for providing the necessary modification to the 4-to-2-wire gain.

The design given in Figure 2 has a 0.1 µF filtering capacitor, $C_{VRX}$, in the receive path. If the impedance of the $C_{VRX}$ capacitor becomes significant with respect to $R_{RX}$ at low-end voiceband frequencies, the capacitor must be increased to maintain proper transmission performance. With a $C_{VRX}$ of 0.1µF, changing $R_{RX}$ from 124 kΩ to 80.6 kΩ moves the corner frequency from approximately 13 Hz to 20 Hz which affects the receive path gain by a mere 0.02 dB at 300 Hz. A gain error of this magnitude has minimal impact on system performance allowing $C_{VRX}$ to remain unchanged in this case. In general, if $1/(2 \bullet \Pi \bullet R_{RX} \bullet C_{VRX}) < 40$ Hz, it is recommended that the capacitor be increased to avoid gain errors at low frequency.

Many of Zarlink's solid state SLICs have nominal 2-to-4-wire gains of 0.5. The gain and drive capability of such SLICs are sufficient to over drive the analog input of the QLSLAC device. The analog input voltage range of both the QSLAC and QLSLAC devices is between ±1.584 $V_{PK}$. In order to permit the same input range, the QLSLAC device has an input voltage attenuator with a gain of 0.6438. In general, the source impedance from the SLIC must be less than 300 Ω (unless using the Le58QL063 device) in order to avoid potential cross talk issues. If the SLIC has an output attenuator of greater than 300 Ω, the design must use an Le58QL063 device. Note that protection diodes to ground and $V_{CCA}$ on the input of VIN could cause clipping of the transmit signal of the QLSLAC device at smaller voltage levels than for the QSLAC device.

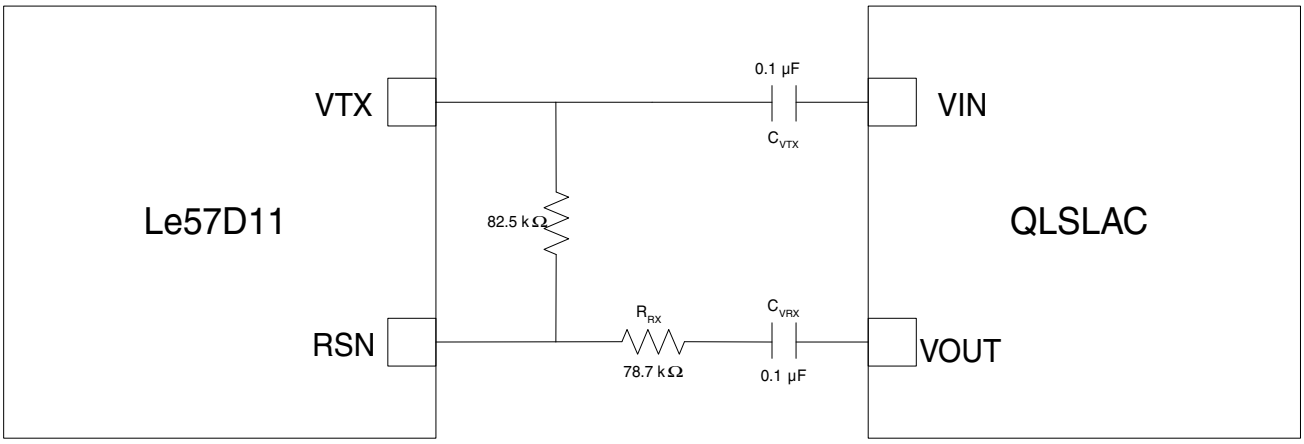
The block diagram at the bottom of Figure 2 gives an example of a QLSLAC/Am7920 device design with the receive path gain of the SLIC device circuit adjusted appropriately by modifying the $R_{RX}$ resistor. Figure 3 shows a similar example comparing a QSLAC device design with the QLSLAC device design using the Am79R79 device for an IAD application. PSpice models are available for all Zarlink SLIC devices including recommended external components values. These models can be used with the WinSLAC 2 software to generate G parameters for characterizing the gains and 2-wire input impedance. Such information is useful in choosing appropriate $Z_{RX}$ and $Z_{TX}$ networks, and in ultimately determining SLAC device filter coefficients for achieving particular design targets.

**Figure 3. Am79R79 Device with QSLAC™ Device vs. Am79R79 Device with QLSLAC™ Device**




Zarlink's new dual channel SLIC device, the Le57D11, is specifically designed with smaller 2-to-4 wire gain for use with the QLSLAC device. With the G24 gain reduced by more than 3.5 dB compared to the Am7920 and Am79R79, QLSLAC device designs using the Le57D11 device do not require an input analog voltage attenuator on VIN. This attenuator can be disabled in software by setting DGIN (bit 7) of the AISN and Analog Gain Register. Figure 4 shows an example of a QLSLAC/Le57D11 design assuming DGIN = 1. Currently, the Le57D11 device is the only Zarlink SLIC which has a 2-to-4 wire gain optimized for a non-default DGIN gain setting.

**Figure 4. Design Using Le57D11 Device with QLSLAC™ Device**




## 3.2 Design with Transformer SLIC Devices

In general, Zarlink recommends that transformer/QLSLAC designs use a turns ratio close to unity with operational amplifiers for extra 2-to-4-wire gain. Ideally, the SLIC circuit design should allow for a straightforward modification of the 2-to-4-wire and 4-to-2-wire gains when converting from the QSLAC device to the QLSLAC device. Developing a line card design using the QSLAC/QLSLAC device with a transformer involves the following steps:

1. Calculate the maximum peak voltage, given the system's power requirements for the receive path voice signal. This value is independent of the SLAC device.
2. From step 1 above, and from the maximum analog output of the QSLAC and QLSAC devices, determine the amount of gain required by the SLIC device circuit for each design. Note that the gain of the SLIC circuit with a QLSLAC device should be 3.82 dB greater than the gain with a QSLAC device.

From the peak voltage calculated in step 1, the required voltage swing of the operational amplifiers can be determined. This information is needed to determine the number of operational amplifiers (single-ended design vs. push-pull design) and power supply rails (3.3 V vs. 5.0 V). Because the termination resistance can produce up to 6 dB of loss, the voltage swing requirement of the amplifiers should allow for twice the line voltage. Note that a push-pull drive enables the operational amplifiers to swing half the total required voltage range.

Given the values from step 2, and assuming a unity gain transformer, the gain of the operational amplifier circuitry is determined for the QSLAC and QLSLAC devices. Using operational amplifiers to provide the 2-to-4-wire gain should allow for straightforward increase of the gain by appropriate modification of resistor values as long as the operational amplifiers have sufficient gain-bandwidth for the additional gain required by the QLSLAC device.

As an example, consider a system requirement of 0 dBm signal into a 900 Ω load. Typically, the maximum receive power level requires an additional 3.1 dB, corresponding to a 3.1dBm received signal, or 1.91 $V_{PK}$ at Tip-Ring. Due to termination loss and potential loss in the transformer, the actual required voltage swing would be approximately ±3.82 V. This could be met using two 5.0 V operational amplifiers in a push-pull design. On the other hand, a system requirement of –7 dBm into a 600 Ω load would need a maximum voltage swing of 1.4 $V_{PK}$. In this case, extra 2-to-4-wire gain would be unnecessary with the QSLAC device, however, the analog output of the QLSLAC device would still require a boost. The smaller voltage swing would allow single-ended operational amplifier designs with a 3.3 V supply rail.

If the system requires sufficient amount of loss that both the QSLAC and QLSLAC devices can be used to directly drive a transformer, a single SLIC device circuit could be used with different SLAC device coefficients. Alternatively, the software could be left unchanged if the transformer circuit includes op amps whose gains could be adjusted for conversion to the QLSLAC device.

Zarlink can provide PSPICE models of transformer/operational amplifier SLIC circuits that can be used for generating G parameters. See Zarlink's *Transformer Interface Requirements Application Note*,

(www.zarlink.com; order# 080332) for further details on designing transformer SLIC devices with Zarlink SLAC devices, including transformer selection criteria, setting required termination resistance, operational amplifier requirements, suggested circuit diagrams and other circuit considerations.

## 4.0 SLAC™ DEVICE COEFFICIENTS

The QSLAC and QLSLAC devices have software programmable digital filters that provide receive and transmit gain, equalization, 2-wire impedance matching, and 4-wire echo cancellation. Additionally, each SLAC has programmable analog gain blocks in both the transmit and receive directions. Once the G parameters of the SLIC are determined, WinSLAC 2 software can be used to compute the necessary filter coefficients for achieving the required receive and transmit levels and for optimizing return losses.

### 4.1 Digital Filter Computation

Developing filter coefficients for the QSLAC device involves the following steps whether or not a transformer or solid state hybrid is used in the design:

1. Determine the G parameters for a given SLIC. The G parameters may be measured on a lab bench or calculated using one of Zarlink's PSpice models with system component values.
2. Using the WinSLAC software, input/select G parameters and expected line impedance. Select QSLAC device model, and compute the filter coefficients. Check predicted performance. Modify the relative receive and transmit levels as needed and recompute coefficients.

Once filter coefficients have been determined for the QSLAC device, converting to the QLSLAC device is straightforward. Using the default input attenuator, and modifying the $Z_{RX}$ network by 0.6438, the software developed for the QSLAC device will be fully compatible with the QLSLAC device coefficients.

### 4.2 Performance and Coefficient Compatibility

Because resistor selection is limited to standard resistor values, it is unlikely that exact scaling can be achieved when converting from the QSLAC device to the QLSLAC device. Using E96 values, the gain error can be kept within 0.1 dB nominal. Using E192 series values, the error will be less than 0.05dB.

The effects on transmission performance of such gain errors when converting from a QSLAC device to a QLSLAC device may be simulated through WinSLAC. Figure 5 compares WinSLAC performance predictions for systems using the QSLAC and QLSLAC devices with an Am7920 SLIC. The simulations included external components as shown in Figure 2. Figure 6 compares system performance assuming an Am79R79 SLIC device as shown in Figure 3. The graphs show predicted 2-wire and 4-wire return loss magnitudes over frequency, as well as receive and transmit attenuation distortion. Green lines represent predicted values for the QSLAC device designs while red lines represent predicted values for the QLSLAC device designs.

**Figure 5. WinSLAC™ Performance Comparison: QSLAC™ and QLSLAC™ Devices with the Am7920 SLIC Device**

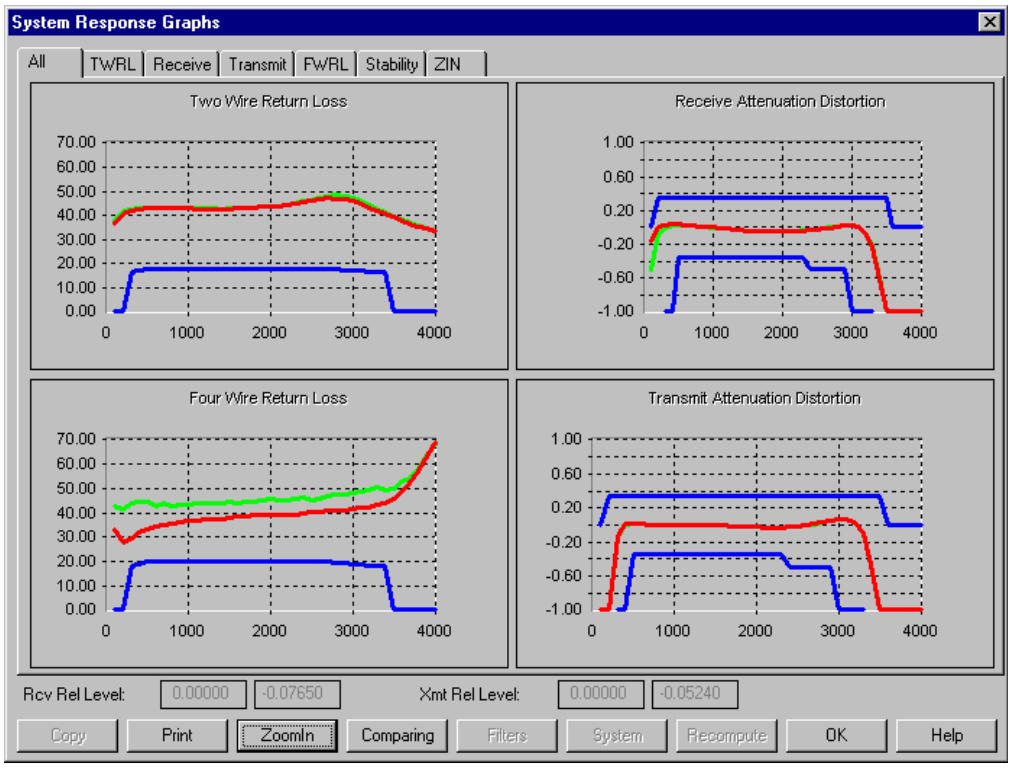
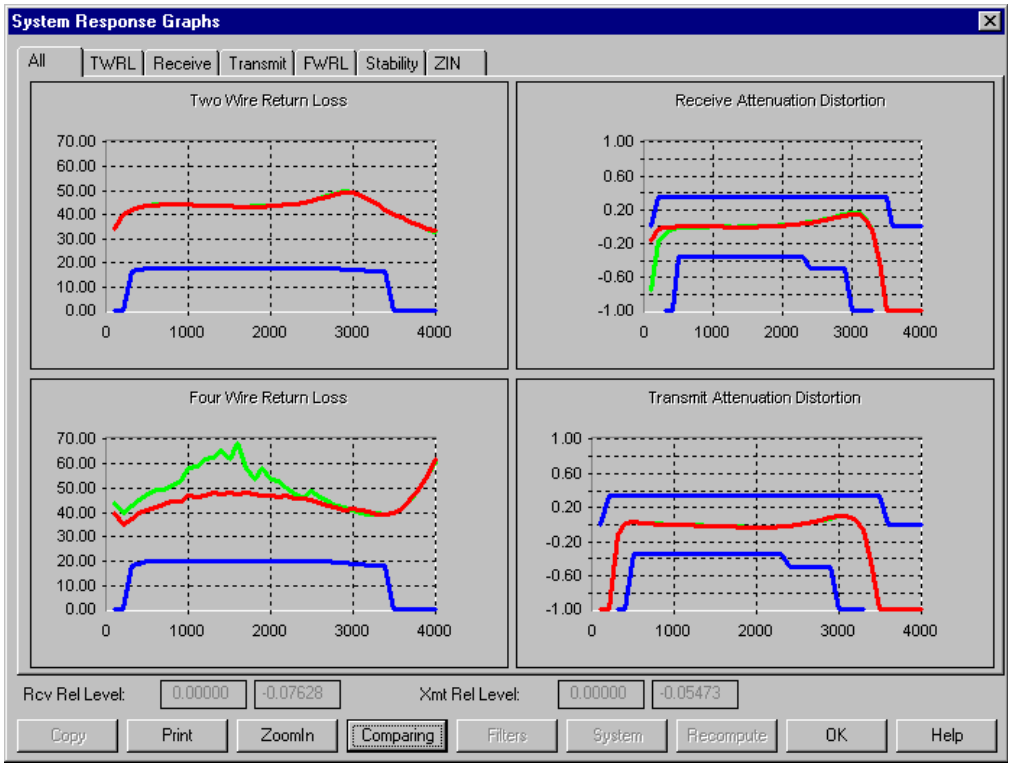



**Figure 6. WinSLAC™ Performance Comparison: QSLAC™ and QLSLAC™ Devices with the Am79R79 SLIC Device**



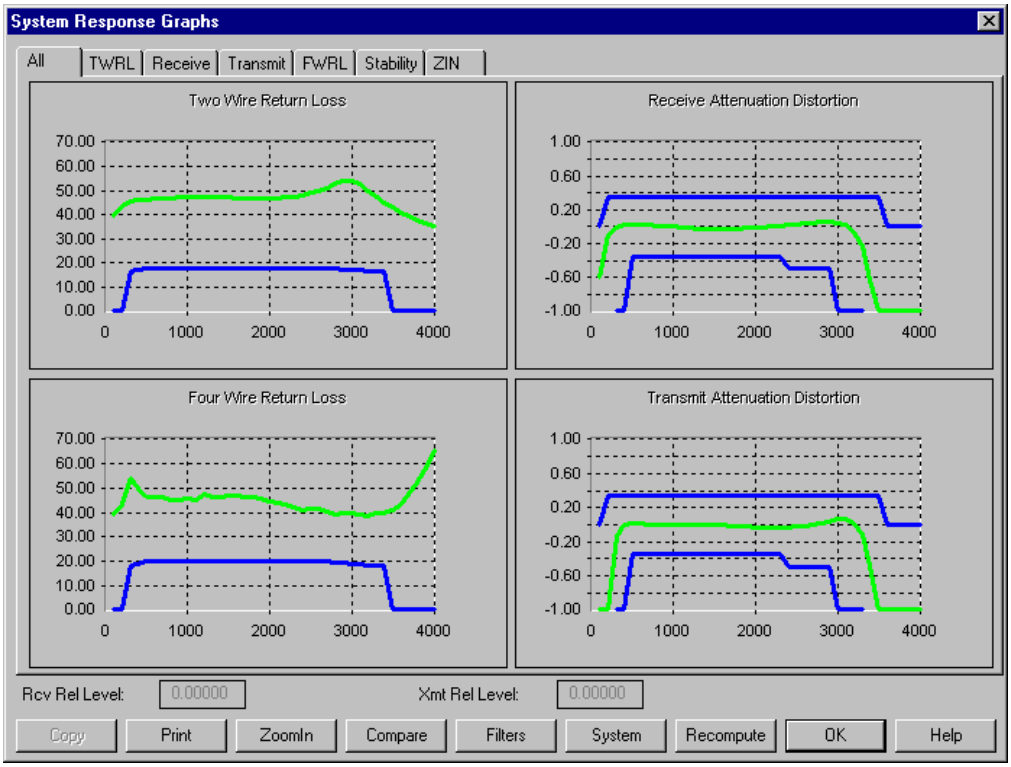

Small differences are due to errors in the transmit and receive gains as a result of choosing standard resistor values. The receive and transmit attenuation distortion curves overlay almost exactly, making the two curves indistinguishable. From Figure 5 it is seen that the receive level is down by 0.076 dB, while the transmit level was reduced by 0.052 dB. The most significant difference is in the 4-wire return

loss, which might suffer slight degradation when introducing error in $Z_{RX}$. Matching gain errors in the receive and transmit direction can minimize the effect on the 4-wire return loss. Indeed, the simulation indicates that the 4-wire return loss for the QLSLAC device design is very similar to that of the QSLAC device design despite the errors introduced by selecting standard component values. Overall, simulations indicate that performance can be maintained by using the same filter coefficients if $Z_{RX}$ and the voltage divider are properly selected. WinSLAC 2 software, which can be ordered from the Zarlink website at www.zarlink.com, can be used to verify that the gain adjustments are correct, as demonstrated in these examples.

## 4.3 Predicted Performance with the Le57D11 DSLIC Device

Because both the Le57D11 SLIC device and the QLSLAC device are new parts, coefficient compatibility and design transitioning are not issues in the case of the Le57D11/QLSLAC device design. Filter coefficients for the QLSLAC device can be determined using WinSLAC 2 using an appropriate SLIC device model. Figure 7 shows the simulated performance of the design illustrated in Figure 4.

**Figure 7. WinSLAC™ Performance Predictions: QLSLAC™ Device with Le57D11 SLIC Device**




## 5.0 COMPARATIVE TRANSMISSION PERFORMANCE

Device and system level testing indicate that the QSLAC and QLSLAC devices exhibit nearly identical performance. Using the example designs of Figure 2, it is possible to directly compare the performance of QSLAC device design versus the QLSLAC device design with the same set of filter coefficients. Using the WinSLAC software tools, filter coefficients are determined for a QSLAC/Am7920 device design with a 600 Ω terminating impedance. With the coefficients loaded into the QSLAC device, various system level transmission measurements can be performed. Similar measurements may be taken for the QLSLAC/Am7920 device design by making the necessary hardware changes while using the same filter coefficients, the same Am7920 device, and the same terminating load.

Figure 8 contains plots comparing transmission performance data taken in the lab for QSLAC and QLSLAC devices with an Am7920 SLIC device. The measurements, which include two wire and four wire return loss and attenuation distortion in both the receive and transmit directions, were taken with Wandel and Goltermann's PCM-4 test equipment and a 600 Ω load. Circles represent data taken for the QSLAC device design, while the "x" symbols represent data taken for the QLSLAC device design. Figure 9 and Figure 10 show comparisons of gain tracking and signal to distortion measurements respectively for the same QSLAC and QLSLAC device designs with an Am7920 chip.

**Figure 8. Transmission Performance with Am7920 SLIC Device**

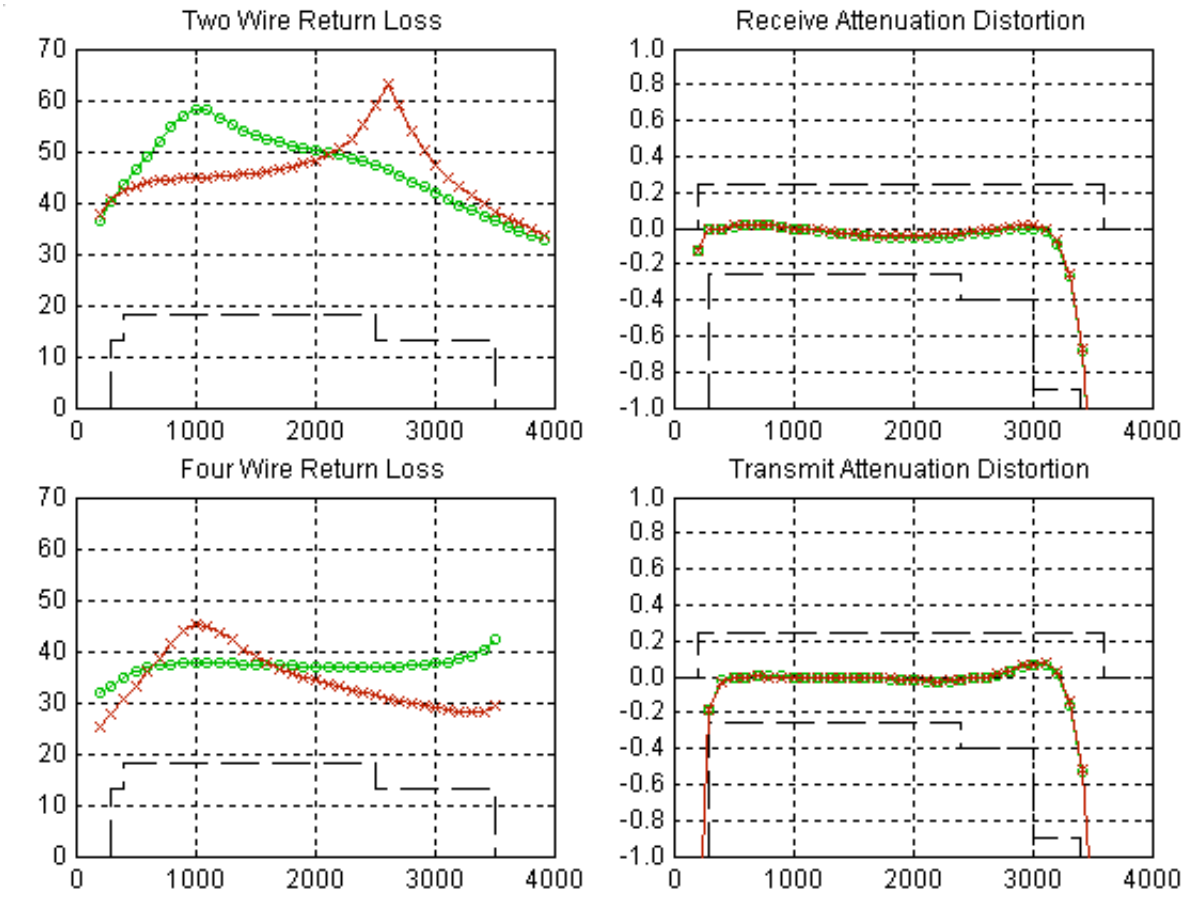


**Figure 9. Gain Tracking with Am7920 SLIC Device**

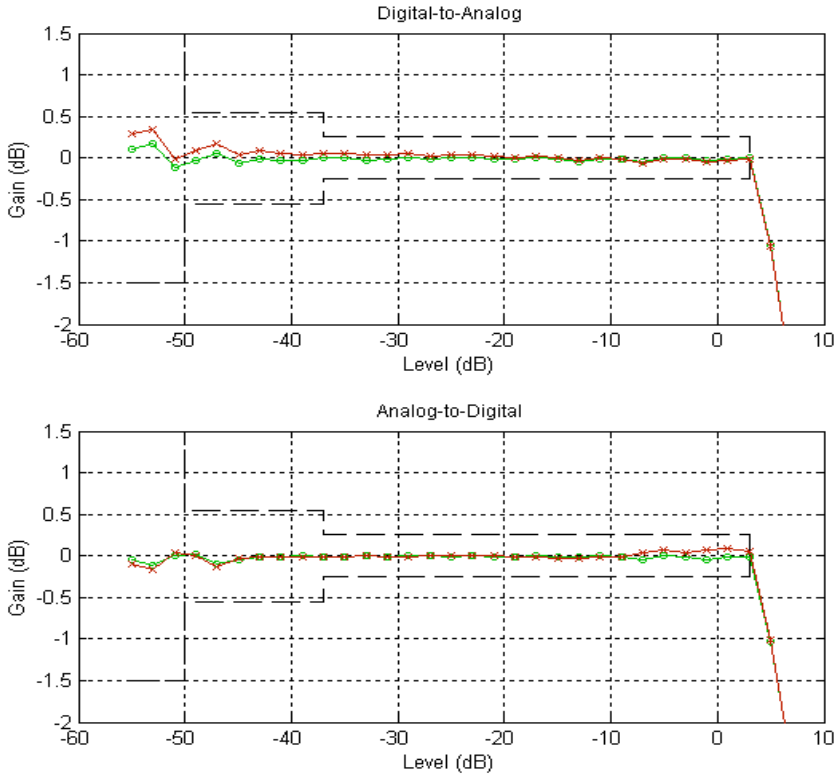



**Figure 10. Signal-to-Distortion with Am7920 SLIC Device**

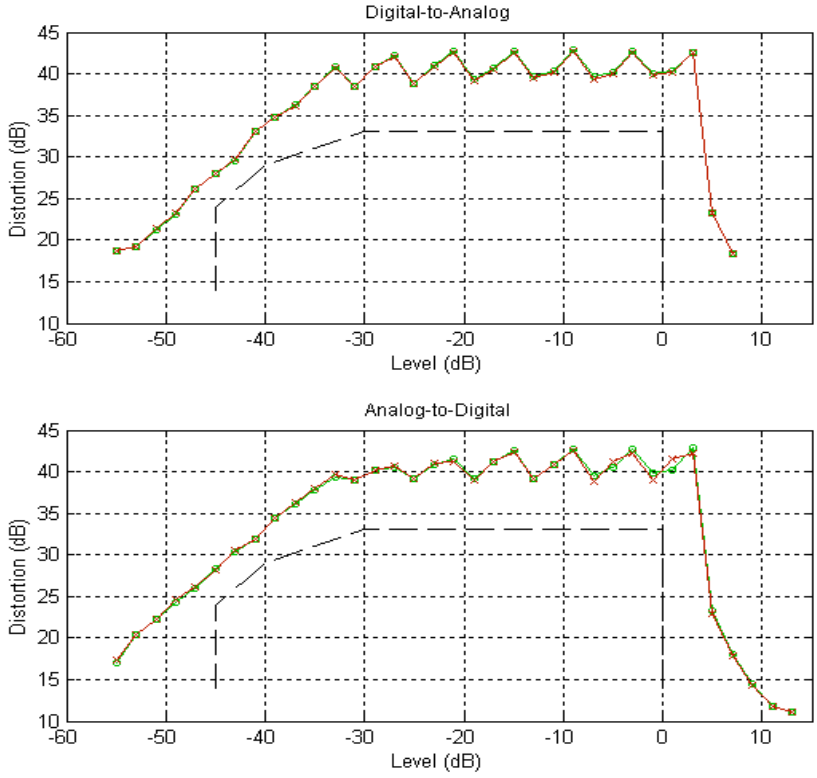


Figure 11 contains transmission plot comparisons for the QSLAC/QLSLAC device designs with an Am79R79 SLIC device, while Figure 12 and Figure 13 compare gain tracking and signal to distortion measurements for an Am79R79 system respectively.

**Figure 11. Transmission Performance with Am79R79 SLIC Device**

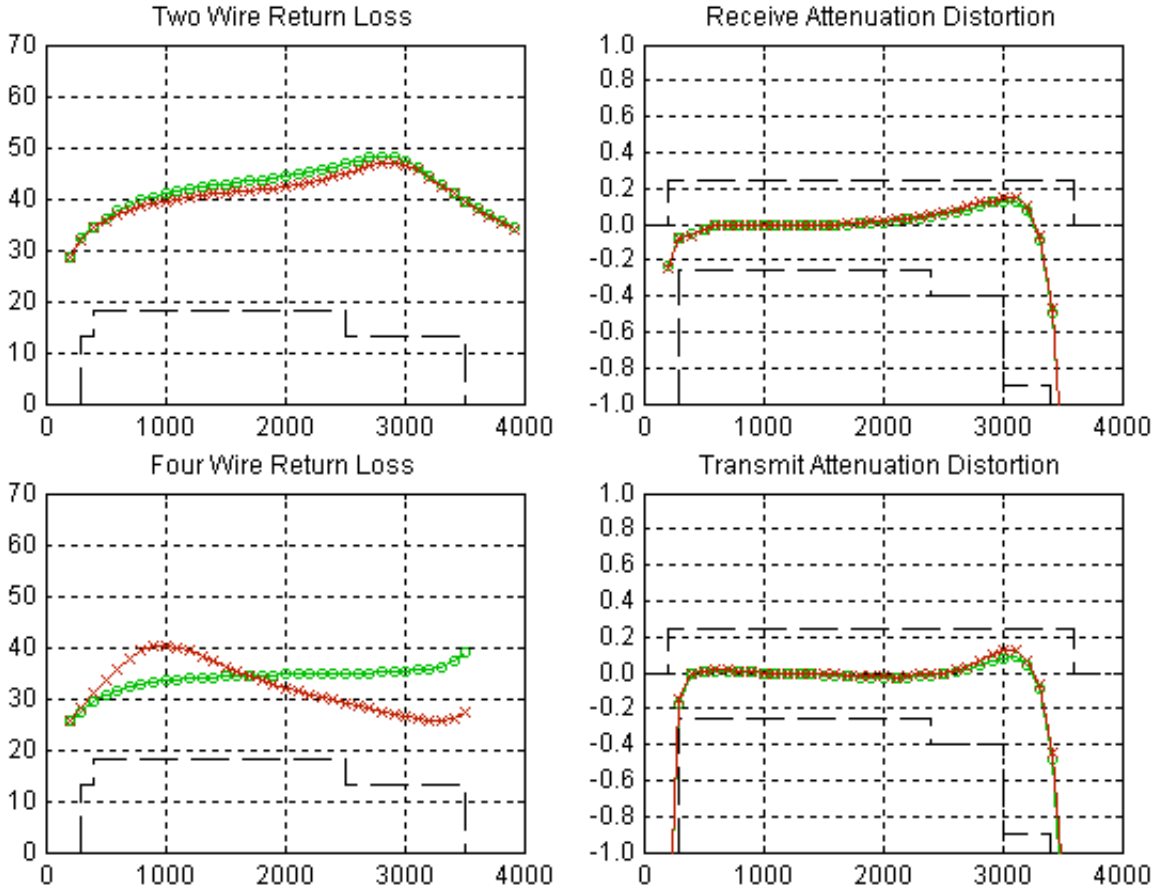


**Figure 12. Gain Tracking with Am79R79 SLIC Device**

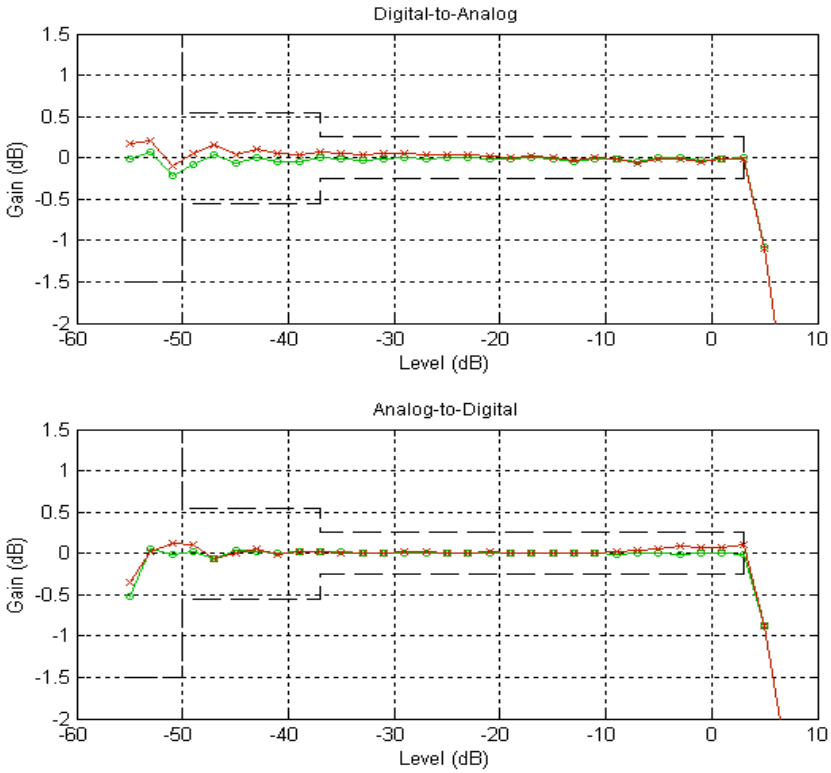
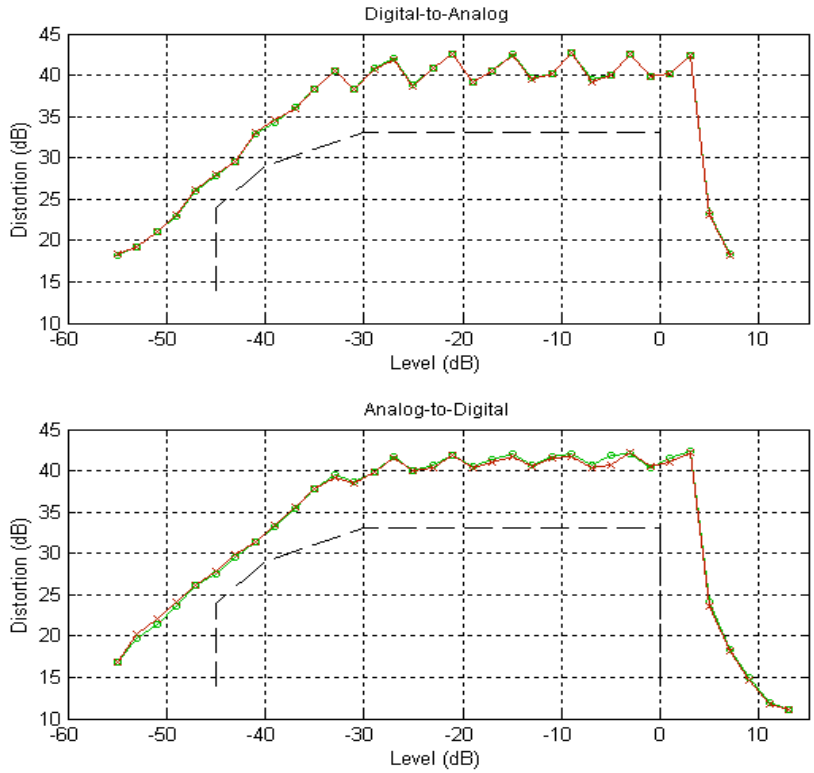



**Figure 13. Signal-to-Distortion with Am79R79 SLIC Device**



From the plots, it is clear that all the system level transmission measurements meet the template requirements. There are some differences in the two-wire and four wire return losses, however such difference are within the normally expected variances of the device. For the most part, the two and four wire return losses are greater than 25 dB for both the QSLAC and QLSLAC designs. In addition, gain tracking and signal-to-distortion measurements appear to be almost identical for systems using the QSLAC device and QLSLAC device.

Similarly Figure 14 contains transmission plots for the QLSLAC device designs with an Le57D11 SLIC device, while Figure 15 and Figure 16 show gain tracking and signal to distortion measurements respectively. These performance measurements were made using the design shown in Figure 4 with the input attenuator disabled and filter coefficients determined by WinSLAC 2.

**Figure 14. Transmission Performance with a QLSLAC Device and Le57D11 SLIC Device**

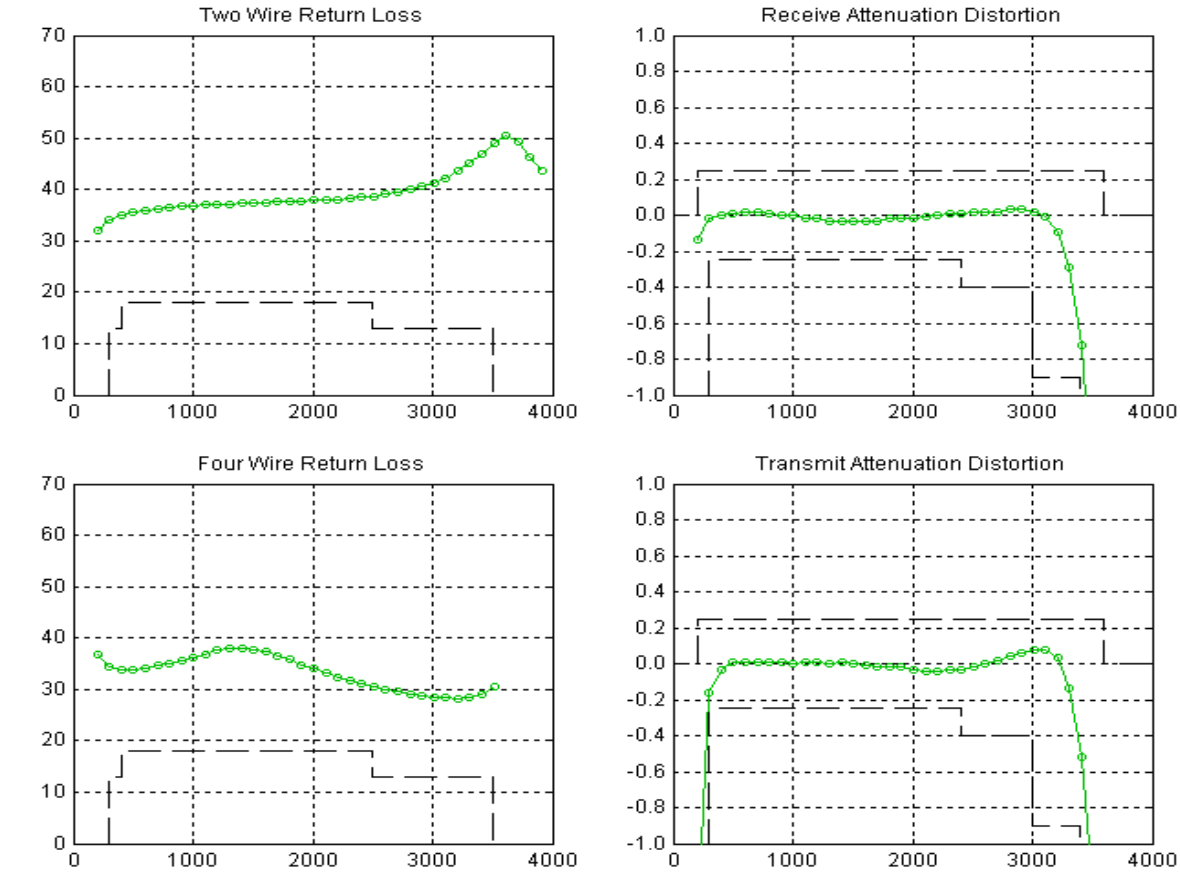


**Figure 15. Gain Tracking of a QLSLAC/Le57D11 Design**

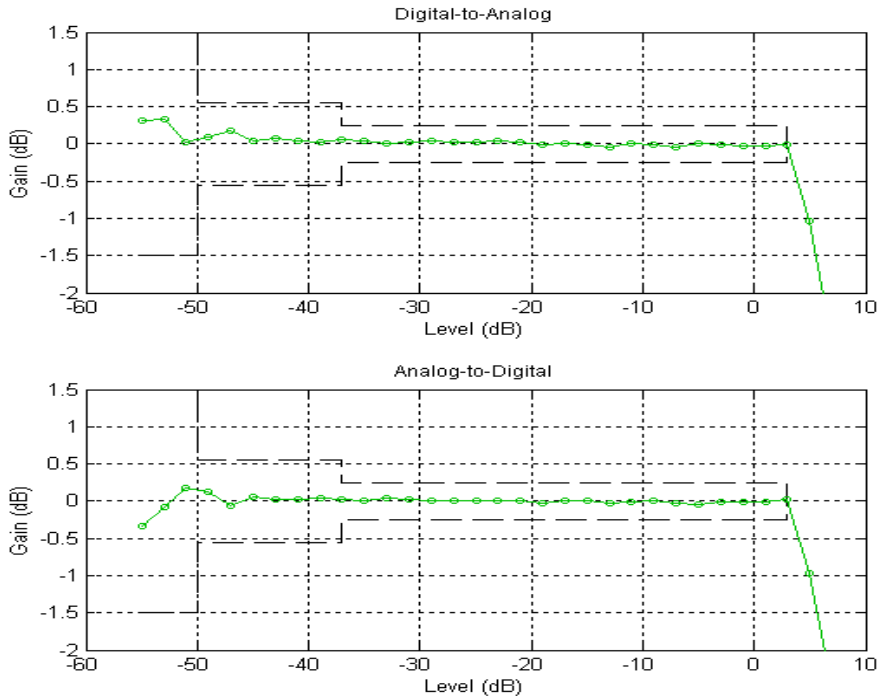
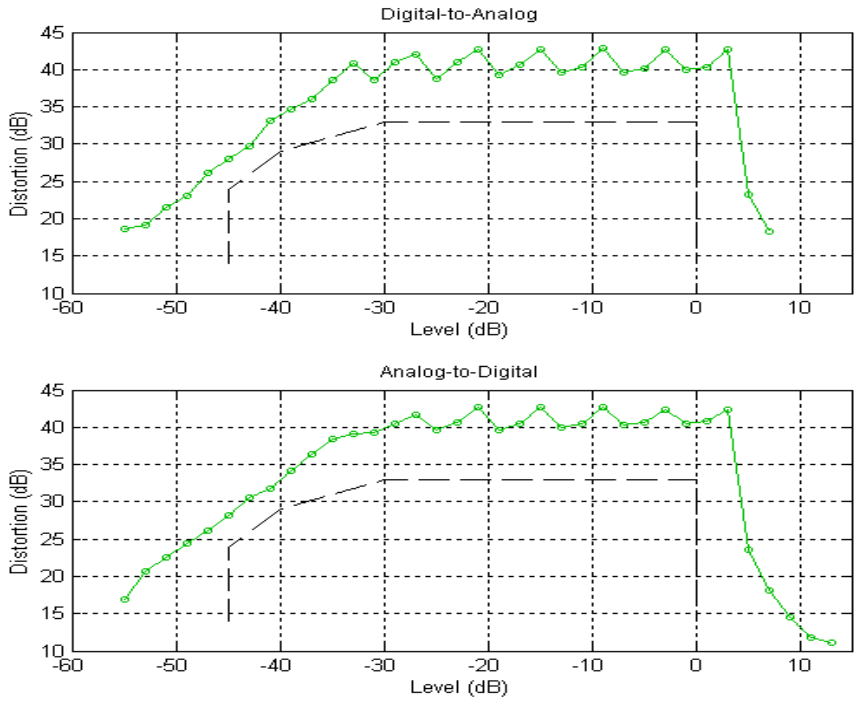



**Figure 16. Signal-to-Distortion of a QLSLAC/Le57D11 Design**



## 6.0 INTERFACE CONSIDERATIONS

The interface considerations include: requirements for the MPI, the PCM interface, master clock (MCLK), and SLIC device control outputs/inputs. Specifications and functionality were intended to be almost identical between the two SLAC devices to maximize compatibility.

### 6.1 Microprocessor Interface

The MPI for the QLSLAC device is almost identical to the QSLAC device MPI, including 5.0 V tolerant inputs, similar timing requirements, and the same logic thresholds for data clock, chip select, and data I/O inputs. One difference is that the maximum data clock (DCLK) rate increased from 4.096 MHz (QSLAC device) to 8.192 MHz (QLSLAC device). As a result, the minimum DCLK low pulse for the QLSLAC device is reduced by half, and the Chip Select set-up time has decreased from 70 ns to 30 ns when compared with the QSLAC device. The only other difference is that the output voltage for the data I/O reaches +3.3 V rather than +5.0 V. An MPI interface clocked at 4.096 MHz or less is completely compatible with both the QSLAC device and QLSLAC devices.

All MPI commands are equivalent for the two devices, with the exception of the most significant bit of the AISN and Analog Gains Register (Command 50/51h). Although it is a reserved bit for both SLAC devices, the bit is a “don’t care” for the QSLAC device, while the QLSLAC device requires that the bit be set to “0” (default). Ensure that this bit does not get set in the QLSLAC device software. If recommendations to set all reserved bits to a logic “0” are followed, this will not be an issue.

### 6.2 PCM Interface

The PCM interface is primarily the same for both the QSLAC and QLSLAC devices, including the 5.0 V tolerant inputs. Frame sync must be provided to both devices as an accurate 8 kHz pulse train. In addition, the PCM clock (PCLK), which has the same timing requirements and logic thresholds for both SLAC devices, must be synchronous with FS in each case.

The timing requirements for the PCM receive data (DRA/DRB) and transmit data (DXA/DXB), and time slot control (TSCA/TSCB) outputs are also consistent between the SLAC devices. From a new design perspective, the only difference in the PCM interface is that the final high voltage of the DXA/DXB output pins reach approximately 3.3 V instead of 5.0 V.

For the QSLAC device, running at an 8.192 MHz clock, a pull-up resistor of 360 Ω to 5.0 V is recommended for the TSCA and TSCB pins. If pulling TSCA and TSCB to 3.3 V, the pull-up resistors should be decreased to 240 Ω in order to maintain approximately the same rise time to the logic threshold. If running at clock speeds lower than 8.192 MHz, the TSCA pull-up times can be slower, meaning that the pull-up resistor can be proportionally larger.

### 6.3 Master Clock

The MCLK circuit, which is identical for both the QSLAC and the QLSLAC devices, may be operated either synchronously or asynchronously with FS. Asynchronous operation, however, can result in occasional phase jumps of the transmission signal, which are likely to be incompatible with V.90 modems. Zarlink recommends that the master clock be an integer multiple of frame sync unless phase jumps of 1.95 µs can be tolerated.

### 6.4 SLIC Device Control/Data Lines

Both the QSLAC device and the QLSLAC device have up to five TTL compatible input/output ports for controlling the SLIC device, relays, LEDs or other devices. These ports are software programmable to be either inputs or outputs. As inputs, the CD1 and CD2 may be debounced, filtered, and/or demultiplexed by the QSLAC or QLSLAC device in order to provide information from the SLIC device, such as off-hook or ground key detection. In general, no software or hardware modifications are necessary for SLIC device control or monitoring.

As inputs, the CD pins are high impedance with leakage currents smaller than ±15 µA. The active low and active high outputs are clamped to $V_{CCD}$ and digital ground respectively for both the QLSLAC and the QSLAC devices. Consequently, the active low output level of the CD pins is lower for QLSLAC device than for the QSLAC device. The CD pins of the QLSLAC device may be pulled-up to a 5 V supply, or some other non-standard voltage, by loading the output data as a logic low, then changing the I/O direction of the pin from an output to an input. If the CD pins are used to drive light emitting diodes or opto-couplers, for example, active low outputs can be pulled up to 5 V by switching the I/O

configuration to an input. The leakage current of the I/O input state should be sufficiently small to avoid a soft turn-on. For active high outputs (sourcing current), the value of the current limiting resistor will need to be changed to provide the same current drive. There are two additional outputs per channel, CD6 and CD7, available on the Le58QL063 device. Because these pins can not be programmed as inputs, they should not be used with 5 volt pull-ups.

## 7.0 CONCLUSION

Line cards that wer conceived to use the QSLAC device may be designed to smoothly convert to the lower voltage QLSLAC device. If proper considerations and flexibility are given to the layout and hardware design, complete software compatibility may be achieved. Such hardware considerations are relatively straightforward, cost competitive, and allow new QLSLAC device designs to realize software compatibility with existing QSLAC device designs.

## ADDITIONAL REFERENCES


1. *Le58QL02/021/031 QLSLAC™ Data Sheet, Revision B1*, PID# 080753, April 2002, http://www.zarlink.com.
2. *Le58QL061/063 QLSLAC™ Data Sheet, Revision C1*, PID# 080754, April 2002, http://www.zarlink.com.
3. *Am79Q02/021/031 QSLAC™ Data Sheet*, PID# 080147, December 2001, http://www.zarlink.com.
4. *Am79Q061/063 QSLAC™ Data Sheet*, PID# 080193, December 2001, http://www.zarlink.com.
5. *WinSLAC2 Software User's Guide*, PID# 080779, March 2002, http://www.zarlink.com.
6. *Transformer SLIC Device Interface Requirements for Zarlink SLAC™ Codec/Filter Devices Application Note*, PID# 080332, October, 2001, http://www.zarlink.com.


## REVISION HISTORY

### Revision A1 to B1

- Added new system design using the DSLIC as well as performance comparisons
- Added information regarding internal attenuator and removed references to external attenuator
- Updated WinSLAC 1.2 simulations with WinSLAC 2 simulations assuming internal attenuator
- Added system performance comparisons for the QSLAC and QLSLAC design examples
- Added information about SLIC control/data pins when pulling up to 5 volts
- Edited Conclusion section
- Updated "Additional References" section

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