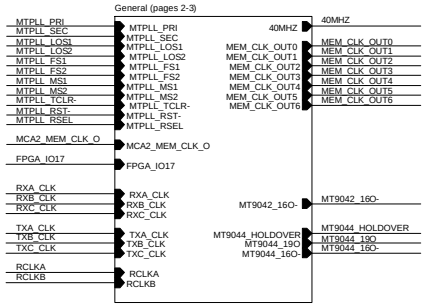
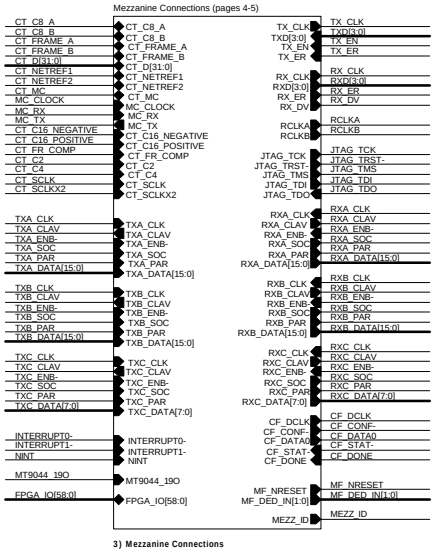
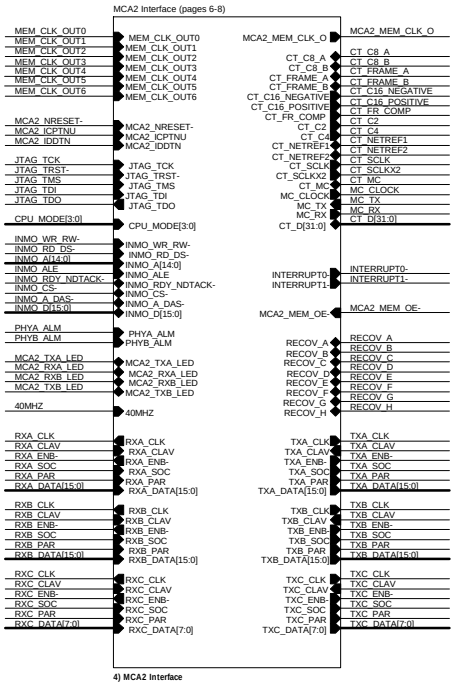
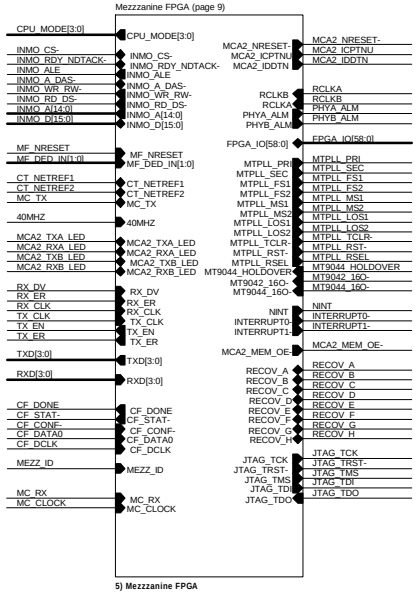








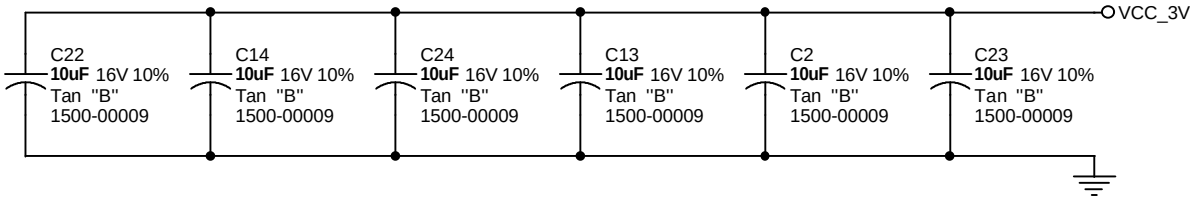
ZARLINK Semiconductor - Global Design Support

Title: MT90503 Mezzanine Board — Interconnections

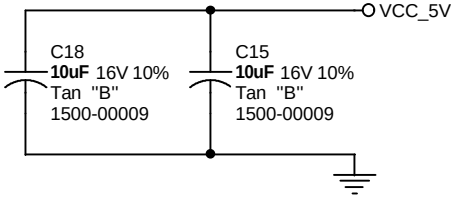
Size	Document Number	Designed By:	Checked By:	Rev
C	1000-001			01

Date: Friday, November 17, 2000 Sheet 1 of 9

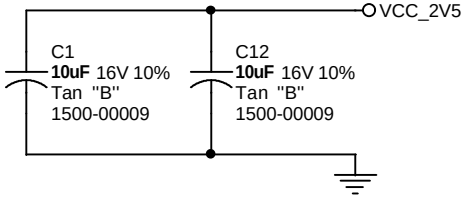
Spread the bulk decoupling capacitors on the board.



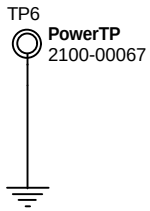
Spread the bulk decoupling capacitors on the board.



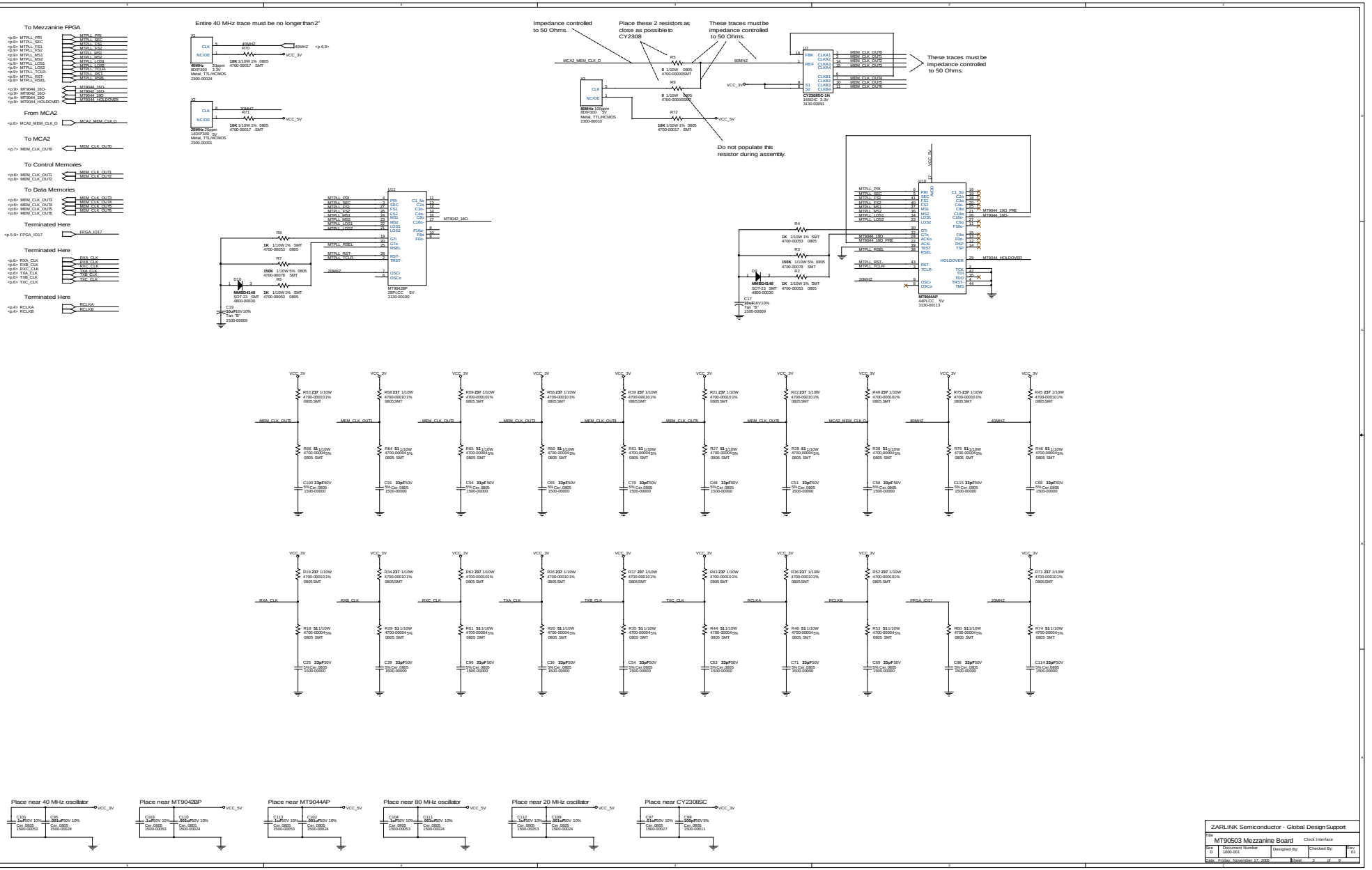
Spread the bulk decoupling capacitors on the board.



Place near CY1352 Memories



ZARLINK Semiconductor - Global Design Support				
Title: MT90503 Mezzanine Board — Power Interface				
Size: A	Document Number: 1000-001	Designed By:	Checked By:	Rev: 01
Date: Friday, November 17, 2000	Sheet 2 of 9			


To Mezzanine FPGA
MTPLL_PRI
MTPLL_SEC
MTPLL_FS1
MTPLL_FS2
MTPLL_MS1
MTPLL_MS2
MTPLL_LOS1
MTPLL_LOS2
MTPLL_TCLR
MTPLL_RST-
MTPLL_RSEL
MT9044_16O-
MT9042_16O-
MT9044_19O
MT9044_HOLDOVER
From MCA2
MCA2_MEM_CLK_O
To MCA2
MEM_CLK_OUT0
To Control Memories
MEM_CLK_OUT1
MEM_CLK_OUT2
To Data Memories
MEM_CLK_OUT3
MEM_CLK_OUT4
MEM_CLK_OUT5
MEM_CLK_OUT6
Terminated Here
FPGA_IO17
Terminated Here
RXA_CLK
RXB_CLK
RXC_CLK
TXA_CLK
TXB_CLK
TXC_CLK
Terminated Here
RCLKA
RCLKB
Entire 40 MHz trace must be no longer than 2"
40MHz
20MHz
Impedance controlled to 50 Ohms.
Place these 2 resistors as close as possible to CY2308
These traces must be impedance controlled to 50 Ohms.
These traces must be impedance controlled to 50 Ohms.
Do not populate this resistor during assembly.
MCA2_MEM_CLK_O
80MHz
VCC_3V
VCC_5V
CY2308SC-1H
MT9042_16O-
MT9044_19O_PRE
MT9044_16O-
MT9044_HOLDOVER
MT9044AP
MEM_CLK_OUT0
MEM_CLK_OUT1
MEM_CLK_OUT2
MEM_CLK_OUT3
MEM_CLK_OUT4
MEM_CLK_OUT5
MEM_CLK_OUT6
MCA2_MEM_CLK_O
80MHz
40MHz
RXA_CLK
RXB_CLK
RXC_CLK
TXA_CLK
TXB_CLK
TXC_CLK
RCLKA
RCLKB
FPGA_IO17
20MHz
Place near 40 MHz oscillator
Place near MT9042BP
Place near MT9044AP
Place near 80 MHz oscillator
Place near 20 MHz oscillator
Place near CY2308SC
ZARLINK Semiconductor - Global Design Support
MT90503 Mezzanine Board
Clock Interface
Document Number 1000-001
Designed By:
Checked By:
Rev 01
Friday, November 17, 2006
Sheet 3 of 9

3 UTOPIA ports.
Between Main board and MCA2.

<p.6> RXA_CLK
<p.6> RXA_CLAV
<p.6> RXA_ENB-
<p.6> RXA_SOC
<p.6> RXA_PAR
<p.6> RXA_DATA[15:0]

<p.6> TXA_CLK
<p.6> TXA_CLAV
<p.6> TXA_ENB-
<p.6> TXA_SOC
<p.6> TXA_PAR
<p.6> TXA_DATA[15:0]

<p.6> RXB_CLK
<p.6> RXB_CLAV
<p.6> RXB_ENB-
<p.6> RXB_SOC
<p.6> RXB_PAR
<p.6> RXB_DATA[15:0]

<p.6> TXB_CLK
<p.6> TXB_CLAV
<p.6> TXB_ENB-
<p.6> TXB_SOC
<p.6> TXB_PAR
<p.6> TXB_DATA[15:0]

<p.6> RXC_CLK
<p.6> RXC_CLAV
<p.6> RXC_ENB-
<p.6> RXC_SOC
<p.6> RXC_PAR
<p.6> RXC_DATA[7:0]

<p.6> TXC_CLK
<p.6> TXC_CLAV
<p.6> TXC_ENB-
<p.6> TXC_SOC
<p.6> TXC_PAR
<p.6> TXC_DATA[7:0]

19.44 MHz Clock from PLL.

<p.3> MT9044_19O

UTOPIA PHY clocks.
From PHYs A & B on Main Board
to FPGA on Mezzanine Board.

<p.3,9> RCLKA
<p.3,9> RCLKB

Ethernet

<p.9> TX_ER
<p.9> TX_EN
<p.9> RX_DV
<p.9> RX_ER
<p.9> TX_CLK
<p.9> RX_CLK

<p.9> TXD[3:0]
<p.9> RXD[3:0]

Sent to Mezzanine FPGA to identify
the board below it

<p.9> MEZZ_ID

Assembled on solder side of Mezzanine Card

J4A

GND	1	USER_IO1	USER_IO2	2	GND
RXA_DATA0	3	USER_IO3	USER_IO4	4	RXA_DATA1
RXA_DATA2	5	USER_IO5	USER_IO6	6	RXA_DATA3
RXA_DATA4	7	USER_IO7	USER_IO8	8	RXA_DATA5
RXA_DATA6	9	USER_IO9	USER_IO10	10	RXA_DATA7
RXA_DATA8	11	USER_IO11	USER_IO12	12	RXA_DATA9
VCC_5V	13	USER_IO13	USER_IO14	14	VCC_5V
RXA_DATA10	15	USER_IO15	USER_IO16	16	RXA_DATA11
RXA_DATA12	17	USER_IO17	USER_IO18	18	RXA_DATA13
RXA_DATA14	19	USER_IO19	USER_IO20	20	RXA_DATA15
RXA_PAR	21	USER_IO21	USER_IO22	22	RXA_SOC
GND	23	USER_IO23	USER_IO24	24	GND
RXA_ENB-	25	USER_IO25	USER_IO26	26	RXA_CLAV
RXA_CLK	27	USER_IO27	USER_IO28	28	TXA_DATA0
TXA_DATA1	29	USER_IO29	USER_IO30	30	TXA_DATA2
TXA_DATA3	31	USER_IO31	USER_IO32	32	TXA_DATA4
TXA_DATA5	33	USER_IO33	USER_IO34	34	TXA_DATA6
VCC_3V	35	USER_IO35	USER_IO36	36	VCC_3V
TXA_DATA7	37	USER_IO37	USER_IO38	38	TXA_DATA8
TXA_DATA9	39	USER_IO39	USER_IO40	40	TXA_DATA10
TXA_DATA11	41	USER_IO41	USER_IO42	42	TXA_DATA12
TXA_DATA13	43	USER_IO43	USER_IO44	44	TXA_DATA14
TXA_DATA15	45	USER_IO45	USER_IO46	46	TXA_PAR
GND	47	USER_IO47	USER_IO48	48	GND
TXA_SOC	49	USER_IO49	USER_IO50	50	TXA_ENB-
TXA_CLAV	51	USER_IO51	USER_IO52	52	TXA_CLK
RXB_DATA0	53	USER_IO53	USER_IO54	54	RXB_DATA1
RXB_DATA2	55	USER_IO55	USER_IO56	56	RXB_DATA3
RXB_DATA4	57	USER_IO57	USER_IO58	58	RXB_DATA5
VCC_2V5	59	USER_IO59	USER_IO60	60	VCC_2V5
RXB_DATA6	61	USER_IO61	USER_IO62	62	RXB_DATA7
RXB_DATA8	63	USER_IO63	USER_IO64	64	RXB_DATA9
RXB_DATA10	65	USER_IO65	USER_IO66	66	RXB_DATA11
RXB_DATA12	67	USER_IO67	USER_IO68	68	RXB_DATA13
GND	69	USER_IO69	USER_IO70	70	GND
RXB_DATA14	71	USER_IO71	USER_IO72	72	RXB_DATA15
RXB_PAR	73	USER_IO73	USER_IO74	74	RXB_SOC
RXB_ENB-	75	USER_IO75	USER_IO76	76	RXB_CLAV
RXB_CLK	77	USER_IO77	USER_IO78	78	TXB_DATA0
TXB_DATA1	79	USER_IO79	USER_IO80	80	TXB_DATA2

177984-8, 7/9mm Plug
80x2 SMT
2100-00061

J4B

VCC_5V	81	USER_IO81	USER_IO82	82	VCC_5V
TXB_DATA3	83	USER_IO83	USER_IO84	84	TXB_DATA4
TXB_DATA5	85	USER_IO85	USER_IO86	86	TXB_DATA6
TXB_DATA7	87	USER_IO87	USER_IO88	88	TXB_DATA8
TXB_DATA9	89	USER_IO89	USER_IO90	90	TXB_DATA10
TXB_DATA11	91	USER_IO91	USER_IO92	92	TXB_DATA12
VCC_3V	93	USER_IO93	USER_IO94	94	VCC_3V
TXB_DATA13	95	USER_IO95	USER_IO96	96	TXB_DATA14
TXB_DATA15	97	USER_IO97	USER_IO98	98	TXB_PAR
TXB_SOC	99	USER_IO99	USER_IO100	100	TXB_ENB-
TXB_CLAV	101	USER_IO101	USER_IO102	102	TXB_CLK
GND	103	USER_IO103	USER_IO104	104	GND
RXC_DATA0	105	USER_IO105	USER_IO106	106	RXC_DATA1
RXC_DATA2	107	USER_IO107	USER_IO108	108	RXC_DATA3
RXC_DATA4	109	USER_IO109	USER_IO110	110	RXC_DATA5
RXC_DATA6	111	USER_IO111	USER_IO112	112	RXC_DATA7
RXC_PAR	113	USER_IO113	USER_IO114	114	RXC_SOC
VCC_2V5	115	USER_IO115	USER_IO116	116	VCC_2V5
RXC_ENB-	117	USER_IO117	USER_IO118	118	RXC_CLAV
RXC_CLK	119	USER_IO119	USER_IO120	120	TXC_DATA0
TXC_DATA1	121	USER_IO121	USER_IO122	122	TXC_DATA2
TXC_DATA3	123	USER_IO123	USER_IO124	124	TXC_DATA4
TXC_DATA5	125	USER_IO125	USER_IO126	126	TXC_DATA6
GND	127	USER_IO127	USER_IO128	128	GND
TXC_DATA7	129	USER_IO129	USER_IO130	130	TXC_PAR
TXC_SOC	131	USER_IO131	USER_IO132	132	TXC_ENB-
TXC_CLAV	133	USER_IO133	USER_IO134	134	TXC_CLK
RCLKA	135	USER_IO135	USER_IO136	136	RCLKB
TX_CLK	137	USER_IO137	USER_IO138	138	RX_CLK
VCC_3V	139	USER_IO139	USER_IO140	140	VCC_3V
TXD0	141	USER_IO141	USER_IO142	142	TXD1
TXD2	143	USER_IO143	USER_IO144	144	TXD3
RXD0	145	USER_IO145	USER_IO146	146	RXD1
RXD2	147	USER_IO147	USER_IO148	148	RXD3
VCC_3V	149	USER_IO149	USER_IO150	150	VCC_3V
TX_ER	151	USER_IO151	USER_IO152	152	TX_EN
RX_DV	153	USER_IO153	USER_IO154	154	RX_ER
MT9044_19O	155	USER_IO155	USER_IO156	156	
	157	USER_IO157	USER_IO158	158	MEZZ_ID
GND	159	USER_IO159	USER_IO160	160	GND

177984-8, 7/9mm Plug
80x2 SMT
2100-00061

Assembled on component side of Mezzanine Card

J1A

GND	1	USER_IO1	USER_IO2	2	GND
RXA_DATA0	3	USER_IO3	USER_IO4	4	RXA_DATA1
RXA_DATA2	5	USER_IO5	USER_IO6	6	RXA_DATA3
RXA_DATA4	7	USER_IO7	USER_IO8	8	RXA_DATA5
RXA_DATA6	9	USER_IO9	USER_IO10	10	RXA_DATA7
RXA_DATA8	11	USER_IO11	USER_IO12	12	RXA_DATA9
VCC_5V	13	USER_IO13	USER_IO14	14	VCC_5V
RXA_DATA10	15	USER_IO15	USER_IO16	16	RXA_DATA11
RXA_DATA12	17	USER_IO17	USER_IO18	18	RXA_DATA13
RXA_DATA14	19	USER_IO19	USER_IO20	20	RXA_DATA15
RXA_PAR	21	USER_IO21	USER_IO22	22	RXA_SOC
GND	23	USER_IO23	USER_IO24	24	GND
RXA_ENB-	25	USER_IO25	USER_IO26	26	RXA_CLAV
RXA_CLK	27	USER_IO27	USER_IO28	28	TXA_DATA0
TXA_DATA1	29	USER_IO29	USER_IO30	30	TXA_DATA2
TXA_DATA3	31	USER_IO31	USER_IO32	32	TXA_DATA4
TXA_DATA5	33	USER_IO33	USER_IO34	34	TXA_DATA6
VCC_3V	35	USER_IO35	USER_IO36	36	VCC_3V
TXA_DATA7	37	USER_IO37	USER_IO38	38	TXA_DATA8
TXA_DATA9	39	USER_IO39	USER_IO40	40	TXA_DATA10
TXA_DATA11	41	USER_IO41	USER_IO42	42	TXA_DATA12
TXA_DATA13	43	USER_IO43	USER_IO44	44	TXA_DATA14
TXA_DATA15	45	USER_IO45	USER_IO46	46	TXA_PAR
GND	47	USER_IO47	USER_IO48	48	GND
TXA_SOC	49	USER_IO49	USER_IO50	50	TXA_ENB-
TXA_CLAV	51	USER_IO51	USER_IO52	52	TXA_CLK
RXB_DATA0	53	USER_IO53	USER_IO54	54	RXB_DATA1
RXB_DATA2	55	USER_IO55	USER_IO56	56	RXB_DATA3
RXB_DATA4	57	USER_IO57	USER_IO58	58	RXB_DATA5
VCC_2V5	59	USER_IO59	USER_IO60	60	VCC_2V5
RXB_DATA6	61	USER_IO61	USER_IO62	62	RXB_DATA7
RXB_DATA8	63	USER_IO63	USER_IO64	64	RXB_DATA9
RXB_DATA10	65	USER_IO65	USER_IO66	66	RXB_DATA11
RXB_DATA12	67	USER_IO67	USER_IO68	68	RXB_DATA13
GND	69	USER_IO69	USER_IO70	70	GND
RXB_DATA14	71	USER_IO71	USER_IO72	72	RXB_DATA15
RXB_PAR	73	USER_IO73	USER_IO74	74	RXB_SOC
RXB_ENB-	75	USER_IO75	USER_IO76	76	RXB_CLAV
RXB_CLK	77	USER_IO77	USER_IO78	78	TXB_DATA0
TXB_DATA1	79	USER_IO79	USER_IO80	80	TXB_DATA2

177983-8 SMT
Mezzanine receptacle
2100-00043

J1B

VCC_5V	81	USER_IO81	USER_IO82	82	VCC_5V
TXB_DATA3	83	USER_IO83	USER_IO84	84	TXB_DATA4
TXB_DATA5	85	USER_IO85	USER_IO86	86	TXB_DATA6
TXB_DATA7	87	USER_IO87	USER_IO88	88	TXB_DATA8
TXB_DATA9	89	USER_IO89	USER_IO90	90	TXB_DATA10
TXB_DATA11	91	USER_IO91	USER_IO92	92	TXB_DATA12
VCC_3V	93	USER_IO93	USER_IO94	94	VCC_3V
TXB_DATA13	95	USER_IO95	USER_IO96	96	TXB_DATA14
TXB_DATA15	97	USER_IO97	USER_IO98	98	TXB_PAR
TXB_SOC	99	USER_IO99	USER_IO100	100	TXB_ENB-
TXB_CLAV	101	USER_IO101	USER_IO102	102	TXB_CLK
GND	103	USER_IO103	USER_IO104	104	GND
RXC_DATA0	105	USER_IO105	USER_IO106	106	RXC_DATA1
RXC_DATA2	107	USER_IO107	USER_IO108	108	RXC_DATA3
RXC_DATA4	109	USER_IO109	USER_IO110	110	RXC_DATA5
RXC_DATA6	111	USER_IO111	USER_IO112	112	RXC_DATA7
RXC_PAR	113	USER_IO113	USER_IO114	114	RXC_SOC
VCC_2V5	115	USER_IO115	USER_IO116	116	VCC_2V5
RXC_ENB-	117	USER_IO117	USER_IO118	118	RXC_CLAV
RXC_CLK	119	USER_IO119	USER_IO120	120	TXC_DATA0
TXC_DATA1	121	USER_IO121	USER_IO122	122	TXC_DATA2
TXC_DATA3	123	USER_IO123	USER_IO124	124	TXC_DATA4
TXC_DATA5	125	USER_IO125	USER_IO126	126	TXC_DATA6
GND	127	USER_IO127	USER_IO128	128	GND
TXC_DATA7	129	USER_IO129	USER_IO130	130	TXC_PAR
TXC_SOC	131	USER_IO131	USER_IO132	132	TXC_ENB-
TXC_CLAV	133	USER_IO133	USER_IO134	134	TXC_CLK
RCLKA	135	USER_IO135	USER_IO136	136	RCLKB
TX_CLK	137	USER_IO137	USER_IO138	138	RX_CLK
VCC_3V	139	USER_IO139	USER_IO140	140	VCC_3V
TXD0	141	USER_IO141	USER_IO142	142	TXD1
TXD2	143	USER_IO143	USER_IO144	144	TXD3
RXD0	145	USER_IO145	USER_IO146	146	RXD1
RXD2	147	USER_IO147	USER_IO148	148	RXD3
VCC_3V	149	USER_IO149	USER_IO150	150	VCC_3V
TX_ER	151	USER_IO151	USER_IO152	152	TX_EN
RX_DV	153	USER_IO153	USER_IO154	154	RX_ER
MT9044_19O	155	USER_IO155	USER_IO156	156	
	157	USER_IO157	USER_IO158	158	VCC_3V
GND	159	USER_IO159	USER_IO160	160	GND

177983-8 SMT
Mezzanine receptacle
2100-00043

Place one 10uF and one .1uF
capacitor near the connector.

VCC_2V5
C8 10uF 16V 10% Tan "B" 1500-00009
C16 1uF 50V 10% Cer. 0805 1500-00053

Place one 10uF and one .1uF
capacitor near the connector.

VCC_3V
C6 10uF 16V 10% Tan "B" 1500-00009
C21 1uF 50V 10% Cer. 0805 1500-00053

Place one 10uF and one .1uF
capacitor near the connector.

VCC_5V
C10 10uF 16V 10% Tan "B" 1500-00009
C3 1uF 50V 10% Cer. 0805 1500-00053

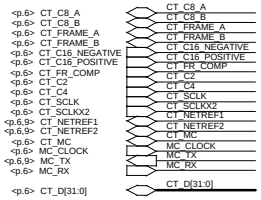
ZARLINK Semiconductor - Global Design Support

Title: MT90503 Mezzanine Board — Left Connector

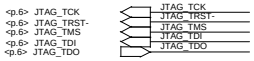
Size	Document Number	Designed By:	Checked By:	Rev
C	1000-001			01

Date: Friday, November 17, 2000 Sheet 4 of 9

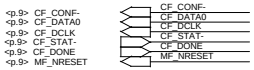
H.100 Clocks and data



JTAG test signals.

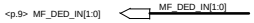


Mezzanine FPGA configuration signals

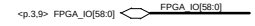


MCA2 Interrupts

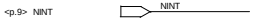
To MF

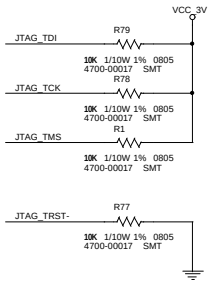


Multi-function IO pins sent to Mezzanine FPGA.

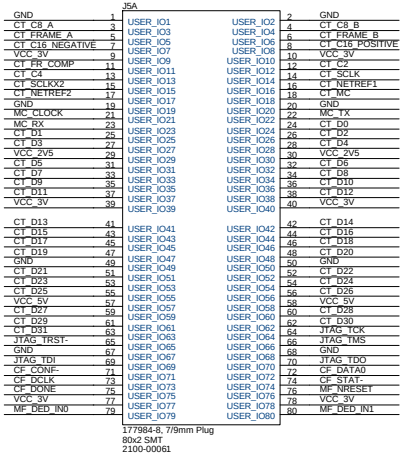


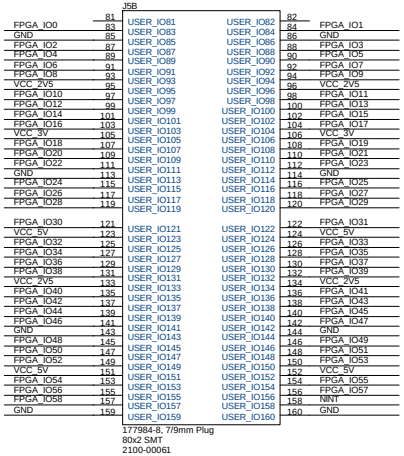
To PCI FPGA



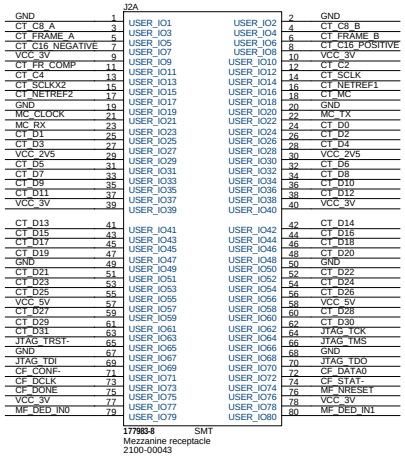


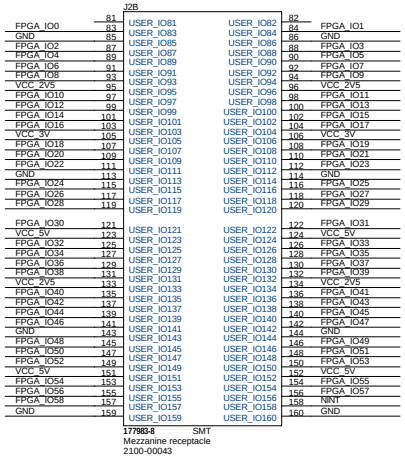
Assembled on solder side of Mezzanine Card

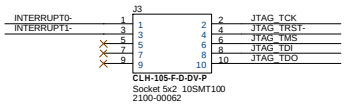




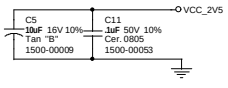
Assembled on component side of Mezzanine Card







Place one 10uF and one .1uF capacitor near the connector.



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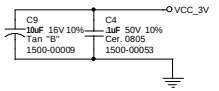
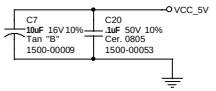
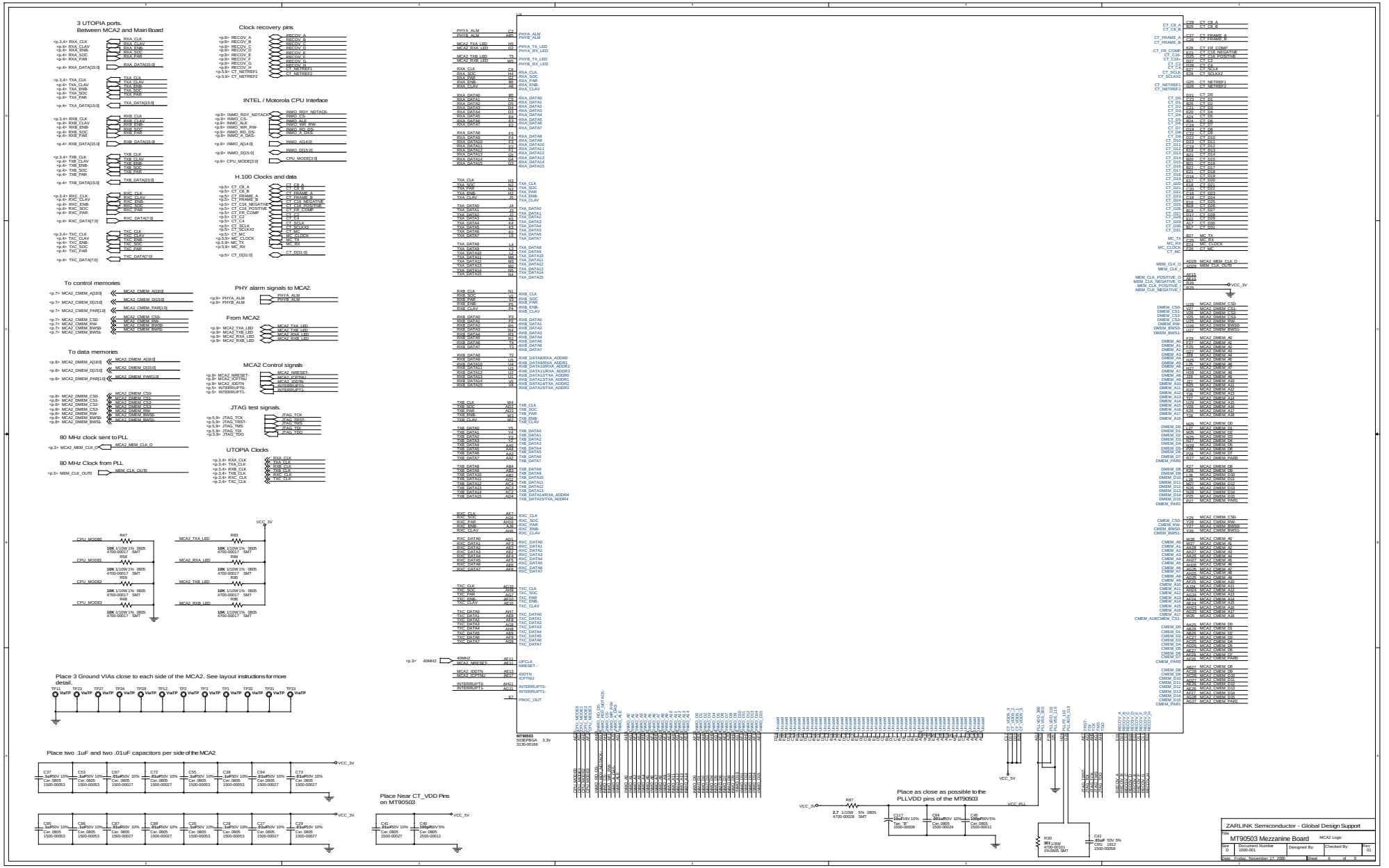


Place one 10uF and one .1uF capacitor near the connector.



ZARLINK Semiconductor - Global Design Support

Title: MT90503 Mezzanine Board — Right Connector				
Size: C	Document Number: 1000-001	Designed By:	Checked By:	Rev: 01
Date: Friday, November 17, 2000	Sheet 5 of 9			


3 UTOPIA ports.
Between MCA2 and Main Board
Clock recovery pins
INTEL / Motorola CPU Interface
H.100 Clocks and data
To control memories
PHY alarm signals to MCA2.
From MCA2
To data memories
MCA2 Control signals
80 MHz clock sent to PLL
JTAG test signals.
80 MHz Clock from PLL
UTOPIA Clocks
Place 3 Ground VIAs close to each side of the MCA2. See layout instructions for more detail.
Place two .1uF and two .01uF capacitors per side of the MCA2
Place Near CT_VDD Pins on MT90503
Place as close as possible to the PLLVDD pins of the MT90503
ZARLINK Semiconductor - Global Design Support
MT90503 Mezzanine Board
MCA2 Logic
Document Number 1009-001
Designed By:
Checked By:
Rev 01
Friday, November 17, 2000
Sheet 6 of 9

From MCA2.

<p.6> MCA2_CMEM_A[18:0] — MCA2_CMEM_A[18:0]

<p.6> MCA2_CMEM_D[15:0] — MCA2_CMEM_D[15:0]

<p.6> MCA2_CMEM_PAR[1:0] — MCA2_CMEM_PAR[1:0]

<p.6> MCA2_CMEM_CS0- — MCA2_CMEM_CS0-

<p.6> MCA2_CMEM_RW- — MCA2_CMEM_RW-

<p.6> MCA2_CMEM_BWS0- — MCA2_CMEM_BWS0-

<p.6> MCA2_CMEM_BWS1- — MCA2_CMEM_BWS1-

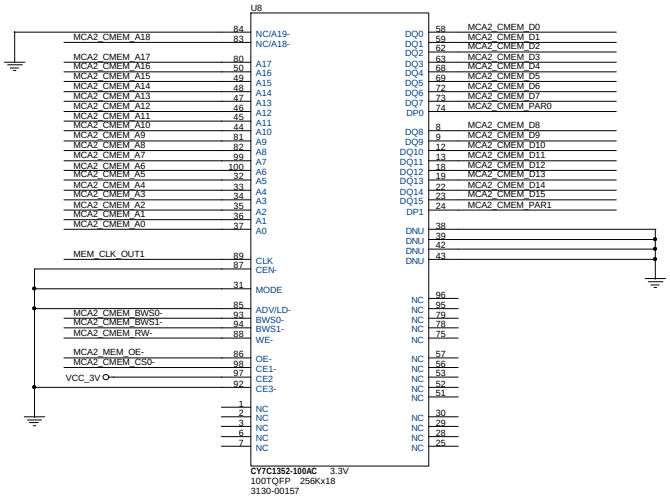
80 MHz Clock from PLL

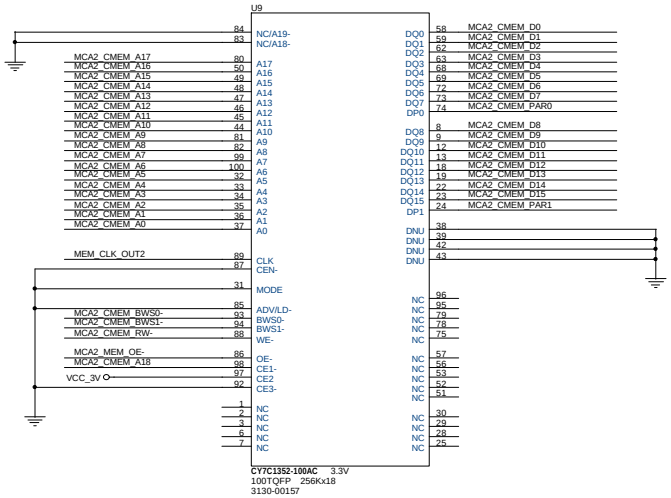
<p.3> MEM_CLK_OUT1 — MEM_CLK_OUT1

<p.3> MEM_CLK_OUT2 — MEM_CLK_OUT2

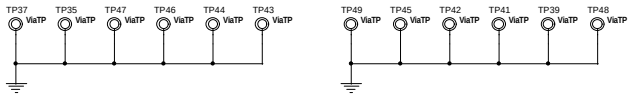
From Mezzanine FPGA

<p.9> MCA2_MEM_OE- — MCA2_MEM_OE-

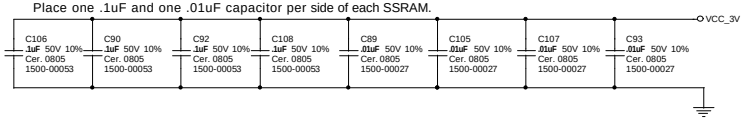




Place 6 ground VIAs around each memory. See layout instructions for more information.



Place one .1uF and one .01uF capacitor per side of each SSRAM.



ZARLINK Semiconductor - Global Design Support

Title: MT90503 Mezzanine Board — Control Memory

Size	Document Number	Designed By:	Checked By:	Rev
C	1000-001			01

Date: Friday, November 17, 2000 Sheet 7 of 9

From MCA2

<p.6> MCA2_DMEM_A[18:0] — MCA2_DMEM_A[18:0]

<p.6> MCA2_DMEM_D[15:0] — MCA2_DMEM_D[15:0]

<p.6> MCA2_DMEM_PAR[1:0] — MCA2_DMEM_PAR[1:0]

<p.6> MCA2_DMEM_CS0- — MCA2_DMEM_CS0-
<p.6> MCA2_DMEM_CS1- — MCA2_DMEM_CS1-
<p.6> MCA2_DMEM_CS2- — MCA2_DMEM_CS2-
<p.6> MCA2_DMEM_CS3- — MCA2_DMEM_CS3-
<p.6> MCA2_DMEM_RW- — MCA2_DMEM_RW-
<p.6> MCA2_DMEM_BWS0- — MCA2_DMEM_BWS0-
<p.6> MCA2_DMEM_BWS1- — MCA2_DMEM_BWS1-

80 MHz Clock from PLL

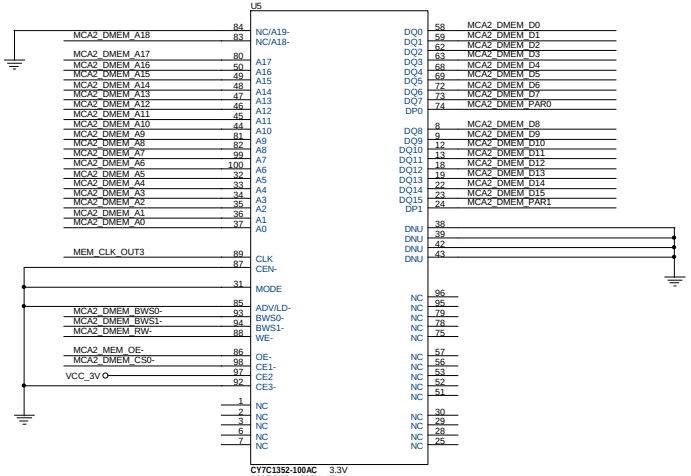
<p.3> MEM_CLK_OUT3 — MEM_CLK_OUT3
<p.3> MEM_CLK_OUT4 — MEM_CLK_OUT4
<p.3> MEM_CLK_OUT5 — MEM_CLK_OUT5
<p.3> MEM_CLK_OUT6 — MEM_CLK_OUT6

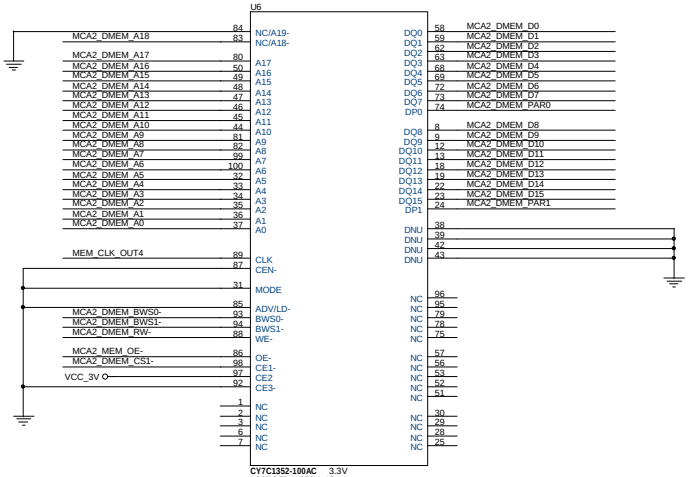
From Mezzanine FPGA

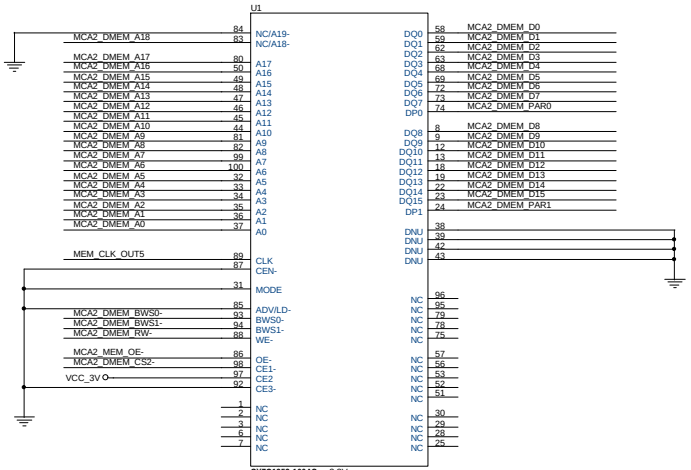
<p.9> MCA2_MEM_OE- — MCA2_MEM_OE-

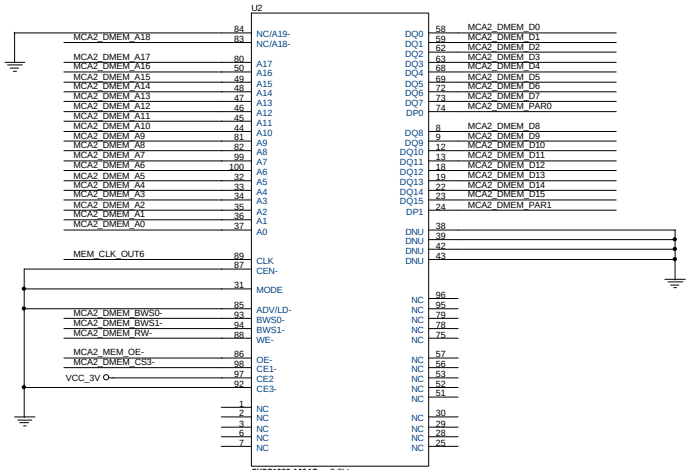
Place 6 ground VIAs around each memory.
See layout instructions for more information.

TP25 TP34 TP16 TP18 TP29 TP36 ViaTP
TP26 TP20 TP38 TP40 TP22 TP30 ViaTP
TP4 TP17 TP15 TP5 TP13 TP9 ViaTP
TP21 TP8 TP14 TP10 TP19 TP7 ViaTP

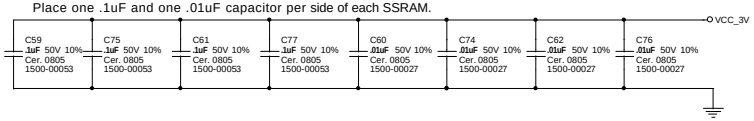








Place one .1uF and one .01uF capacitor per side of each SSRAM.



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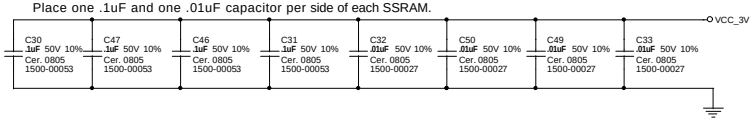
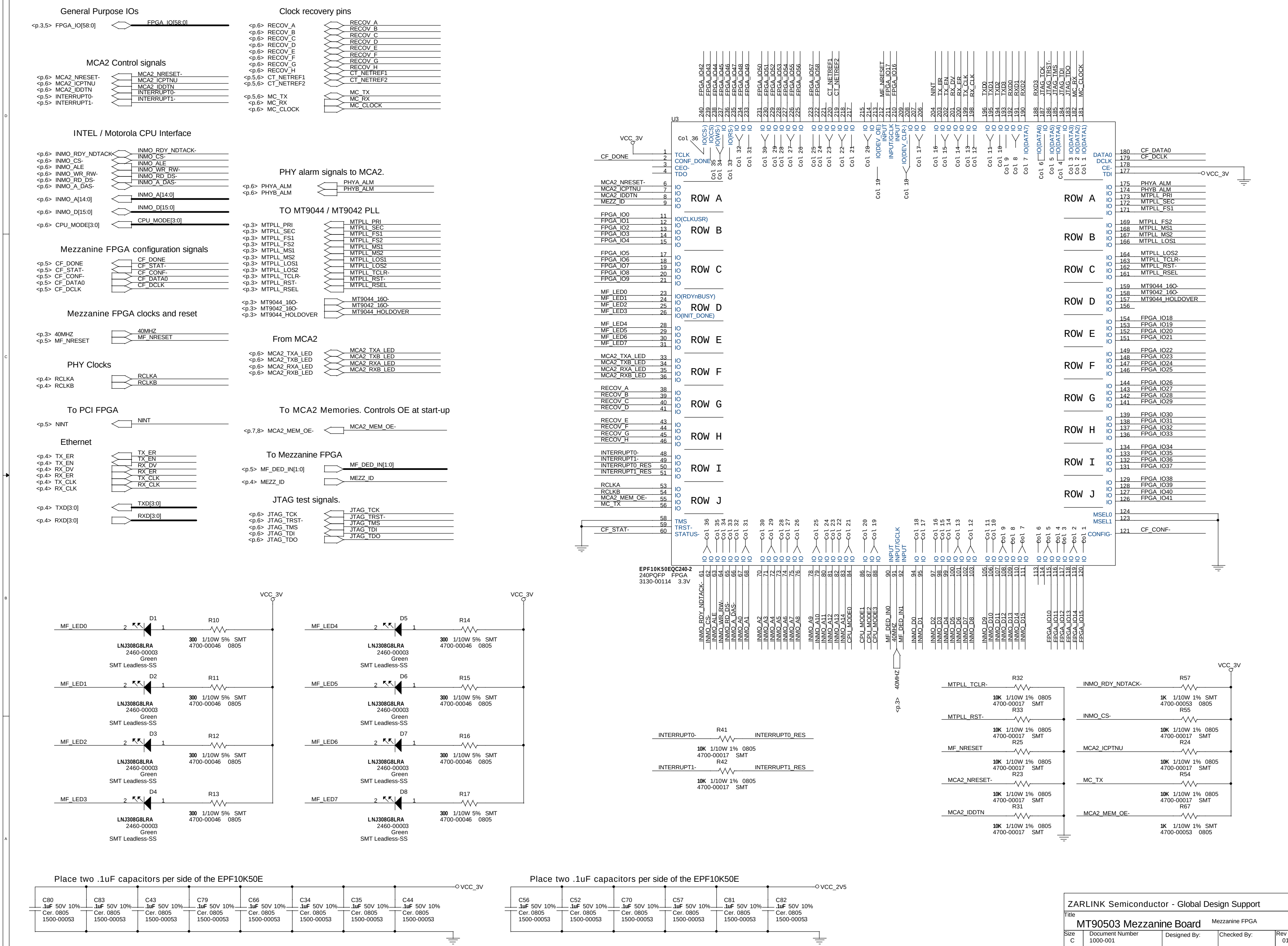


ZARLINK Semiconductor - Global Design Support

Title: MT90503 Mezzanine Board — Data Memory

Size	Document Number	Designed By:	Checked By:	Rev
C	1000-001			01

Date: Friday, November 17, 2000 Sheet 8 of 9



ZARLINK Semiconductor - Global Design Support

Title: MT90503 Mezzanine Board	Mezzanine FPGA		
Size: C	Document Number: 1000-001	Designed By:	Checked By:
Rev: 01			
Date: Friday, November 17, 2000	Sheet 9 of 9		