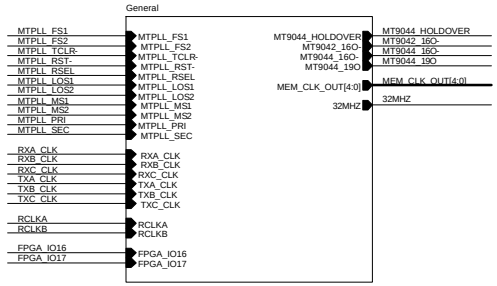
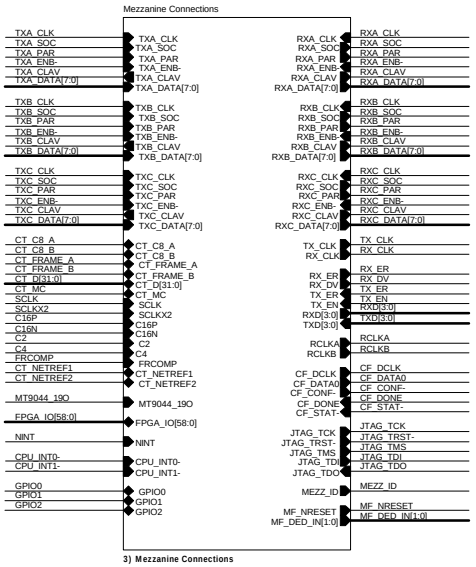
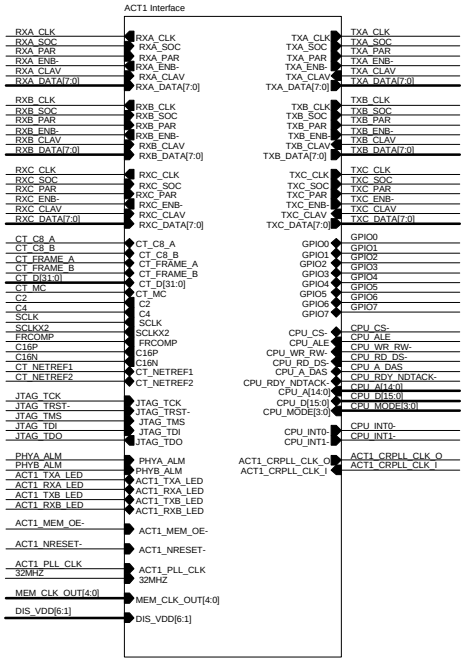


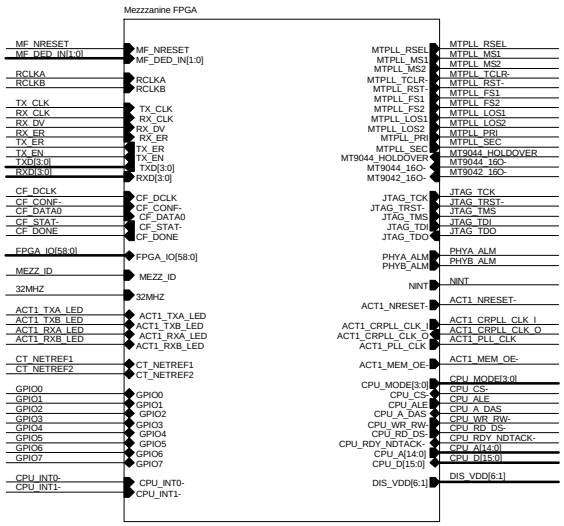
2) General



3) Mezzanine Connections



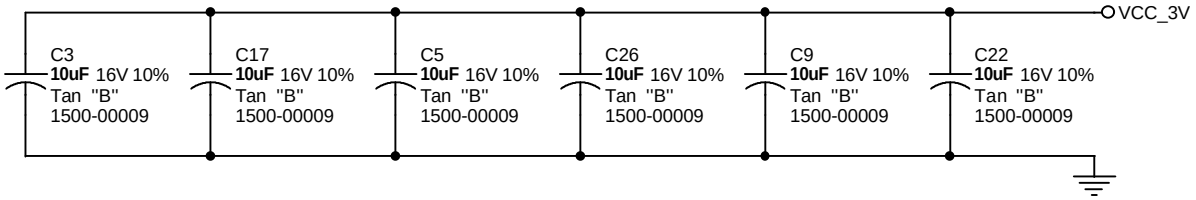
4) ACT1 Interface



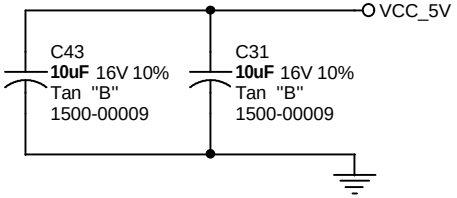
5) Mezzzanine FPGA

ZARLINK Semiconductor - Global Design Support					
Title: MT90502 Mezzanine Board — Interconnections					
Size: C	Document Number: 1000-002		Designed By:	Checked By:	Rev: 01
Date: Friday, November 17, 2000		Sheet 1 of 9			

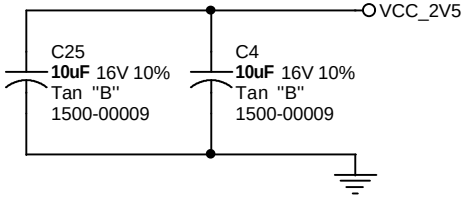
Spread the bulk decoupling capacitors on the board.



Spread the bulk decoupling capacitors on the board.

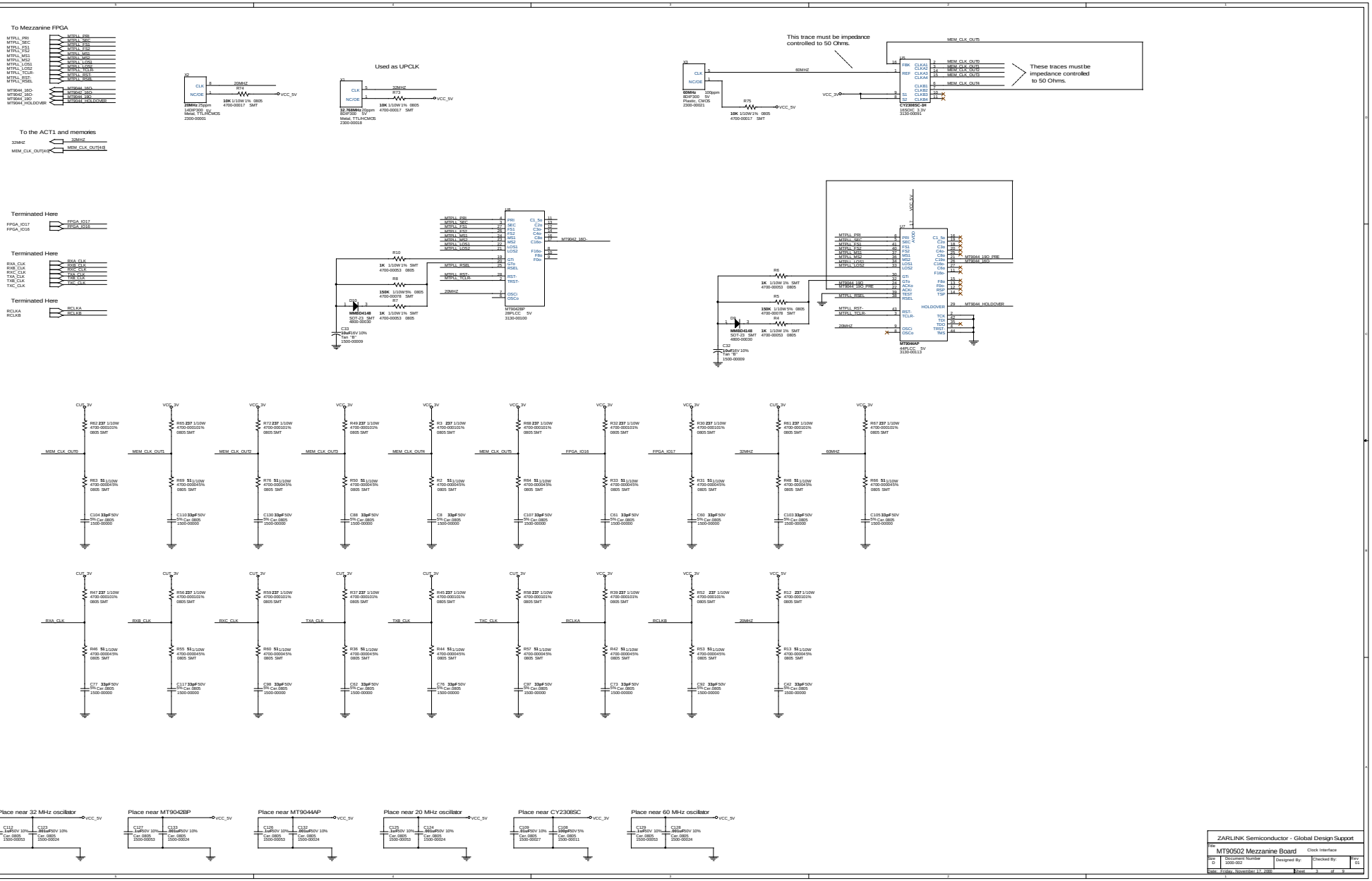


Spread the bulk decoupling capacitors on the board.



ZARLINK Semiconductor - Global Design Support

Title: MT90502 Mezzanine Board — Power Interface				
Size: A	Document Number: 1000-002	Designed By:	Checked By:	Rev: 01
Date: Friday, November 17, 2000		Sheet 2 of 9		


To Mezzanine FPGA
MTPLL_PRI
MTPLL_SEC
MTPLL_FS1
MTPLL_FS2
MTPLL_MS1
MTPLL_MS2
MTPLL_LOS1
MTPLL_LOS2
MTPLL_TCLR-
MTPLL_RST-
MTPLL_RSEL
MT9044_16O-
MT9042_16O-
MT9044_19O
MT9044_HOLDOVER
To the ACT1 and memories
32MHZ
MEM_CLK_OUT[4:0]
Terminated Here
FPGA_IO17
FPGA_IO16
RXA_CLK
RXB_CLK
RXC_CLK
TXA_CLK
TXB_CLK
TXC_CLK
RCLKA
RCLKB
Used as UPCLK
This trace must be impedance controlled to 50 Ohms.
These traces must be impedance controlled to 50 Ohms.
MEM_CLK_OUT5
60MHZ
20MHZ
VCC_5V
VCC_3V
MT9042_16O-
MT9044_19O
MT9044_HOLDOVER
Place near 32 MHz oscillator
Place near MT9042BP
Place near MT9044AP
Place near 20 MHz oscillator
Place near CY2308SC
Place near 60 MHz oscillator
ZARLINK Semiconductor - Global Design Support
MT90502 Mezzanine Board
Clock Interface

3 UTOPIA ports.
Between Main board and ACT1.

RXA_CLK
RXA_CLAV
RXA_ENB-
RXA_SOC
RXA_PAR
RXA_DATA[7:0]

TXA_CLK
TXA_CLAV
TXA_ENB-
TXA_SOC
TXA_PAR
TXA_DATA[7:0]

RXB_CLK
RXB_CLAV
RXB_ENB-
RXB_SOC
RXB_PAR
RXB_DATA[7:0]

TXB_CLK
TXB_CLAV
TXB_ENB-
TXB_SOC
TXB_PAR
TXB_DATA[7:0]

RXC_CLK
RXC_CLAV
RXC_ENB-
RXC_SOC
RXC_PAR
RXC_DATA[7:0]

TXC_CLK
TXC_CLAV
TXC_ENB-
TXC_SOC
TXC_PAR
TXC_DATA[7:0]

19.44 MHz Clock from PLL.

MT9044_19O

UTOPIA PHY clocks.
From PHYs A & B on Main Board
to FPGA on Mezzanine Board.

RCLKA
RCLKB

Ethernet

TX_ER
TX_EN
RX_DV
RX_ER
TX_CLK
RX_CLK
TXD[3:0]
RXD[3:0]

Sent to Mezzanine FPGA to identify
the board below it

MEZZ_ID

Assembled on solder side of Mezzanine Card

J4A

GND	1	USER_IO1	USER_IO2	2	GND
RXA_DATA0	3	USER_IO3	USER_IO4	4	RXA_DATA1
RXA_DATA2	5	USER_IO5	USER_IO6	6	RXA_DATA3
RXA_DATA4	7	USER_IO7	USER_IO8	8	RXA_DATA5
RXA_DATA6	9	USER_IO9	USER_IO10	10	RXA_DATA7
	11	USER_IO11	USER_IO12	12	
VCC_5V	13	USER_IO13	USER_IO14	14	VCC_5V
	15	USER_IO15	USER_IO16	16	
	17	USER_IO17	USER_IO18	18	
	19	USER_IO19	USER_IO20	20	
RXA_PAR	21	USER_IO21	USER_IO22	22	RXA_SOC
GND	23	USER_IO23	USER_IO24	24	GND
RXA_ENB-	25	USER_IO25	USER_IO26	26	RXA_CLAV
RXA_CLK	27	USER_IO27	USER_IO28	28	TXA_DATA0
TXA_DATA1	29	USER_IO29	USER_IO30	30	TXA_DATA2
TXA_DATA3	31	USER_IO31	USER_IO32	32	TXA_DATA4
TXA_DATA5	33	USER_IO33	USER_IO34	34	TXA_DATA6
VCC_3V	35	USER_IO35	USER_IO36	36	VCC_3V
TXA_DATA7	37	USER_IO37	USER_IO38	38	
	39	USER_IO39	USER_IO40	40	
	41	USER_IO41	USER_IO42	42	
	43	USER_IO43	USER_IO44	44	
	45	USER_IO45	USER_IO46	46	TXA_PAR
GND	47	USER_IO47	USER_IO48	48	GND
TXA_SOC	49	USER_IO49	USER_IO50	50	TXA_ENB-
TXA_CLAV	51	USER_IO51	USER_IO52	52	TXA_CLK
RXB_DATA0	53	USER_IO53	USER_IO54	54	RXA_DATA1
RXB_DATA2	55	USER_IO55	USER_IO56	56	RXB_DATA3
RXB_DATA4	57	USER_IO57	USER_IO58	58	RXB_DATA5
VCC_2V5	59	USER_IO59	USER_IO60	60	VCC_2V5
RXB_DATA6	61	USER_IO61	USER_IO62	62	RXB_DATA7
	63	USER_IO63	USER_IO64	64	
	65	USER_IO65	USER_IO66	66	
	67	USER_IO67	USER_IO68	68	
GND	69	USER_IO69	USER_IO70	70	GND
	71	USER_IO71	USER_IO72	72	
RXB_PAR	73	USER_IO73	USER_IO74	74	RXB_SOC
RXB_ENB-	75	USER_IO75	USER_IO76	76	RXB_CLAV
RXB_CLK	77	USER_IO77	USER_IO78	78	TXB_DATA0
TXB_DATA1	79	USER_IO79	USER_IO80	80	TXB_DATA2

177984-8, 7/9mm Plug
80x2 SMT
2100-00061

J4B

VCC_5V	81	USER_IO81	USER_IO82	82	VCC_5V
TXB_DATA3	83	USER_IO83	USER_IO84	84	TXB_DATA4
TXB_DATA5	85	USER_IO85	USER_IO86	86	TXB_DATA6
TXB_DATA7	87	USER_IO87	USER_IO88	88	
	89	USER_IO89	USER_IO90	90	
VCC_3V	91	USER_IO91	USER_IO92	92	VCC_3V
	93	USER_IO93	USER_IO94	94	
	95	USER_IO95	USER_IO96	96	
	97	USER_IO97	USER_IO98	98	TXB_PAR
TXB_SOC	99	USER_IO99	USER_IO100	100	TXB_ENB-
TXB_CLAV	101	USER_IO101	USER_IO102	102	TXB_CLK
GND	103	USER_IO103	USER_IO104	104	GND
RXC_DATA0	105	USER_IO105	USER_IO106	106	RXC_DATA1
RXC_DATA2	107	USER_IO107	USER_IO108	108	RXC_DATA3
RXC_DATA4	109	USER_IO109	USER_IO110	110	RXC_DATA5
RXC_DATA6	111	USER_IO111	USER_IO112	112	RXC_DATA7
RXC_PAR	113	USER_IO113	USER_IO114	114	RXC_SOC
VCC_2V5	115	USER_IO115	USER_IO116	116	VCC_2V5
RXC_ENB-	117	USER_IO117	USER_IO118	118	RXC_CLAV
RXC_CLK	119	USER_IO119	USER_IO120	120	TXC_DATA0
TXC_DATA1	121	USER_IO121	USER_IO122	122	TXC_DATA2
TXC_DATA3	123	USER_IO123	USER_IO124	124	TXC_DATA4
TXC_DATA5	125	USER_IO125	USER_IO126	126	TXC_DATA6
GND	127	USER_IO127	USER_IO128	128	GND
TXC_DATA7	129	USER_IO129	USER_IO130	130	TXC_PAR
TXC_SOC	131	USER_IO131	USER_IO132	132	TXC_ENB-
TXC_CLAV	133	USER_IO133	USER_IO134	134	TXC_CLK
RCLKA	135	USER_IO135	USER_IO136	136	RCLKB
TX_CLK	137	USER_IO137	USER_IO138	138	RX_CLK
VCC_3V	139	USER_IO139	USER_IO140	140	VCC_3V
TXD0	141	USER_IO141	USER_IO142	142	TXD1
TXD2	143	USER_IO143	USER_IO144	144	TXD3
RXD0	145	USER_IO145	USER_IO146	146	RXD1
RXD2	147	USER_IO147	USER_IO148	148	RXD3
VCC_3V	149	USER_IO149	USER_IO150	150	VCC_3V
TX_ER	151	USER_IO151	USER_IO152	152	TX_EN
RX_DV	153	USER_IO153	USER_IO154	154	RX_ER
MT9044_19O	155	USER_IO155	USER_IO156	156	
	157	USER_IO157	USER_IO158	158	MEZZ_ID
GND	159	USER_IO159	USER_IO160	160	GND

177984-8, 7/9mm Plug
80x2 SMT
2100-00061

Assembled on component side of Mezzanine Card

J1A

GND	1	USER_IO1	USER_IO2	2	GND
RXA_DATA0	3	USER_IO3	USER_IO4	4	RXA_DATA1
RXA_DATA2	5	USER_IO5	USER_IO6	6	RXA_DATA3
RXA_DATA4	7	USER_IO7	USER_IO8	8	RXA_DATA5
RXA_DATA6	9	USER_IO9	USER_IO10	10	RXA_DATA7
	11	USER_IO11	USER_IO12	12	
VCC_5V	13	USER_IO13	USER_IO14	14	VCC_5V
	15	USER_IO15	USER_IO16	16	
	17	USER_IO17	USER_IO18	18	
	19	USER_IO19	USER_IO20	20	
RXA_PAR	21	USER_IO21	USER_IO22	22	RXA_SOC
GND	23	USER_IO23	USER_IO24	24	GND
RXA_ENB-	25	USER_IO25	USER_IO26	26	RXA_CLAV
RXA_CLK	27	USER_IO27	USER_IO28	28	TXA_DATA0
TXA_DATA1	29	USER_IO29	USER_IO30	30	TXA_DATA2
TXA_DATA3	31	USER_IO31	USER_IO32	32	TXA_DATA4
TXA_DATA5	33	USER_IO33	USER_IO34	34	TXA_DATA6
VCC_3V	35	USER_IO35	USER_IO36	36	VCC_3V
TXA_DATA7	37	USER_IO37	USER_IO38	38	
	39	USER_IO39	USER_IO40	40	
	41	USER_IO41	USER_IO42	42	
	43	USER_IO43	USER_IO44	44	
	45	USER_IO45	USER_IO46	46	TXA_PAR
GND	47	USER_IO47	USER_IO48	48	GND
TXA_SOC	49	USER_IO49	USER_IO50	50	TXA_ENB-
TXA_CLAV	51	USER_IO51	USER_IO52	52	TXA_CLK
RXB_DATA0	53	USER_IO53	USER_IO54	54	RXB_DATA1
RXB_DATA2	55	USER_IO55	USER_IO56	56	RXB_DATA3
RXB_DATA4	57	USER_IO57	USER_IO58	58	RXB_DATA5
VCC_2V5	59	USER_IO59	USER_IO60	60	VCC_2V5
RXB_DATA6	61	USER_IO61	USER_IO62	62	RXB_DATA7
	63	USER_IO63	USER_IO64	64	
	65	USER_IO65	USER_IO66	66	
	67	USER_IO67	USER_IO68	68	
GND	69	USER_IO69	USER_IO70	70	GND
	71	USER_IO71	USER_IO72	72	
RXB_PAR	73	USER_IO73	USER_IO74	74	RXB_SOC
RXB_ENB-	75	USER_IO75	USER_IO76	76	RXB_CLAV
RXB_CLK	77	USER_IO77	USER_IO78	78	TXB_DATA0
TXB_DATA1	79	USER_IO79	USER_IO80	80	TXB_DATA2

177983-8 SMT
Mezzanine receptacle
2100-00043

J1B

VCC_5V	81	USER_IO81	USER_IO82	82	VCC_5V
TXB_DATA3	83	USER_IO83	USER_IO84	84	TXB_DATA4
TXB_DATA5	85	USER_IO85	USER_IO86	86	TXB_DATA6
TXB_DATA7	87	USER_IO87	USER_IO88	88	
	89	USER_IO89	USER_IO90	90	
VCC_3V	91	USER_IO91	USER_IO92	92	VCC_3V
	93	USER_IO93	USER_IO94	94	
	95	USER_IO95	USER_IO96	96	
	97	USER_IO97	USER_IO98	98	TXB_PAR
TXB_SOC	99	USER_IO99	USER_IO100	100	TXB_ENB-
TXB_CLAV	101	USER_IO101	USER_IO102	102	TXB_CLK
GND	103	USER_IO103	USER_IO104	104	GND
RXC_DATA0	105	USER_IO105	USER_IO106	106	RXC_DATA1
RXC_DATA2	107	USER_IO107	USER_IO108	108	RXC_DATA3
RXC_DATA4	109	USER_IO109	USER_IO110	110	RXC_DATA5
RXC_DATA6	111	USER_IO111	USER_IO112	112	RXC_DATA7
RXC_PAR	113	USER_IO113	USER_IO114	114	RXC_SOC
VCC_2V5	115	USER_IO115	USER_IO116	116	VCC_2V5
RXC_ENB-	117	USER_IO117	USER_IO118	118	RXC_CLAV
RXC_CLK	119	USER_IO119	USER_IO120	120	TXC_DATA0
TXC_DATA1	121	USER_IO121	USER_IO122	122	TXC_DATA2
TXC_DATA3	123	USER_IO123	USER_IO124	124	TXC_DATA4
TXC_DATA5	125	USER_IO125	USER_IO126	126	TXC_DATA6
GND	127	USER_IO127	USER_IO128	128	GND
TXC_DATA7	129	USER_IO129	USER_IO130	130	TXC_PAR
TXC_SOC	131	USER_IO131	USER_IO132	132	TXC_ENB-
TXC_CLAV	133	USER_IO133	USER_IO134	134	TXC_CLK
RCLKA	135	USER_IO135	USER_IO136	136	RCLKB
TX_CLK	137	USER_IO137	USER_IO138	138	RX_CLK
VCC_3V	139	USER_IO139	USER_IO140	140	VCC_3V
TXD0	141	USER_IO141	USER_IO142	142	TXD1
TXD2	143	USER_IO143	USER_IO144	144	TXD3
RXD0	145	USER_IO145	USER_IO146	146	RXD1
RXD2	147	USER_IO147	USER_IO148	148	RXD3
VCC_3V	149	USER_IO149	USER_IO150	150	VCC_3V
TX_ER	151	USER_IO151	USER_IO152	152	TX_EN
RX_DV	153	USER_IO153	USER_IO154	154	RX_ER
MT9044_19O	155	USER_IO155	USER_IO156	156	
	157	USER_IO157	USER_IO158	158	VCC_3V
GND	159	USER_IO159	USER_IO160	160	GND

177983-8 SMT
Mezzanine receptacle
2100-00043

Place one 10uF and one .1uF
capacitor near the connector.

VCC_2V5
C16 10uF 16V 10% Tan "B" 1500-00009
C30 1uF 50V 10% Cer. 0805 1500-00053

Place one 10uF and one .1uF
capacitor near the connector.

VCC_3V
C40 10uF 16V 10% Tan "B" 1500-00009
C12 1uF 50V 10% Cer. 0805 1500-00053

Place one 10uF and one .1uF
capacitor near the connector.

VCC_5V
C24 10uF 16V 10% Tan "B" 1500-00009
C2 1uF 50V 10% Cer. 0805 1500-00053

ZARLINK Semiconductor - Global Design Support

Title: MT90502 Mezzanine Board — Left Connector

Size	Document Number	Designed By:	Checked By:	Rev
C	1000-002			01

Date: Friday, November 17, 2000 Sheet 4 of 9

H.100 Clocks and data

CT_C8_A
CT_C8_B
CT_FRAME_A
CT_FRAME_B
C16N
C16P
FRCOMP
C2
C4
SCLK
SCLKX2
CT_NETREF1
CT_NETREF2
CT_MC
CT_D[31:0]

JTAG test signals.

JTAG_TCK
JTAG_TRST-
JTAG_TMS
JTAG_TDI
JTAG_TDO

Mezzanine FPGA configuration signals

CF_CONF-
CF_DATA0
CF_DCLK
CF_STAT-
CF_DONE
MF_NRESET

From ACT1

GPIO0
GPIO1
GPIO2

ACT1 Interrupts

CPU_INT0-
CPU_INT1-

To MF

MF_DED_IN[1:0]

Multi-function IO pins sent to Mezzanine FPGA.

FPGA_IO[58:0]

To PCI FPGA

NINT

VCC_3V

R80 — JTAG_TDI
R77 — JTAG_TCK
R79 — JTAG_TMS
R78 — JTAG_TRST-

10K 1/10W 1% 0805
4700-00017 SMT

J3

CPU_INT0-	1	2	JTAG_TCK
CPU_INT1-	3	4	JTAG_TRST-
	5	6	JTAG_TMS
	7	8	JTAG_TDI
	9	10	JTAG_TDO

CLH-105-F-D-DV-P
Socket 5x2 10SMT100
2100-00062

Place one 10uF and one .1uF capacitor near the connector.

VCC_2V5: C15 10uF 16V 10% Tan "B" 1500-00009; C39 .1uF 50V 10% Cer. 0805 1500-00053

Place one 10uF and one .1uF capacitor near the connector.

VCC_3V: C29 10uF 16V 10% Tan "B" 1500-00009; C11 .1uF 50V 10% Cer. 0805 1500-00053

Place one 10uF and one .1uF capacitor near the connector.

VCC_5V: C23 10uF 16V 10% Tan "B" 1500-00009; C41 .1uF 50V 10% Cer. 0805 1500-00053

Assembled on solder side of Mezzanine Card

J5A

GND	1	USER_IO1	USER_IO2	2	GND
CT_C8_A	3	USER_IO3	USER_IO4	4	CT_C8_B
CT_FRAME_A	5	USER_IO5	USER_IO6	6	CT_FRAME_B
C16N	7	USER_IO7	USER_IO8	8	C16P
VCC_3V	9	USER_IO9	USER_IO10	10	VCC_3V
FRCOMP	11	USER_IO11	USER_IO12	12	C2
C4	13	USER_IO13	USER_IO14	14	SCLK
SCLKX2	15	USER_IO15	USER_IO16	16	CT_NETREF1
CT_NETREF2	17	USER_IO17	USER_IO18	18	CT_MC
GND	19	USER_IO19	USER_IO20	20	GND
GPIO0	21	USER_IO21	USER_IO22	22	GPIO2
GPIO1	23	USER_IO23	USER_IO24	24	CT_D0
CT_D1	25	USER_IO25	USER_IO26	26	CT_D2
CT_D3	27	USER_IO27	USER_IO28	28	CT_D4
VCC_2V5	29	USER_IO29	USER_IO30	30	VCC_2V5
CT_D5	31	USER_IO31	USER_IO32	32	CT_D6
CT_D7	33	USER_IO33	USER_IO34	34	CT_D8
CT_D9	35	USER_IO35	USER_IO36	36	CT_D10
CT_D11	37	USER_IO37	USER_IO38	38	CT_D12
VCC_3V	39	USER_IO39	USER_IO40	40	VCC_3V
CT_D13	41	USER_IO41	USER_IO42	42	CT_D14
CT_D15	43	USER_IO43	USER_IO44	44	CT_D16
CT_D17	45	USER_IO45	USER_IO46	46	CT_D18
CT_D19	47	USER_IO47	USER_IO48	48	CT_D20
GND	49	USER_IO49	USER_IO50	50	GND
CT_D21	51	USER_IO51	USER_IO52	52	CT_D22
CT_D23	53	USER_IO53	USER_IO54	54	CT_D24
CT_D25	55	USER_IO55	USER_IO56	56	CT_D26
VCC_5V	57	USER_IO57	USER_IO58	58	VCC_5V
CT_D27	59	USER_IO59	USER_IO60	60	CT_D28
CT_D29	61	USER_IO61	USER_IO62	62	CT_D30
CT_D31	63	USER_IO63	USER_IO64	64	JTAG_TCK
JTAG_TRST-	65	USER_IO65	USER_IO66	66	JTAG_TMS
GND	67	USER_IO67	USER_IO68	68	GND
JTAG_TDI	69	USER_IO69	USER_IO70	70	JTAG_TDO
CF_CONF-	71	USER_IO71	USER_IO72	72	CF_DATA0
CF_DCLK	73	USER_IO73	USER_IO74	74	CF_STAT-
CF_DONE	75	USER_IO75	USER_IO76	76	MF_NRESET
VCC_3V	77	USER_IO77	USER_IO78	78	VCC_3V
MF_DED_IN0	79	USER_IO79	USER_IO80	80	MF_DED_IN1

177984-8, 7/9mm Plug
80x2 SMT
2100-00061

J5B

FPGA_IO0	81	USER_IO81	USER_IO82	82	FPGA_IO1
GND	83	USER_IO83	USER_IO84	84	GND
FPGA_IO2	85	USER_IO85	USER_IO86	86	FPGA_IO3
FPGA_IO4	87	USER_IO87	USER_IO88	88	FPGA_IO5
FPGA_IO6	89	USER_IO89	USER_IO90	90	FPGA_IO7
FPGA_IO8	91	USER_IO91	USER_IO92	92	FPGA_IO9
VCC_2V5	93	USER_IO93	USER_IO94	94	VCC_2V5
FPGA_IO10	95	USER_IO95	USER_IO96	96	FPGA_IO11
FPGA_IO12	97	USER_IO97	USER_IO98	98	FPGA_IO13
FPGA_IO14	99	USER_IO99	USER_IO100	100	FPGA_IO15
FPGA_IO16	101	USER_IO101	USER_IO102	102	FPGA_IO17
VCC_3V	103	USER_IO103	USER_IO104	104	VCC_3V
FPGA_IO18	105	USER_IO105	USER_IO106	106	FPGA_IO19
FPGA_IO20	107	USER_IO107	USER_IO108	108	FPGA_IO21
FPGA_IO22	109	USER_IO109	USER_IO110	110	FPGA_IO23
GND	111	USER_IO111	USER_IO112	112	GND
FPGA_IO24	113	USER_IO113	USER_IO114	114	FPGA_IO25
FPGA_IO26	115	USER_IO115	USER_IO116	116	FPGA_IO27
FPGA_IO28	117	USER_IO117	USER_IO118	118	FPGA_IO29
FPGA_IO30	119	USER_IO119	USER_IO120	120	FPGA_IO31
VCC_5V	121	USER_IO121	USER_IO122	122	VCC_5V
FPGA_IO32	123	USER_IO123	USER_IO124	124	FPGA_IO33
FPGA_IO34	125	USER_IO125	USER_IO126	126	FPGA_IO35
FPGA_IO36	127	USER_IO127	USER_IO128	128	FPGA_IO37
FPGA_IO38	129	USER_IO129	USER_IO130	130	FPGA_IO39
VCC_2V5	131	USER_IO131	USER_IO132	132	VCC_2V5
FPGA_IO40	133	USER_IO133	USER_IO134	134	FPGA_IO41
FPGA_IO42	135	USER_IO135	USER_IO136	136	FPGA_IO43
FPGA_IO44	137	USER_IO137	USER_IO138	138	FPGA_IO45
FPGA_IO46	139	USER_IO139	USER_IO140	140	FPGA_IO47
GND	141	USER_IO141	USER_IO142	142	GND
FPGA_IO48	143	USER_IO143	USER_IO144	144	FPGA_IO49
FPGA_IO50	145	USER_IO145	USER_IO146	146	FPGA_IO51
FPGA_IO52	147	USER_IO147	USER_IO148	148	FPGA_IO53
VCC_5V	149	USER_IO149	USER_IO150	150	VCC_5V
FPGA_IO54	151	USER_IO151	USER_IO152	152	FPGA_IO55
FPGA_IO56	153	USER_IO153	USER_IO154	154	FPGA_IO57
FPGA_IO58	155	USER_IO155	USER_IO156	156	NINT
GND	157	USER_IO157	USER_IO158	158	NINT
	159	USER_IO159	USER_IO160	160	GND

177984-8, 7/9mm Plug
80x2 SMT
2100-00061

Assembled on component side of Mezzanine Card

J2A

GND	1	USER_IO1	USER_IO2	2	GND
CT_C8_A	3	USER_IO3	USER_IO4	4	CT_C8_B
CT_FRAME_A	5	USER_IO5	USER_IO6	6	CT_FRAME_B
C16N	7	USER_IO7	USER_IO8	8	C16P
VCC_3V	9	USER_IO9	USER_IO10	10	VCC_3V
FRCOMP	11	USER_IO11	USER_IO12	12	C2
C4	13	USER_IO13	USER_IO14	14	SCLK
SCLKX2	15	USER_IO15	USER_IO16	16	CT_NETREF1
CT_NETREF2	17	USER_IO17	USER_IO18	18	CT_MC
GND	19	USER_IO19	USER_IO20	20	GND
GPIO0	21	USER_IO21	USER_IO22	22	GPIO2
GPIO1	23	USER_IO23	USER_IO24	24	CT_D0
CT_D1	25	USER_IO25	USER_IO26	26	CT_D2
CT_D3	27	USER_IO27	USER_IO28	28	CT_D4
VCC_2V5	29	USER_IO29	USER_IO30	30	VCC_2V5
CT_D5	31	USER_IO31	USER_IO32	32	CT_D6
CT_D7	33	USER_IO33	USER_IO34	34	CT_D8
CT_D9	35	USER_IO35	USER_IO36	36	CT_D10
CT_D11	37	USER_IO37	USER_IO38	38	CT_D12
VCC_3V	39	USER_IO39	USER_IO40	40	VCC_3V
CT_D13	41	USER_IO41	USER_IO42	42	CT_D14
CT_D15	43	USER_IO43	USER_IO44	44	CT_D16
CT_D17	45	USER_IO45	USER_IO46	46	CT_D18
CT_D19	47	USER_IO47	USER_IO48	48	CT_D20
GND	49	USER_IO49	USER_IO50	50	GND
CT_D21	51	USER_IO51	USER_IO52	52	CT_D22
CT_D23	53	USER_IO53	USER_IO54	54	CT_D24
CT_D25	55	USER_IO55	USER_IO56	56	CT_D26
VCC_5V	57	USER_IO57	USER_IO58	58	VCC_5V
CT_D27	59	USER_IO59	USER_IO60	60	CT_D28
CT_D29	61	USER_IO61	USER_IO62	62	CT_D30
CT_D31	63	USER_IO63	USER_IO64	64	JTAG_TCK
JTAG_TRST-	65	USER_IO65	USER_IO66	66	JTAG_TMS
GND	67	USER_IO67	USER_IO68	68	GND
JTAG_TDI	69	USER_IO69	USER_IO70	70	JTAG_TDO
CF_CONF-	71	USER_IO71	USER_IO72	72	CF_DATA0
CF_DCLK	73	USER_IO73	USER_IO74	74	CF_STAT-
CF_DONE	75	USER_IO75	USER_IO76	76	MF_NRESET
VCC_3V	77	USER_IO77	USER_IO78	78	VCC_3V
MF_DED_IN0	79	USER_IO79	USER_IO80	80	MF_DED_IN1

177983-8 SMT
Mezzanine receptacle
2100-00043

J2B

FPGA_IO0	81	USER_IO81	USER_IO82	82	FPGA_IO1
GND	83	USER_IO83	USER_IO84	84	GND
FPGA_IO2	85	USER_IO85	USER_IO86	86	FPGA_IO3
FPGA_IO4	87	USER_IO87	USER_IO88	88	FPGA_IO5
FPGA_IO6	89	USER_IO89	USER_IO90	90	FPGA_IO7
FPGA_IO8	91	USER_IO91	USER_IO92	92	FPGA_IO9
VCC_2V5	93	USER_IO93	USER_IO94	94	VCC_2V5
FPGA_IO10	95	USER_IO95	USER_IO96	96	FPGA_IO11
FPGA_IO12	97	USER_IO97	USER_IO98	98	FPGA_IO13
FPGA_IO14	99	USER_IO99	USER_IO100	100	FPGA_IO15
FPGA_IO16	101	USER_IO101	USER_IO102	102	FPGA_IO17
VCC_3V	103	USER_IO103	USER_IO104	104	VCC_3V
FPGA_IO18	105	USER_IO105	USER_IO106	106	FPGA_IO19
FPGA_IO20	107	USER_IO107	USER_IO108	108	FPGA_IO21
FPGA_IO22	109	USER_IO109	USER_IO110	110	FPGA_IO23
GND	111	USER_IO111	USER_IO112	112	GND
FPGA_IO24	113	USER_IO113	USER_IO114	114	FPGA_IO25
FPGA_IO26	115	USER_IO115	USER_IO116	116	FPGA_IO27
FPGA_IO28	117	USER_IO117	USER_IO118	118	FPGA_IO29
FPGA_IO30	119	USER_IO119	USER_IO120	120	FPGA_IO31
VCC_5V	121	USER_IO121	USER_IO122	122	VCC_5V
FPGA_IO32	123	USER_IO123	USER_IO124	124	FPGA_IO33
FPGA_IO34	125	USER_IO125	USER_IO126	126	FPGA_IO35
FPGA_IO36	127	USER_IO127	USER_IO128	128	FPGA_IO37
FPGA_IO38	129	USER_IO129	USER_IO130	130	FPGA_IO39
VCC_2V5	131	USER_IO131	USER_IO132	132	VCC_2V5
FPGA_IO40	133	USER_IO133	USER_IO134	134	FPGA_IO41
FPGA_IO42	135	USER_IO135	USER_IO136	136	FPGA_IO43
FPGA_IO44	137	USER_IO137	USER_IO138	138	FPGA_IO45
FPGA_IO46	139	USER_IO139	USER_IO140	140	FPGA_IO47
GND	141	USER_IO141	USER_IO142	142	GND
FPGA_IO48	143	USER_IO143	USER_IO144	144	FPGA_IO49
FPGA_IO50	145	USER_IO145	USER_IO146	146	FPGA_IO51
FPGA_IO52	147	USER_IO147	USER_IO148	148	FPGA_IO53
VCC_5V	149	USER_IO149	USER_IO150	150	VCC_5V
FPGA_IO54	151	USER_IO151	USER_IO152	152	FPGA_IO55
FPGA_IO56	153	USER_IO153	USER_IO154	154	FPGA_IO57
FPGA_IO58	155	USER_IO155	USER_IO156	156	NINT
GND	157	USER_IO157	USER_IO158	158	NINT
	159	USER_IO159	USER_IO160	160	GND

177983-8 SMT
Mezzanine receptacle
2100-00043

ZARLINK Semiconductor - Global Design Support

Title: MT90502 Mezzanine Board — Right Connector

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C	1000-002			01

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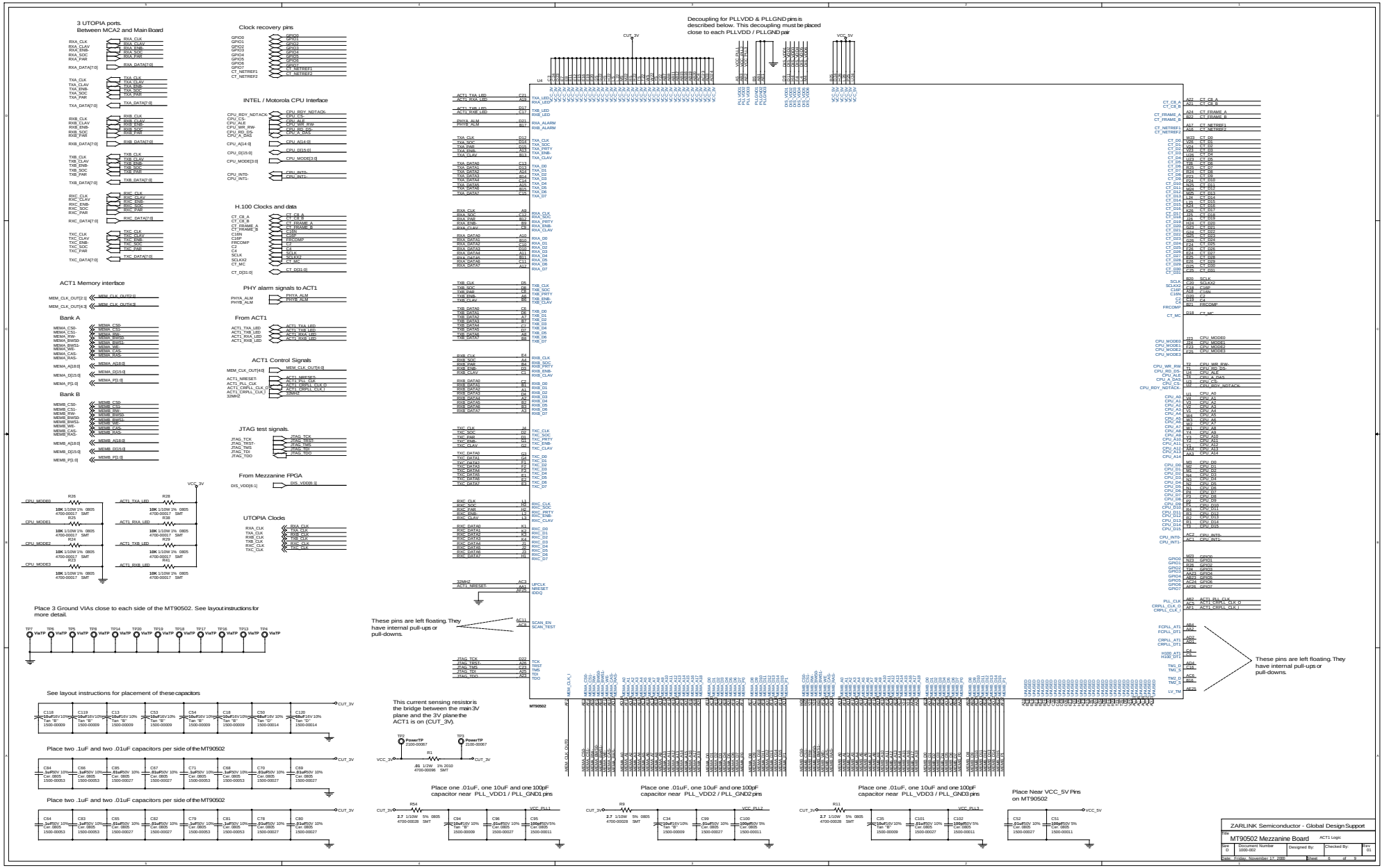
3 UTOPIA ports.
Between MCA2 and Main Board
Clock recovery pins
INTEL / Motorola CPU Interface
H.100 Clocks and data
ACT1 Memory interface
PHY alarm signals to ACT1
Bank A
Bank B
From ACT1
ACT1 Control Signals
JTAG test signals.
From Mezzanine FPGA
UTOPIA Clocks
Decoupling for PLLVDD & PLLGND pins is described below. This decoupling must be placed close to each PLLVDD / PLLGND pair
These pins are left floating. They have internal pull-ups or pull-downs.
Place 3 Ground VIAs close to each side of the MT90502. See layout instructions for more detail.
See layout instructions for placement of these capacitors
Place two .1uF and two .01uF capacitors per side of the MT90502
Place two .1uF and two .01uF capacitors per side of the MT90502
This current sensing resistor is the bridge between the main 3V plane and the 3V plane the ACT1 is on (CUT_3V).
Place one .01uF, one 10uF and one 100pF capacitor near PLL_VDD1 / PLL_GND1 pins
Place one .01uF, one 10uF and one 100pF capacitor near PLL_VDD2 / PLL_GND2 pins
Place one .01uF, one 10uF and one 100pF capacitor near PLL_VDD3 / PLL_GND3 pins
Place Near VCC_5V Pins on MT90502
These pins are left floating. They have internal pull-ups or pull-downs.
ZARLINK Semiconductor - Global Design Support
MT90502 Mezzanine Board
ACT1 Logic
Size: D
Document Number: 1009-002
Designed By:
Checked By:
Rev: 01
Date: Friday, November 17, 2000
Sheet 6 of 9

ACT1 Memory interface

Bank A

MEMA_CS0-
MEMA_CS1-
MEMA_RW-
MEMA_BWS0-
MEMA_BWS1-
MEMA_WE-
MEMA_CAS-
MEMA_RAS-
MEMA_A[18:0]
MEMA_D[15:0]
MEMA_P[1:0]
ACT1_MEM_OE-

From Mezzanine FPGA

ACT1_MEM_OE-

Clocks for memory interface

MEM_CLK_OUT[2:1]

This second SSRAM Part is optional

U9 / U13

CY7C1352-80AC 3.3V
100TQFP 256Kx18
3130-00111

This second SDRAM part is only used for parity on test boards. It is not needed by the MT90502.

U6 / U12

uPD4564163
54-TSOP II 4M x 16
3130-00194 3V

Place 1 Ground VIA test point close to each side of each memory.
When two memories are facing each other, only use 1 test point.
See layout instructions for more detail.

TP23 ViaTP TP22 ViaTP TP24 ViaTP TP26 ViaTP TP25 ViaTP TP21 ViaTP

Place one .1uF and one .01uF capacitor per side of each SDRAM.

C38 .1uF 50V 10% Cer. 0805 1500-00053
C111 .1uF 50V 10% Cer. 0805 1500-00053
C28 .1uF 50V 10% Cer. 0805 1500-00053
C131 .1uF 50V 10% Cer. 0805 1500-00053
C121 .01uF 50V 10% Cer. 0805 1500-00027
C134 .01uF 50V 10% Cer. 0805 1500-00027
C135 .01uF 50V 10% Cer. 0805 1500-00027
C136 .01uF 50V 10% Cer. 0805 1500-00027

VCC_3V

Place one .1uF and one .01uF capacitor per side of each SSRAM.

C122 .1uF 50V 10% Cer. 0805 1500-00053
C106 .1uF 50V 10% Cer. 0805 1500-00053
C36 .1uF 50V 10% Cer. 0805 1500-00053
C44 .1uF 50V 10% Cer. 0805 1500-00053
C45 .01uF 50V 10% Cer. 0805 1500-00027
C46 .01uF 50V 10% Cer. 0805 1500-00027
C37 .01uF 50V 10% Cer. 0805 1500-00027
C27 .01uF 50V 10% Cer. 0805 1500-00027

VCC_3V

ZARLINK Semiconductor - Global Design Support

Title: MT90502 Mezzanine Board — Memory Bank A

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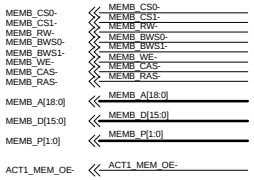
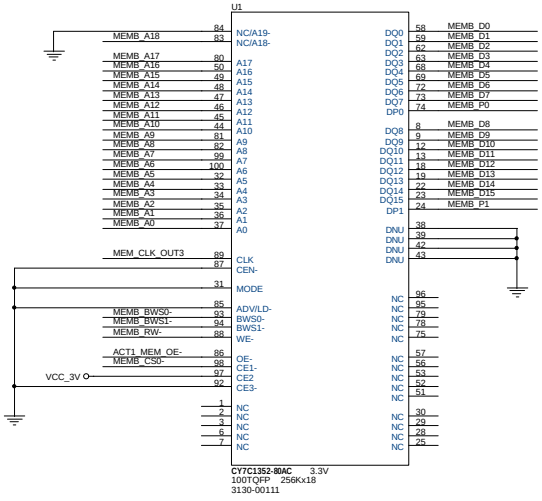
ACT1 Memory interface

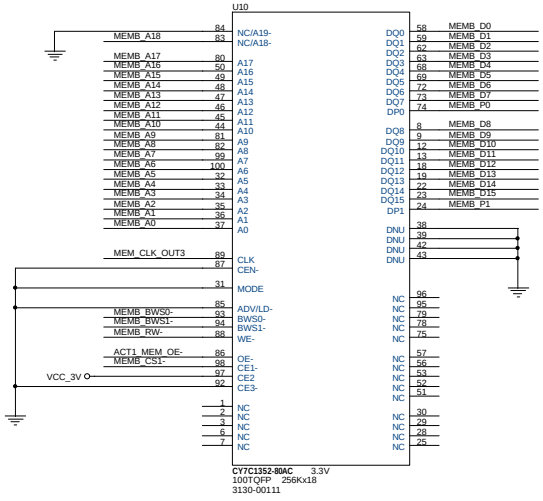
Bank B



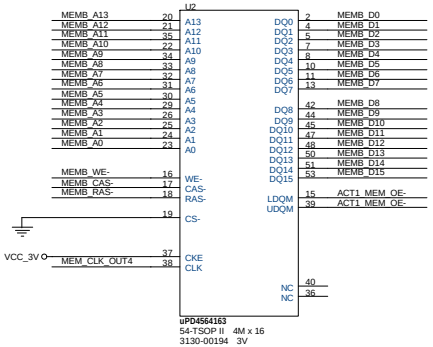
Clocks for memory interface

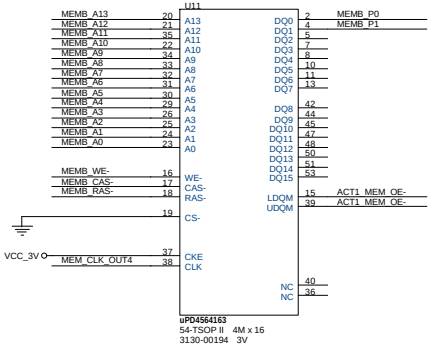


This second SSRAM Part is optional

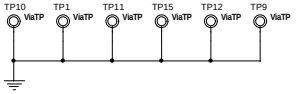


This second SDRAM part is only used for parity on test boards. It is not needed by the MT90502.

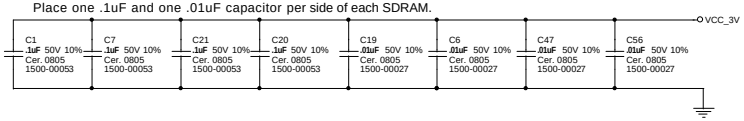




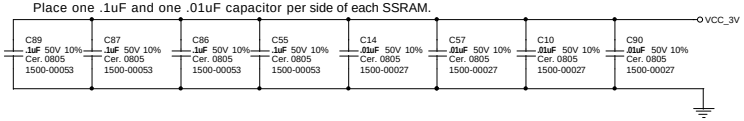
Place 1 Ground VIA test point close to each side of each memory.
When two memories are facing each other, only use 1 test point.
See layout instructions for more detail.



Place one .1uF and one .01uF capacitor per side of each SDRAM.



Place one .1uF and one .01uF capacitor per side of each SSRAM.



ZARLINK Semiconductor - Global Design Support

Title: MT90502 Mezzanine Board — Memory Bank B				
Size: C	Document Number: 1000-002	Designed By:	Checked By:	Rev: 01
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General Purpose IOs

FPGA_IO[58:0] — FPGA_IO[58:0]

ACT1 Control signals

ACT1_NRESET- — ACT1_NRESET-
ACT1_PLL_CLK — ACT1_PLL_CLK
ACT1_CRPLL_CLK_O — ACT1_CRPLL_CLK_O
ACT1_CRPLL_CLK_I — ACT1_CRPLL_CLK_I

INTEL / Motorola CPU Interface

CPU_RDY_NDTACK- — CPU_RDY_NDTACK-
CPU_CS- — CPU_CS-
CPU_ALE — CPU_ALE
CPU_WR_RW- — CPU_WR_RW-
CPU_RD_DS- — CPU_RD_DS-
CPU_A_DAS — CPU_A_DAS
CPU_A[14:0] — CPU_A[14:0]
CPU_D[15:0] — CPU_D[15:0]
CPU_MODE[3:0] — CPU_MODE[3:0]
CPU_INT0- — CPU_INT0-
CPU_INT1- — CPU_INT1-

Mezzanine FPGA configuration signals

CF_DONE — CF_DONE
CF_STAT- — CF_STAT-
CF_CONF- — CF_CONF-
CF_DATA0 — CF_DATA0
CF_DCLK — CF_DCLK

Mezzanine FPGA clocks and reset

32MHZ — 32MHZ
MF_NRESET — MF_NRESET

PHY Clocks

RCLKA — RCLKA
RCLKB — RCLKB

To PCI FPGA

NINT — NINT

Ethernet

TX_ER — TX_ER
TX_EN — TX_EN
RX_DV — RX_DV
RX_ER — RX_ER
TX_CLK — TX_CLK
RX_CLK — RX_CLK
TXD[3:0] — TXD[3:0]
RXD[3:0] — RXD[3:0]

Clock recovery pins

GPIO0 — GPIO0
GPIO1 — GPIO1
GPIO2 — GPIO2
GPIO3 — GPIO3
GPIO4 — GPIO4
GPIO5 — GPIO5
GPIO6 — GPIO6
GPIO7 — GPIO7
CT_NETREF1 — CT_NETREF1
CT_NETREF2 — CT_NETREF2

To memory interface

ACT1_MEM_OE- — ACT1_MEM_OE-

PHY alarm signals to ACT1.

PHYA_ALM — PHYA_ALM
PHYB_ALM — PHYB_ALM

TO MT9044 / MT9042 PLL

MTPLL_PRI — MTPLL_PRI
MTPLL_SEC — MTPLL_SEC
MTPLL_FS1 — MTPLL_FS1
MTPLL_FS2 — MTPLL_FS2
MTPLL_MS1 — MTPLL_MS1
MTPLL_MS2 — MTPLL_MS2
MTPLL_LOS1 — MTPLL_LOS1
MTPLL_LOS2 — MTPLL_LOS2
MTPLL_TCLR- — MTPLL_TCLR-
MTPLL_RST- — MTPLL_RST-
MTPLL_RSEL — MTPLL_RSEL
MT9044_16O- — MT9044_16O-
MT9042_16O- — MT9042_16O-
MT9044_HOLDOVER — MT9044_HOLDOVER

From ACT1

ACT1_TXA_LED — ACT1_TXA_LED
ACT1_TXB_LED — ACT1_TXB_LED
ACT1_RXA_LED — ACT1_RXA_LED
ACT1_RXB_LED — ACT1_RXB_LED

To ACT1

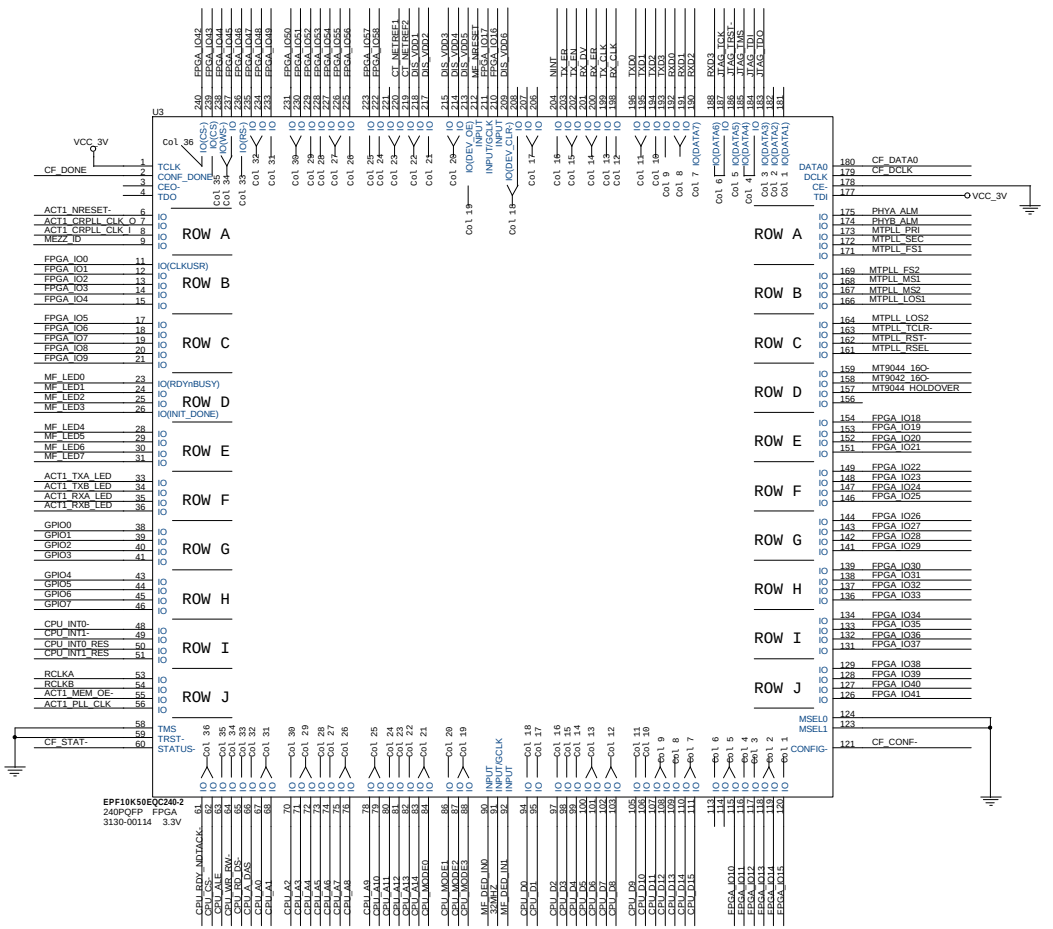
DIS_VDD[6:1] — DIS_VDD[6:1]

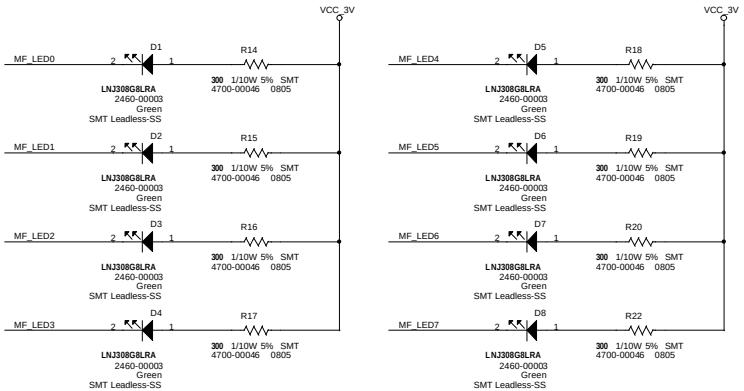
To Mezzanine FPGA

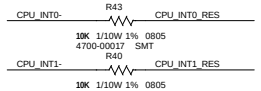
MF_DED_IN[1:0] — MF_DED_IN[1:0]
MEZZ_ID — MEZZ_ID

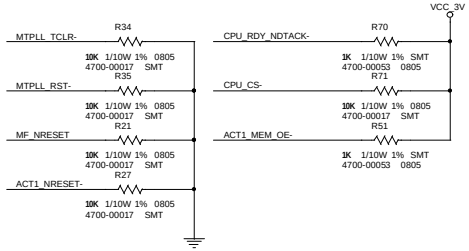
JTAG test signals.

JTAG_TCK — JTAG_TCK
JTAG_TRST- — JTAG_TRST-
JTAG_TMS — JTAG_TMS
JTAG_TDI — JTAG_TDI
JTAG_TDO — JTAG_TDO

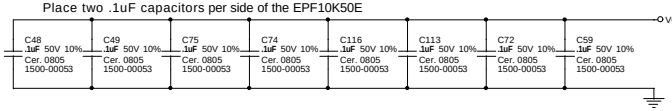




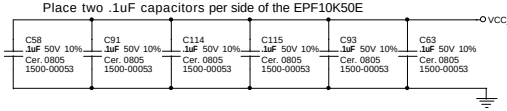




Place two .1uF capacitors per side of the EPF10K50E



Place two .1uF capacitors per side of the EPF10K50E



ZARLINK Semiconductor - Global Design Support

Title: MT90502 Mezzanine Board			Mezzanine FPGA	
Size: C	Document Number: 1000-002	Designed By:	Checked By:	Rev: 01
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