ZL38004

Dedicated Voice Processor with Dual Channel Codec

Data Sheet

August 2011

A full Design Manual is available to qualified customers. To register, please send an email to VoiceProcessing@Zarlink.com.

Features

- 100 MHz (200 MIPs) Zarlink voice processor with Butterfly hardware accelerator and breakpoint/interrupt controller
- On-board Data (26 Kbytes), Instruction (24 Kbytes RAM and Boot (3 Kbytes) ROM
- Dual ΔΣ ADCs with input buffer gain selection programmable to either 8 or 16 kHz sampling
- Dual ΔΣ DACs with output sampling of 8, 16, 44.1 and 48 kHz and internal output driver
- 2048 tap Filter co-processor shared across up to 16 separate functions in 128 tap increments
- Dual function Inter-IC Sound (I^2S) or Secondary TDM port
- Primary PCM port supports TDM (ST BUS, GCI or McBSP framing) or SSI modes at bit rates of 128, 256, 512, 1024, 2048, 4096, 8192 or 16384 Kb/sec
- Separate slave (microcontroller) and master (Flash) SPI ports, maximum clock rate = 25 MHz

Ordering Information

ZL38004QCG1	100 Pin LQFP*	Trays, Bake & Drypack
ZL38004GGG2	96 Pin VFBGA*	Trays, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

- Watchdog and 2 auxiliary timers
- 11 General Purpose Input/Output (GPIO) pins
- General purpose UART port
- Bootloadable for future Zarlink software upgrades
- External oscillator or crystal/ceramic resonator
- 1.2 V Core; 3.3 V IO with 5 V-tolerant inputs
- IEEE-1149.1 compatible JTAG port

Applications

- Hands-free car kits
- Full duplex speaker-phone for digital telephone
- Echo cancellation for video conferences

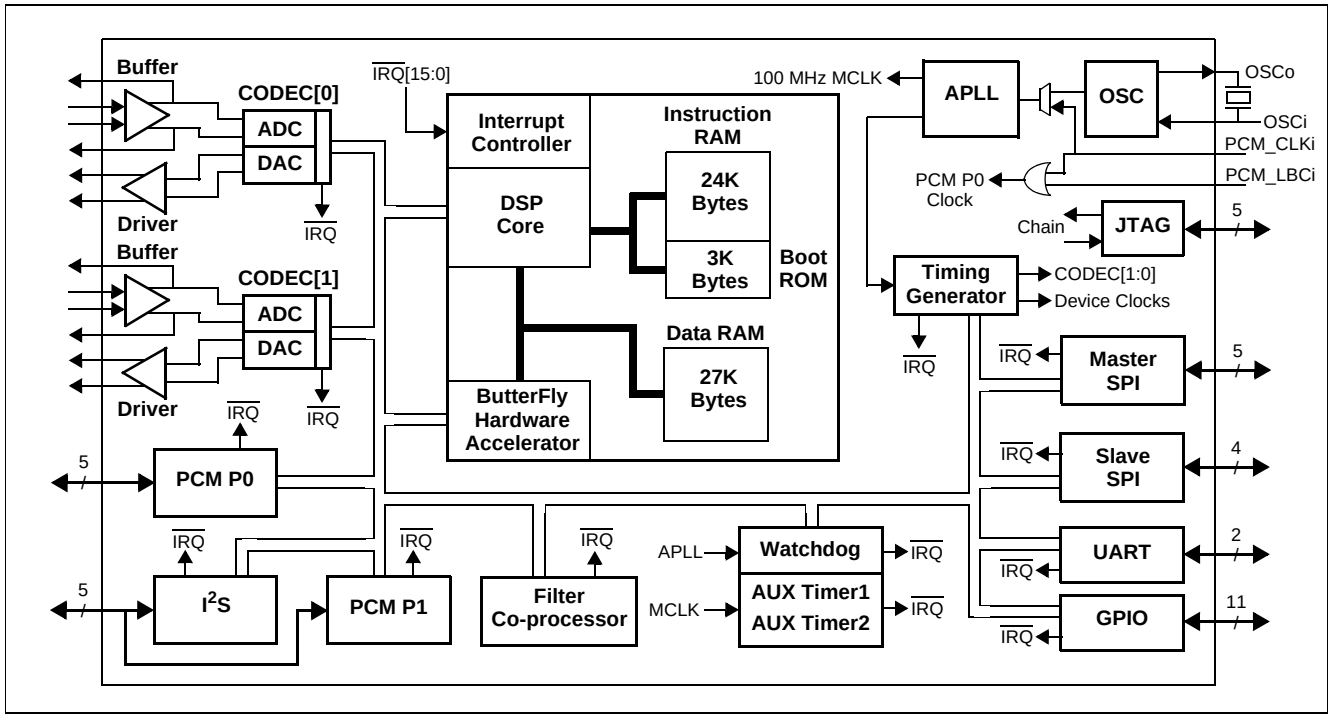


Figure 1 - Functional Block Diagram

- Intercom Systems
- Security Systems

Change Summary

Changes from March 2006 issue to August 2011 issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information	Added VFBGA package.
7	Package Drawing	Updated 96L VFBGA package drawing.

1.0 Functional Description

The ZL38004 is a hardware platform designed to support advanced acoustic echo canceller (with noise reduction) firmware applications available from Zarlink Semiconductor. These applications are resident in external memory and are down-loaded by the ZL38004 resident boot code during initialization.

The firmware products and manuals available at the release of this data sheet are: ZLS38500: Acoustic Echo Canceller with Noise Reduction for Hands-Free Car Kits; ZLS38501 Speakerphone. If these applications do not meet your requirements, please contract your local Zarlink Sales Office for the latest firmware releases.

The ZL38004 Advanced Acoustic Echo Canceller with Noise Reduction platform integrates Zarlink's Voice Processor (ZVP) DSP Core with a number of internal peripherals. These peripherals include the following:

- Two independent ΔΣ CODECs
- Two PCM ports - ST BUS, GCI, McBSP or SSI operation
- An I^2S interface port
- A 2048 tap Filter Co-processor
- Two Auxiliary Timers and a Watchdog Timer
- 11 GPIO pins
- A UART interface
- A Slave SPI port and a Master SPI port
- A timing block that supports master and slave operation
- An IEEE - 1149.1 compatible JTAG port

The DSP Core can process up to four 8-bit audio channels, two 16-bit audio channels or two 8-bit and one 16-bit audio channel. These audio channels may originate and terminate with the ΣΔ CODECs, or be communicated to and from the DSP Core through the PCM ports or the I^2S port.

2.0 Core DSP Functional Block

The ZL38004 DSP Core functional block, illustrated in Figure 1, is made up of a DSP Core, Interrupt Controller, Data RAM, Instruction RAM, BOOT ROM and a ButterFly Hardware Accelerator. This block controls the timing (APLL and Timing Generator), peripheral interfaces and Filter Co-processor through a peripheral address/data/control bus and 16 prioritized interrupts.

The ZL38004 implementation of DSP core and Filter Co-processor have been optimized to efficiently support voice processing applications. These applications are described in detail in the firmware manuals associated with this hardware platform.

When an interrupt occurs the DSP core saves its current status and jumps to the address of the associated interrupt service routine.

3.0 Codec[1:0]

The ZL38004 has two 16-bit fully differential ΔΣ CODECs (CODEC 0/1) that can be programmed for 48 kHz or 44.1 kHz sampling, or to meet G.712 requirements at 8 kHz sampling or G.722 at 16 kHz sampling, see Figure 2. The ADC path consists of input signal pins C0/1_ADCi+ and C0/1_ADCi- (buffer output pins C0/1_BF0+ and C0/1_BFo-), which feed selectable Microphone Amplifier or Line Amplifier options. Once past the buffer the analog signal goes through a low pass antialiasing filter and to a 4^{th} order feed-forward ΔΣ Modulator that produces a Pulse Density Modulated (PDM) signal. Next the PDM signal goes through a Low Pass Decimation Filter and then is converted into a 16-bit parallel word that can be read by the ZL38004 DSP (ADCout[15:0], Figures 2).

The ZL38004 DSP will send 16-bit parallel word samples (DACin[15:0], Figure 2) to the DAC where they are converted to serial data and passed through an interpolation filter followed by a digital ΔΣ Modulator. The ΔΣ Modulator generates PDM data, which then passes through a 32-tap FIR reconstruction filter. The reconstructed analog signal is then passed to a unity voltage gain differential output driver and to pins C0/1_DACo+ and C0/1_DACo-.

The CODEC bias voltages are generated by an internal bandgap circuit (BIAS_VCM, BIAS_RF+ and BIAS_RF-).

Each ZL38004 CODEC has two loopbacks. When activated, the input analog signal on pins C0/1_ADC+/- is looped around to C0/1_DAC+/-. Pulse Density Modulated (PDM) serial data from the ADC Analog ΔΣ Modulator output is looped around to the input of the DAC Reconstruction Filter. At the same time 16-bit parallel data is looped around from DACin[15:0] to ADCout[15:0]. PDM serial data from the DAC Digital ΔΣ Modulator is looped around to the input of the ADC Digital Low Pass Decimation Filter.

When the Parallel Loopback is activated the input analog signal on pins C0/1_ADC+/- is looped around to the C0/1_DAC+/- output. 16-bit parallel data from the ADC Digital Low Pass Decimation Filter is looped around to the DAC Digital Low Pass Interpolation Filter. This data may be read by the DSP, but parallel data written to the DAC by the DSP will be lost.

CODEC0 and CODCE1 of the ZL38004 may be powered down if they are not required. See firmware manual.

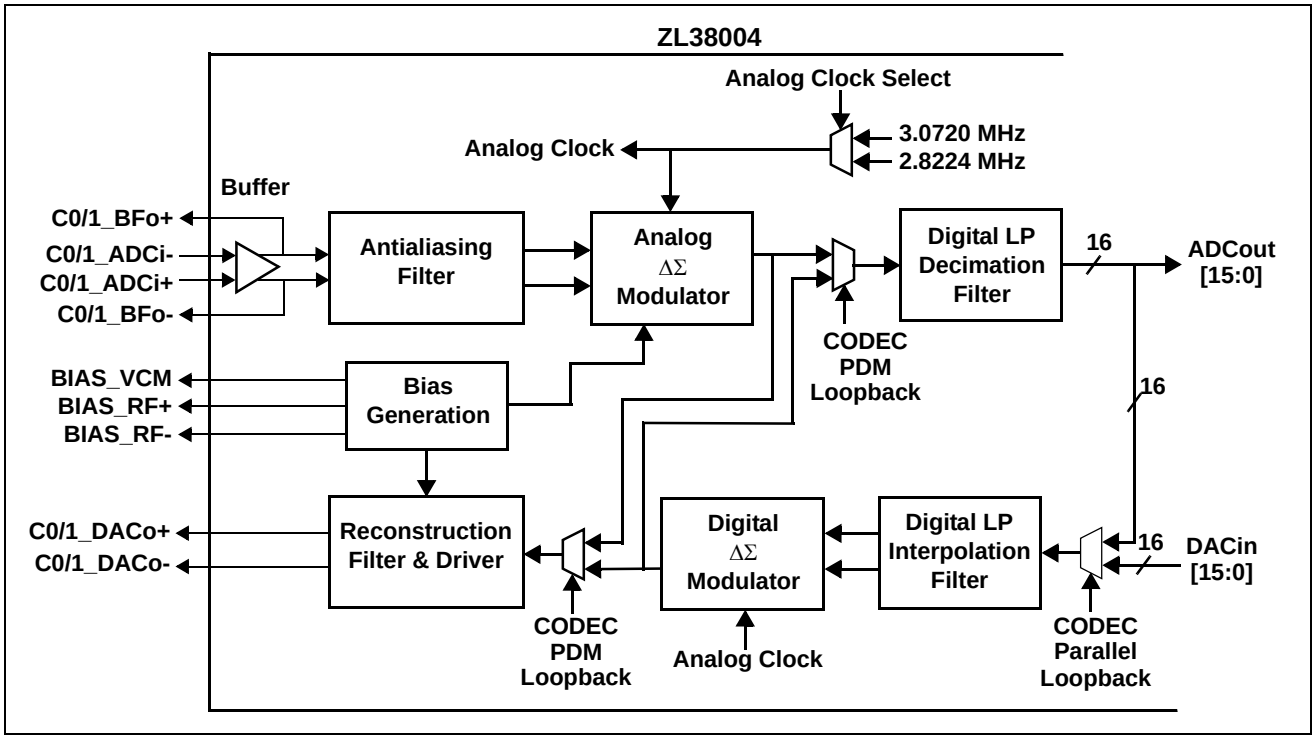


Figure 2 - CODEC Block Diagram

4.0 PCM / I²S Ports

The PCM ports 0 and 1 support data communication between an external peripheral device and the ZL38004 DSP Core using separate input (P0/1PCMi) and output (P0/1PCMo) serial streams with TDM (i.e., ST-BUS, GCI or McBSP) or SSI interface timing in both master or slave timing modes. Both PCM Ports 0 and 1 support the same functionality and modes of operation.

PCM Port 1 pin functions are shared with the I^2S Port pin functions. The I^2S (Inter-IC Sound) port and PCM Port One share the same physical pins of the ZL38004. Selection of either I^2S port operation or PCM Port One operation is done through the Port One PCM/I^2S Select Register. See firmware manual.

The I^2S port can be used to connect external Analog-to-Digital Converters or CODECs to the internal DSP. This port can operate in master mode, where the ZL38004 is the source of the port clocks, or slave mode, where the bit and sampling clocks (I^2S_SCK and I^2S_ LRCK) are inputs to the ZL38004. In I^2S port master mode the clock signal at output pin I^2S_LRCK is the sampling frequency (f_S), the clock signal at output I^2S_SCK is 32 x f_S, and the clock signal at output I^2S_MCLK is 256 x f_S. In I^2S port slave mode the relationship between the clock signal at input pin I^2S_LRCK and the clock signal at input I^2S_SCK must be 32 x f_S. In slave mode the 256 x f_S relationship between f_S and the I^2S_MCLK is not mandatory, and the I^2S_MCLK output pin will be in a high impedance state.

Access to the control and status registers associated with these ports is through the Slave SPI port or UART.

5.0 Host Microprocessor and Peripheral Interfaces

The ZL38004 provides 1 master SPI port (with 2 chip selects), 1 slave SPI ports and an UART. The master SPI port's primary function is to access and external FLASH memory to download firmware to the ZL38004.

The control/status registers and memory of the ZL38004 can be accessed (R/W) by an external host through the Slave SPI and the UART ports. Register/Memory read and write accesses are carried out through a series of port read and write accesses as follows:

5.1 Master SPI (FLASH Port)

The Master SPI port is used by the ZL38004 to access one or two peripheral devices (chip select signals SPIM_CS[1:0]). It supports both SPI and MICROWIRE modes of operation and can write up to 40 bits or read up to 32 bits in a single access. The Chip Select output signals may be programmed for a single access or burst access. All communication is MSB first and all pins of the master SPI port are outputs controlled by the ZL38004, except SPIM_MISO.

5.2 Slave SPI (Host Port)

The slave SPI port may be used by an external host microprocessor to access (Read/Write) the ZL38004 internal control/status registers and memory. Access is initiated when the external host makes signal SPIS_CS low and is ended when this signal goes high. The host will then apply a clock (maximum 25 MHz) to signal SPIS_CLK to clock data out of SPIS_MISO and in on SPIS_MOSI.

5.3 UART

The UART (Universal Asynchronous Receiver Transmitter) port may be used by an external host microprocessor to access (Read/Write) the ZL38004 internal control/status registers and memory. The ZL38004 DSP will set up the initial parameters of this port (i.e., master/slave, baud rate, stop bits, parity bit...) during the Boot process. After the device has been booted these port options can be changed as per the firmware manual.

The UART port will support 8-bit data only with any combination of 1 start bit, 0 or 1 parity bit(s) and 1, 1.5 or 2 stop bit(s).

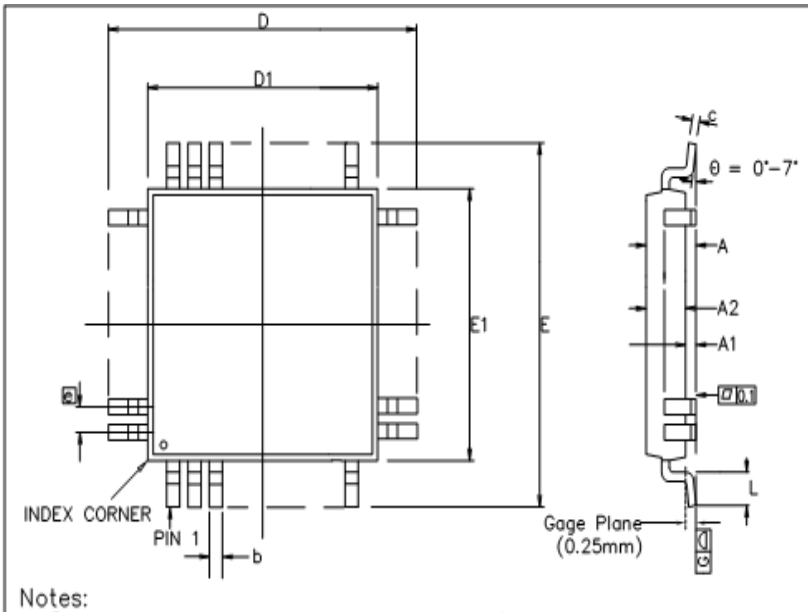
The ZL38004 has 11 GPIO (General Purpose Input/Output) pins that can be individually configured as either input or output. These pins are intended for low frequency signalling.

When a GPIO pin is defined as an input the state of that input pin is sampled with the internal master clock (Mclk = 100 MHz) and latched into the GPIO Read Register. This sampling can be stopped (Freeze) on an individual GPIO pin. Individual pins of GPIO[4:0] may have an internal pull-down resistor activated/deactivated and individual pins of GPIO[10:5] may have an internal pull-up activated/deactivated.

Immediately after a power-on reset ($\overline{\text{RST}}$ pin) the GPIO pins are defined as inputs and their state is captured in the GPIO Start-Up Status Register. The state of this register is used by the Boot program to determine the base functionality and programming options of the device.

Individual GPIO pins may also be defined as outputs with associated enable/disable (active/high impedance) control.

Mechanical Drawings



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.60		---	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	16.00 BSC			0.630 BSC	
D1	14.00 BSC			0.551 BSC	
E	16.00 BSC			0.630 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	100				
ND	25				
NE	25				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BED Iss. C

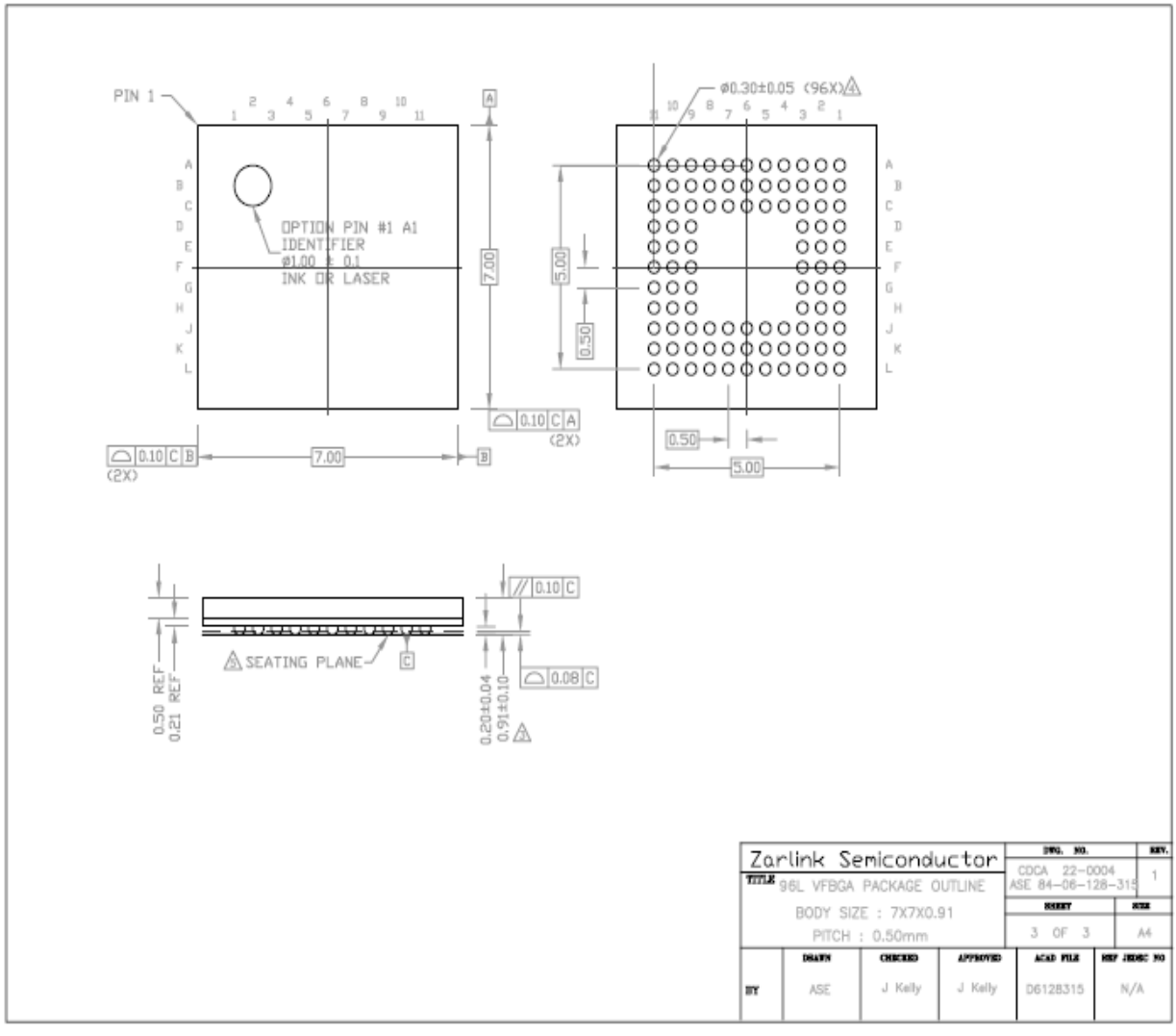
Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/023 (Swindon)

ISSUE	1	2	3	
ACN	201373	207144	212447	
DATE	29Oct96	15Jul99	26Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

	Package Code QC
Previous package codes GP / B	Package Outline for 100 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint
	GPD00253


PIN 1
OPTION PIN #1 A1 IDENTIFIER
ø1.00 ± 0.1
INK OR LASER
ø0.30±0.05 (96X)
7.00
5.00
0.50
0.10 C A (2X)
0.10 C B (2X)
SEATING PLANE
0.50 REF
0.21 REF
0.20±0.04
0.91±0.10
0.08 C
Zarlink Semiconductor
96L VFBGA PACKAGE OUTLINE
BODY SIZE : 7X7X0.91
PITCH : 0.50mm
CDCA 22-0004
ASE 84-06-128-315
3 OF 3
A4
ASE
J Kelly
J Kelly
D6128315
N/A

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