ZL30107

GbE Line Card Synchronizer

Data Sheet

September 2007

Features

- Single chip low cost solution for synchronizing an Ethernet PHY to a standard telecom clock
- Generates an IEEE 802.3 jitter compliant 25 MHz Gigabit Ethernet output clock
- Supports three modes of operation: Asynchronous Freerun, Synchronous, and Asynchronous Holdover
- Defaults in Asynchronous Freerun mode
- In Asynchronous Freerun mode, the DPLL generates an output clock with a frequency accuracy equal to frequency accuracy of the external crystal oscillator (XO) or a low cost crystal (XTAL)
- In Synchronous mode, the DPLL automatically synchronizes to one of a pre-defined set of frequencies including 2 kHz, 8 kHz, 64 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz, 38.88 MHz, 77.76 MHz.
- Configurable to accept a 25 MHz input reference
- Automatic entry into Asynchronous Holdover mode when all input references fail

Ordering Information

ZL30107GGG	64 Pin CABGA	Trays
ZL30107GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Input reference is manually selectable through the serial (SPI) interface
- Hitless input reference switching
- Lock indicator pin
- Input reference status monitors
- Programmable loop bandwidth of 14 Hz, 28 Hz, or 890 Hz

Applications

- Ethernet Line Cards Supporting Synchronous Transmission

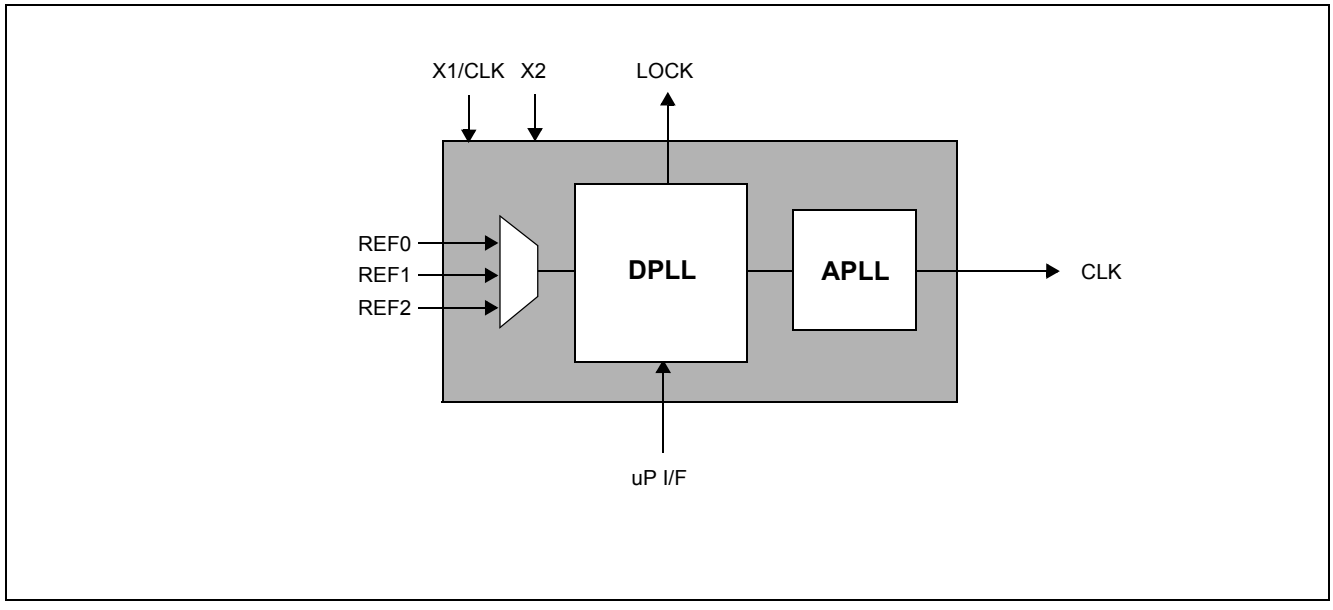


Figure 1 - Block Diagram

1.0 Change Summary

Changes from the June 2007 Issue to September 2007. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
7	Pin Description	Changed pin description of pins G3 and H3 from "IC - Leave unconnected" to "IC - Connect to ground"
19	4.0, “Detailed Register Map“	Added a note in the register description for the reset ready bit (reg 0x01, bit 7) recommending to wait until this bit is set to 1 before reading or writing to any other registers.
19	4.0, “Detailed Register Map“	Added a note to register description for register 0x03 regarding the operation of the sticky bits

Changes from March 2007 Issue to June 2007 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
17	3.0, “Register Map Summary“	Added "Register Map Summary" section.
19	4.0, “Detailed Register Map“	Updated the "Detailed Register Map" section.

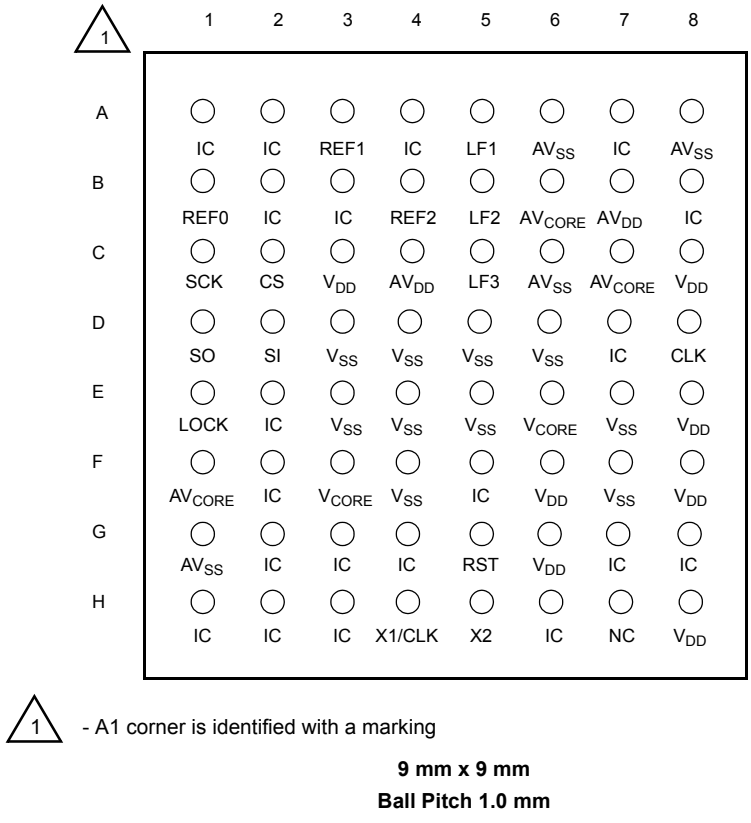


Figure 2 - Pin Connections

Table of Contents

List of Figures

List of Tables

Pin Description

Pin #	Name	I/O Type	Description
B1 A3 B4	REF0 REF1 REF2	I_d	**Reference Inputs (LVCMOS, Schmitt Trigger).** These reference inputs are used for synchronizing the PLL. These pins are internally pulled down to Vss.
D8	CLK	O	**SONET/SDH/Ethernet Clock Output (LVCMOS).** This output clock is configurable as 77.76 MHz, 25 MHz, and 50 MHz. Default is 77.76 MHz.
G5	RST	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
E1	LOCK	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for the PLL. This output goes high when the DPLL's output is frequency is phase locked to the input reference.
A5	LF1	A	**External Analog PLL Loop Filter terminal.**
B5	LF2	A	**Analog PLL External Loop Filter Reference.**
C5	LF3	A	**Analog PLL External Loop Filter Reference.**
H4	X1/CLK	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (XO, XTAL). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
H5	X2	O	**Oscillator Master Clock Output (LVCMOS).** This pin is used for connection with an crystal. This pin must be left unconnected when the X1 pin is connected to a clock oscillator.
C1	SCK	I	**Clock for Serial Interface (LVCMOS).** Serial interface clock.
D2	SI	I	**Serial Interface Input (LVCMOS).** Serial interface data input pin.
D1	SO	O	**Serial Interface Output (LVCMOS).** Serial interface data output pin.
C2	CS	I_u	**Chip Select for Serial Interface (LVCMOS).** Serial interface chip select. This pin is internally pulled up to Vdd.
F5 A1 A2 A4 A7 B8 D7 E2 G7 H1 B2 G4 G2 G8 F2	IC		**Internal Connection.** Leave unconnected.

Pin #	Name	I/O Type	Description
H6 B3 H2 G3 H3	IC		**Internal Connection.** Connect to ground.
H7	NC		**No Connection.** Leave unconnected.
C3 C8 E8 F6 F8 G6 H8	V_{DD}	P P P P P P P	**Positive Supply Voltage.** +3.3 V_{DC} nominal.
E6 F3	V_{CORE}	P P	**Positive Supply Voltage.** +1.8 V_{DC} nominal.
B7 C4	AV_{DD}	P P	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
B6 C7 F1	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
D3 D4 D5 D6 E3 E4 E5 E7 F4 F7	V_{SS}	G G G G G G G G G G	**Ground.** 0 Volts.
A6 A8 C6 G1	AV_{SS}	G G G G	**Analog Ground.** 0 Volts.

I - Input
I_d - Input, Internally pulled down
I_u - Input, Internally pulled up
O - Output
A - Analog
P - Power
G - Ground

2.0 Functional Description

The ZL30107 Low Jitter Ethernet Synchronizer is a single chip low cost solution for synchronizing an Ethernet PHY to a standard telecom clock.

2.1 Reference Inputs

The DPLL provides three reference inputs (**REF0**, **REF1**, **REF2**) for systems that have two redundant references and one loop timing reference. Reference inputs are manually selected through the SPI interface by accessing the *dpll_refsel* register (0x20).

Switching between reference inputs is hitless meaning that the DPLL will absorb the phase difference between clock inputs instead of passing a phase transient through to the output.

Each of the reference inputs accept a single-ended LVCMOS clock with a frequency ranging from 2 kHz to 77.76 MHz. Built-in frequency detection circuitry automatically determines the frequency of the reference if its frequency is within the set of pre-defined frequencies as shown in Table 1.

2 kHz
8 kHz
64 kHz
1.544 MHz
2.048 MHz
6.48 MHz
8.192 MHz
16.384 MHz
19.44 MHz
38.88 MHz
77.76 MHz

Table 1 - Set of Pre-Defined Auto-Detect Clock Frequencies

The reference inputs can also lock to 25 MHz when configured as a custom frequency. To support a 25 MHz input reference, the following register configuration is required to define a new custom frequency.

Write 0x35 to address 0x67
Write 0x0C to address 0x68
Write 0x06 to address 0x69
Write 0x12 to address 0x6A
Write 0x37 to address 0x6B
Write 0x06 to address 0x6C
Write 0x99 to address 0x6D
Write 0x06 to address 0x6E
Write 0x80 to address 0x6F
Write 0x01 to address 0x70

Note: This procedure must be performed after each reset cycle.

Figure 3 - Configuring a 25 MHz Custom Input Reference Frequency

The *ref_freq_mode register* (0x65) determines if the reference inputs to lock to one of the frequencies listed in Table 1 (auto frequency detect), or to the 25 MHz custom frequency configuration.

2.2 Loop Bandwidth

The loop bandwidth of the DPLL can be selected as 14 Hz, 28 Hz, or 890 Hz using the *dpll_bw* register (0x1D). A loop bandwidth of 890 Hz is selected by default, but if additional jitter filtering is required, a value of 28 Hz or 14 Hz can be selected. A lower bandwidth will allow less reference input jitter to propagate to the output.

2.3 Mode of Operation

The DPLL supports three modes of operation: Asynchronous Freerun, Synchronous, and Asynchronous Holdover. By default the DPLL operates in an Asynchronous Freerun mode where the frequency accuracy of the output is equal to the frequency accuracy of the external oscillator. This is a normal mode prior to entering Synchronous operation.

To enable Synchronous operation, the *dpll_modesel* register (0x1F) must be reconfigured to the Synchronous Mode. Once in Synchronous mode, the DPLL will start the lock acquisition process on the selected reference input. Once locked, the DPLL generates an output clock with an equivalent frequency accuracy to the reference input. If the input reference fails, the DPLL will automatically enter Asynchronous Holdover mode.

The Asynchronous Holdover mode can also be used to help eliminate a possible phase transient when switching from Synchronous to an Asynchronous mode. When switching to the Asynchronous Holdover mode, the DPLL keeps on generating an output clock based on historical frequency data collected while the DPLL was synchronized.

2.4 Generating a 25 MHz Output Clock

By default, the DPLL generates a 77.76 MHz output clock. To generate a 25 MHz Ethernet clock, the DPLL must be re-configured by modifying register values using the following procedure:

```
Write 0x04 to address 0x64
Write 0x7C to address 0x65
Write 0x92 to address 0x66
Write 0x00 to address 0x64
Write 0xAB to address 0x52
Write 0x07 to address 0x64

Read register VALUE from address 0x6E
if VALUE ≤ 0x0B
    NewVALUE = VALUE + 4
else
     NewVALUE = 0x0F
Write NewVALUE to address 0x6E
Write 0x00 to address 0x64
```

Note: This procedure must be performed after each reset cycle.

Figure 4 - Configuring the 25 MHz Output Clock

2.5 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL) operating at a 20 MHz frequency. Refer to application note ZLAN-68 for a list of recommended clock oscillators.

2.5.1 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **X1/CLK** pin as shown in Figure 5. The connection to X1/CLK should be direct and not AC coupled. The **X2** pin must be left unconnected.

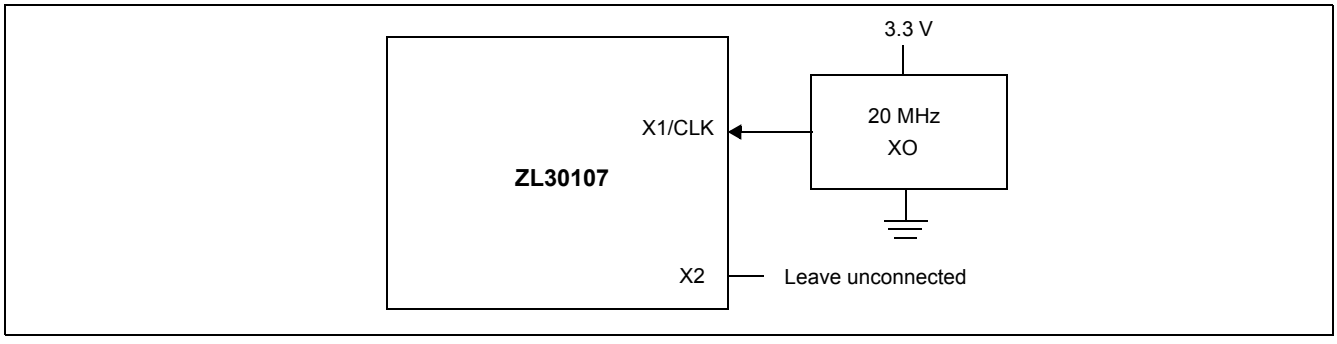


Figure 5 - Clock Oscillator Circuit

2.5.2 Crystal (XTAL)

When using a crystal as the master timing source, it should be connected as shown in Figure 6.

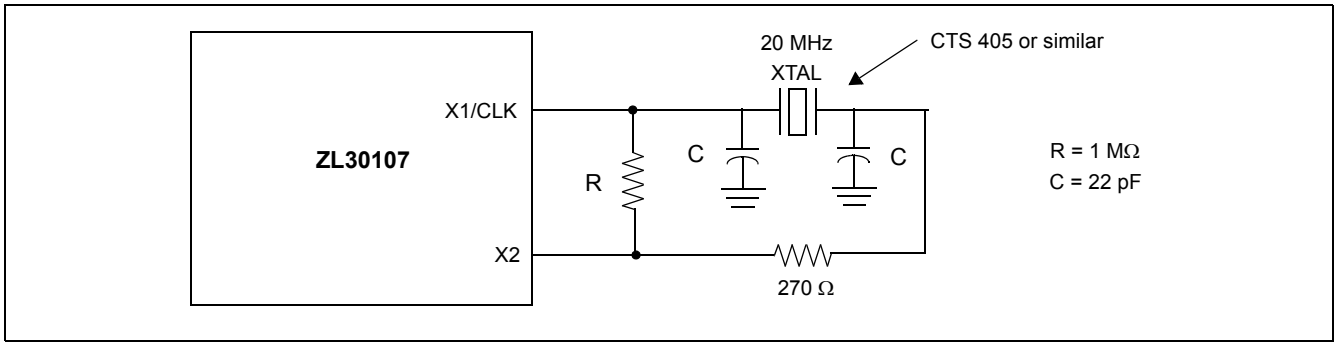


Figure 6 - Crystal Oscillator Circuit

2.6 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up. The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

2.7 Reducing Power Consumption

To optimize power consumption during Synchronous or Asynchronous modes, the following registers can be modified:

Write 0x0F to address 0x67
Write 0x8D to address 0x68

Note: This procedure must be performed after each reset cycle.

Figure 7 - Configuration for Optimizing Power Consumption

2.8 Power Supply Filtering

Jitter levels on the ZL30107 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30107 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-179.

2.9 Reset Circuit

To ensure proper operation, the device must be reset by holding the rst_b pin low for at least 300 ns after power-up. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 8. This circuit provides approximately 60 μs of reset low time. The rst_b input has schmitt trigger properties to prevent level bouncing.

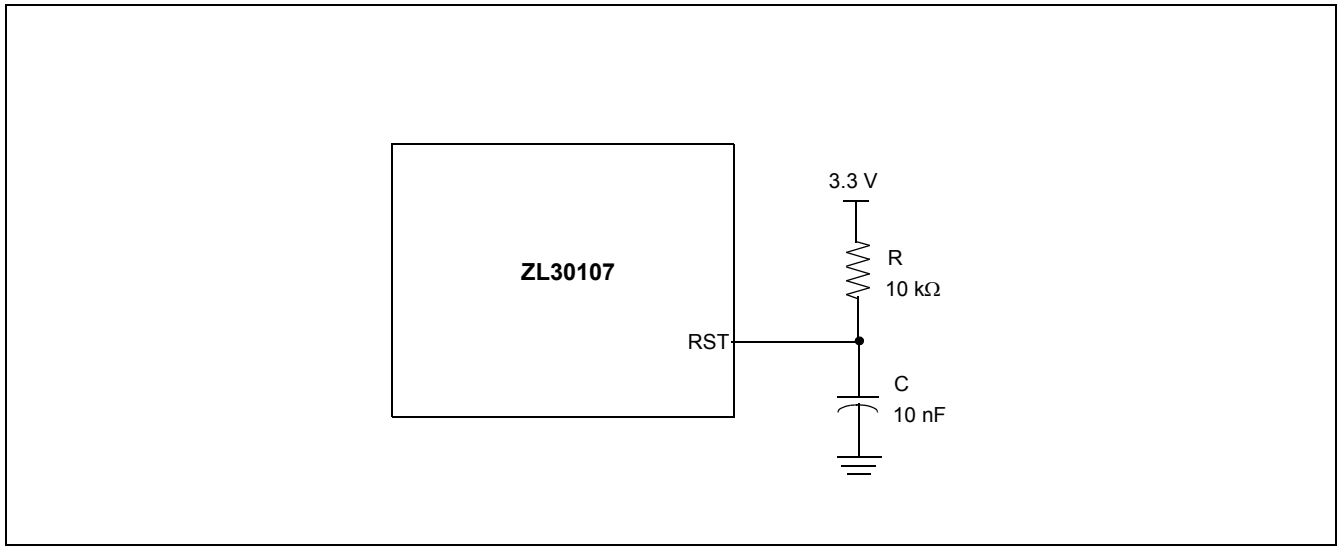


Figure 8 - Typical Power-Up Reset Circuit

2.10 Filter Components and Recommended Layout

The low jitter APLL in the ZL30107 uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

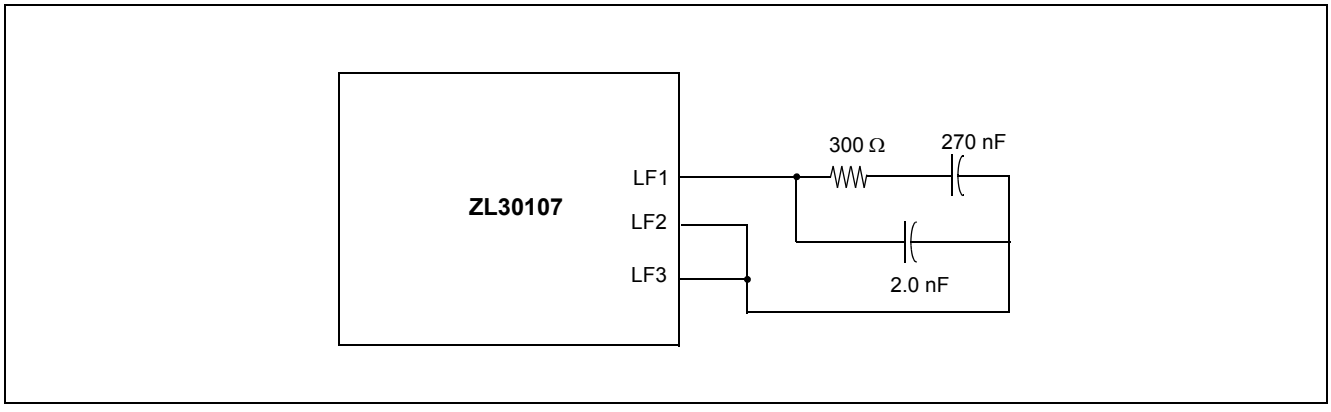


Figure 9 - Filter Component Values

The recommended PCB layout for the external filter components is shown in Figure 10.

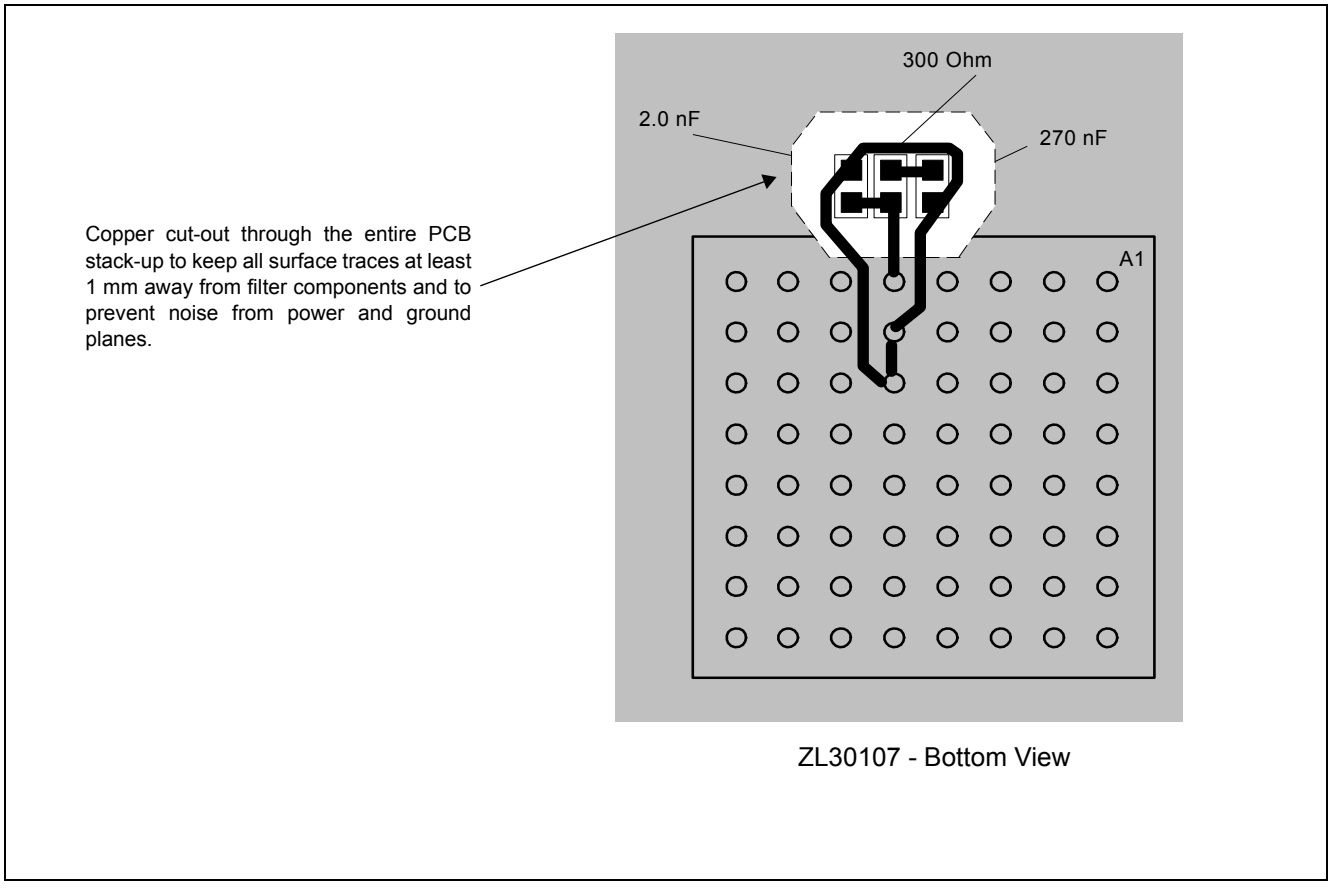


Figure 10 - Recommended Filter Layout

2.11 Serial Peripheral Interface

The serial peripheral interface allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **SCK** pin when the **CS** pin is active. If the **SCK** pin is low during **CS** activation, then MSB first timing is selected. If the **SCK** pin is high during **CS** activation, then LSB first timing is assumed.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the ZL30107, output data from the **SO** pin must be ignored. Similarly, the input data on the **SI** pin is ignored by the device during a read cycle from the ZL30107.

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 11 and Figure 12, and Figure 13 and Figure 14 describe the MSB first mode. Table 2 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 2 - Serial Peripheral Interface Timing

2.11.1 Least Significant Bit (LSB) First Transmission Mode

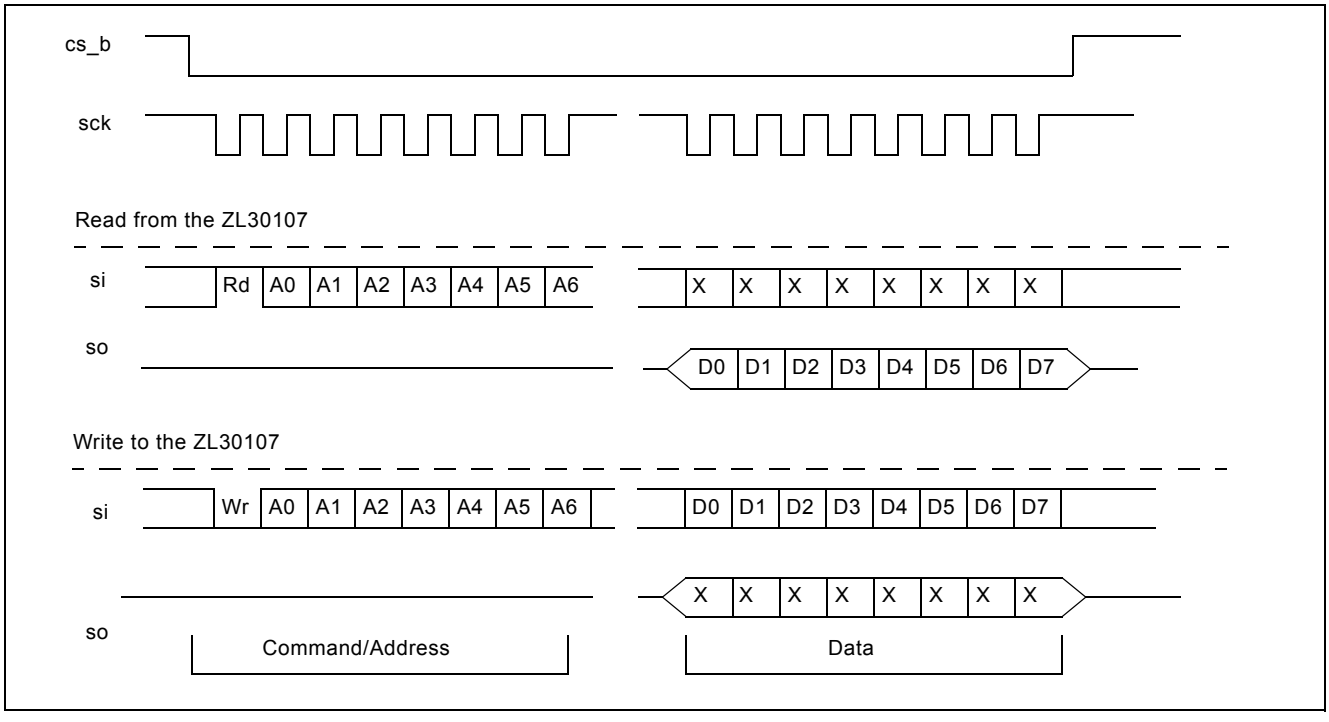


Figure 11 - Serial Peripheral Interface Functional Waveforms - LSB First Mode

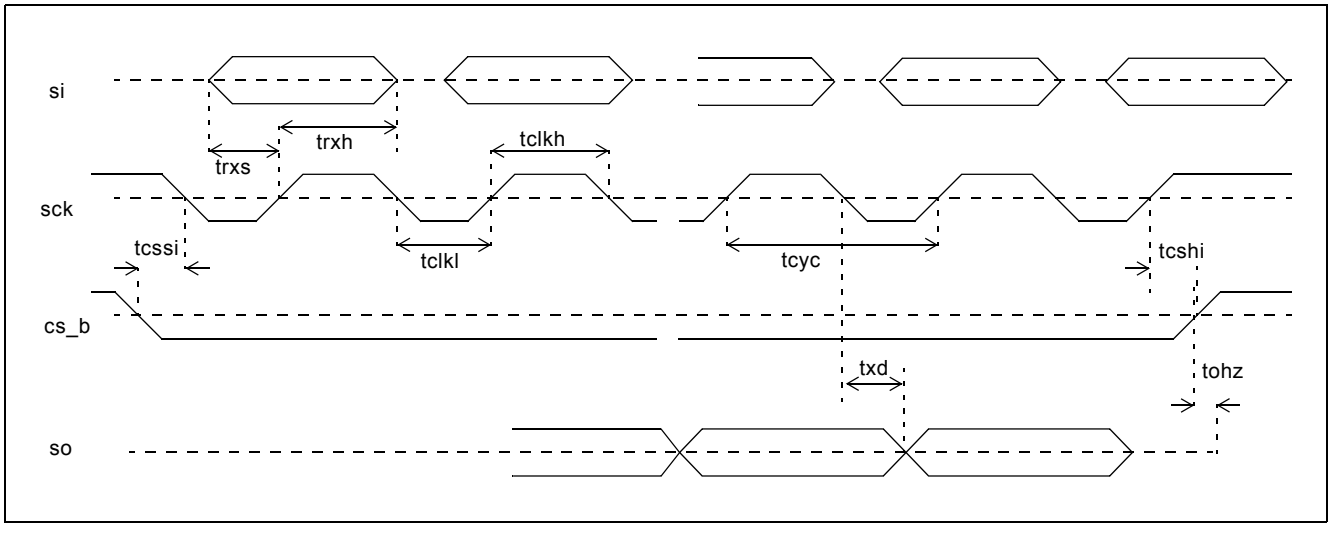


Figure 12 - Serial Peripheral Interface Timing - LSB First Mode

2.11.2 Most Significant Bit (MSB) First Transmission Mode

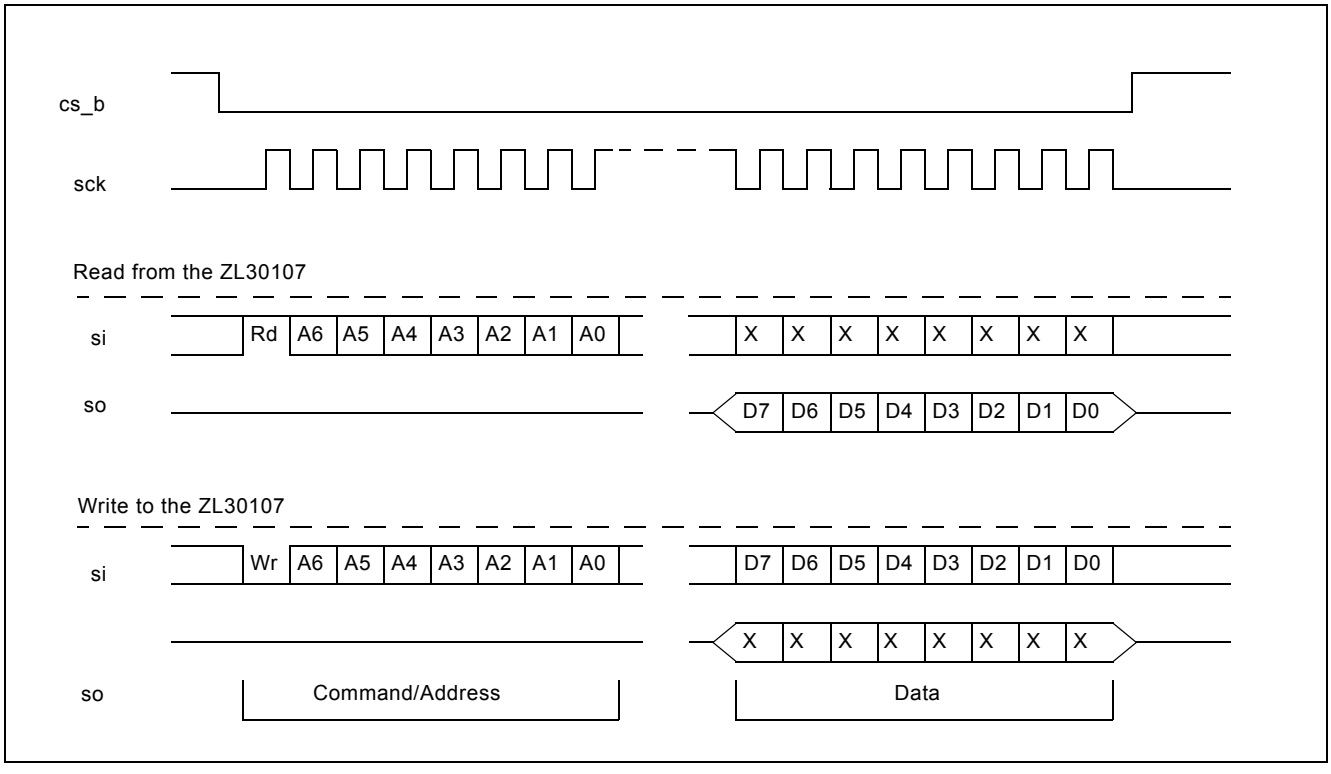


Figure 13 - Serial Peripheral Interface Functional Waveforms - MSB First Mode

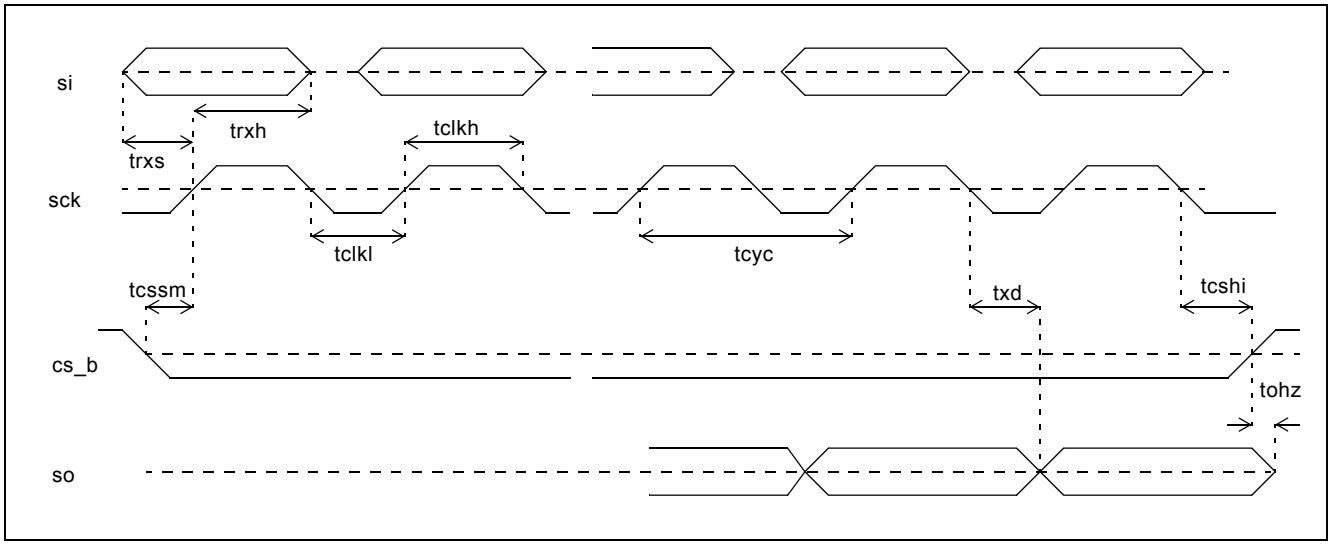


Figure 14 - Serial Peripheral Interface Timing - MSB First Mode

3.0 Register Map Summary

The following table provides a summary of the registers available for status updates and configuration of the device.

Page_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Main Registers				
0x00	id_reg	A1	Chip and version identification.	R
0x01	Reserved			
0x02	ref_fail	FF	Reference failure indicators.	R
0x03	dpll_status	70	Mode status indicator for the DPLL.	Sticky R
0x04 - 0x1C	Reserved			
0x1D	dpll_bw	A3	Control register for setting the DPLL Bandwidth.	R/W
0x1E	Reserved			
0x1F	dpll_modesel	02	Control register for setting the DPLL mode of operation (Synchronous, Free-run, Asynchronous).	R/W
0x20	dpll_refsel	00	DPLL reference selection.	R/W
0x21 - 0x51	Reserved			
0x52	clk_freq	42	Control register for the CLK frequency selection.	R/W
0x53 - 0x63	Reserved			
0x64	page_pointer	00	Use to access extended page addresses.	R/W
0x65	ref_freq_mode_0	00	Control register to set whether to use auto frequency detect or 25 MHz for ref0, ref1, ref2.	R/W
0x67	25M_in_freq_config_0	00	Control register for the [7:0] bits of the 25 MHz input frequency configuration.	R/W
0x68	25M_in_freq_config_1	00	Control register for the [15:8] bits of the 25 MHz input frequency configuration.	R/W
0x69	scm_low	00	Control register for the SCM low limiter.	R/W
0x6A	scm_high	00	Control register for the SCM high limiter.	R/W
0x6B	cfm_low_0	00	Control register [7:0] for the CFM low limit.	R/W
0x6C	cfm_low_1	00	Control register [15:8] for the CFM low limit.	R/W

Page_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x6D	cfm_hi_0	00	Control register [7:0] for the CFM high limit.	R/W
0x6E	cfm_hi_1	00	Control register [15:0] for the CFM high limiter.	R/W
0x6F	cfm_cycle	00	Control register for the CFM reference monitoring cycles - 1.	R/W
0x70	ref_div4	00	Control register to enable the use of ref_div4 for the CFM and PFM inputs.	R/W
0x6D - 0x7F	Reserved			
Extended Registers - Page 4				
04_0x65	apll_fconv7_0	E0	Controls the apll center frequency.	R/W
04_0x66	apll_fconv15_8	97		
Extended Registers - Page 7				
07_6E	vco_lim	07	Sets the internal VCO limits.	R/W

4.0 Detailed Register Map

4.1 Main Registers

Page_Address:**0x00**
Register Name: **id_reg**
Default Value: **See description**
Type: **R/W**

Bit Field	Function Name	Description
4:0	chip_id	Chip Identification.
6:5	chip_revision	Chip revision number.
7	reset_ready	Reset ready indication. When this bit is set to 1 the reset cycle has completed. **Note that it is recommended not to read or write to any other registers until this bit is set to 1.**

Address: **0x02**
Register Name: **ref_fail**
Default Value: **0xFF**
Type: **R**

Bit Field	Function Name	Description
0	ref0_fail	This bit is set to 1 when ref0 has a failure
1	ref1_fail	This bit is set to 1 when ref1 has a failure
2	ref2_fail	This bit is set to 1 when ref2 has a failure
7:3	Reserved	

Address: **0x03**
Register Name: **dpll_status**
Default Value: **0x70**
Type: **R Sticky**[1]

Bit Field	Function Name	Description
0	locked	This bit is set to high when the DPLL achieves lock. The bit is cleared automatically when this register is read.
1	lost_lock	This bit is set to high when the DPLL loses lock. The bit is cleared automatically when this register is read.
2	holdover	This bit is set to high when the DPLL enters holdover. The bit is cleared automatically when this register is read.
3	ref_changed	This bit is set to high when the DPLL makes a reference switch. The bit is cleared automatically when this register is read.
7:4	Reserved	

[1] Once a sticky bit is set, it will remain set until the register is read. To determine if the condition that caused the status change is persistent, the register bit should be read twice (once to clear, once to read the new value).

Address: **0x1D**
Register Name: **dpll_bw**
Default Value: **0xA3**
Type: **R/W**

Bit Field	Function Name	Description
0	Reserved	
3:1	bandwidth	000: reserved, do not use 001: reserved, do not use 010: reserved, do not use 011: 14 Hz 100: 28 Hz (limited to 14 Hz for 2 kHz references) 101: (Default) 890 Hz (limited to 14 Hz and 56 Hz for 2 kHz and 8 kHz references respectively) 110: reserved, do not use 111: reserved, do not use
7:4	Reserved	

Address: **0x1F**
Register Name: **dpll_modesel**
Default Value: **0x02**
Type: **R/W**

Bit Field	Function Name	Description
1:0	modesel	DPLL mode of operation 00: **Synchronous Mode**. In this mode, the DPLL output is synchronized with the selected reference input. If the selected reference fails, the device enters holdover mode. 01: **Asynchronous Holdover Mode**. In this mode, the DPLL continues to generate a clock with frequency accuracy based on historical frequency data collected while the DPLL was synchronized. 10: **Asynchronous Freerun Mode**. This is the default mode. 11: **Reserved.**
7:2	Reserved	

Address: **0x20**
Register Name: **dpll_refsel**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
2:0	refsel	DPLL reference selection. 000: ref 0 001: ref 1 010: ref 2 011 - 111:do not use
7:3	Reserved	

Address: **0x52**
Register Name: **clk_freq**
Default Value: **0x42**
Type: **R/W**

Bit Field	Function Name	Description
3:0	apll_clk_freq	Sets the frequency of the clk output. Set to 0xAB for 25 MHz output.
7:4	Reserved	

Address: **0x64**
Register Name: **page_pointer**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	page_pointer	Use to access extended page addresses 00 - General registers 01 - 0F Extended Registers

Address: **0x65**
Register Name: **ref_freq_mode**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
1:0	ref0_freq_mode	0: Telecom frequency. See Table 1. 1: Ethernet frequency 25 MHz. Requires configuration shown in Figure 3. All other values reserved.
3:2	ref1_freq_mode	0: Telecom frequency. See Table 1. 1: Ethernet frequency 25 MHz*. Requires configuration shown in Figure 3. All other values reserved.
5:4	ref2_freq_mode	0: Telecom frequency. See Table 1. 1: Ethernet frequency 25 MHz. Requires configuration shown in Figure 3. All other values reserved.

Address: **0x65**
Register Name: **ref_freq_mode**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:6	Reserved	

Address: **0x67**
Register Name: **25M_in_freq_config_0**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	25M_config7:0	Bits 7:0 of a 14-bit value that defines the input reference frequency. Set to 0x35 for 25 MHz. Leave as default for telecom frequencies.

Address: **0x68**
Register Name: **25M_in_freq_config_1**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
5:0	25M_config13_8	Bits 13:8 of a 14-bit value that defines the input reference frequency. Set to 0x0C for 25 MHz. Leave as default for Telecom input frequencies.
7:6	Reserved	

Address: **0x69**
Register Name: **scm_low**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	scm_low_lim	Defines the SCM low limit. Set to 0x06 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x6A**
Register Name: **scm_high**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	scm_high_lim	Defines the SCM high limit. Set to 0x12 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x6B**
Register Name: **cfm_low_0**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit. Set to 0x37 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x6C**
Register Name: **cfm_low_1**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit. Set to 0x06 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x6D**
Register Name: **cfm_hi_0**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit. Set to 0x99 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x6E**
Register Name: **cfm_hi_1**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit. Set to 0x06 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x6F**
Register Name: **cfm_cycle**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	cfm_cycle	Defines the number of cycles that are monitored in the given sample window. Set to 0x80 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.

Address: **0x70**
Register Name: **ref_div4**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
0	ref_div4	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. Set to 0x01 for a 25 MHz input frequency. Leave as default for Telecom input frequencies.
7:1	Reserved	Leave as default.

4.2 Extended Page Registers

The following registers are located in the extended address pages. These registers are accessed by first setting the extended address page pointer located at address 0x64 on the main address page.

Address: **04_0x65 - Extended Page 4 Register**
Register Name: **apll_fconv_0**
Default Value: **0xE0**
Type: **R/W**

Bit Field	Function Name	Description
7:0	apll_fconv7_0	Sets the apll center frequency. Set to 0x7C for generating 25 MHz. **Note: Changing to values other than recommended values may cause abnormal operation.**

Address: **04_0x66 - Extended Page 4 Register**
Register Name: **apll_fconv_1**
Default Value: **0x97**
Type: **R/W**

Bit Field	Function Name	Description
7:0	apll_fconv15_8	Sets the apll center frequency. Set to 0x92 for generating 25 MHz. **Note: Changing to values other than recommended values may cause abnormal operation.**

Address: **07_0x6E - Extended Page 7 Register**
Register Name: **vco_lim**
Default Value: **0x6E**
Type: **R/W**

Bit Field	Function Name	Description
7:0	vco_lim	Sets the internal VCO limits. **Note: Changing to values other than recommended values may cause abnormal operation.**

5.0 AC and DC Electrical Characteristics

DC Electrical Characteristics - Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	-0.5	4.6	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	3.1	3.3	3.5	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	1.7	1.8	1.9	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	1.8V Core Supply Current	$I_{1.8\_CORE}$		129	180	mA	osci = 20 MHz
2	3.3V Supply Current	$I_{3.3}$		5	7	mA	osci = 20 MHz
5	Total Power Dissipation	P_{T_D}		TBD	TBD	mW	Clock output running at 25 MHz
6	CMOS high-level input voltage	V_{IH}	0.7*V_{DD}			V	Applies to osci pin
7	CMOS low-level input voltage	V_{IL}			0.3*V_{DD}	V	
8	Input leakage current	I_{IL}	-15		15	µA	V_I = V_{DD} or 0 V
9	Input leakage current low for pull-up pads	I_{IL_PU}	-121		-23	µA	V_I = 0 V
10	Input leakage current high for pull-up pads	I_{IL_PD}	23		121	µA	V_I = V_{DD}
11	Schmitt trigger Low to High threshold point	V_{t+}	1.35		1.85	V	All CMOS inputs are schmitt level triggered
12	Schmitt trigger High to Low threshold point	V_{t-}	0.80		1.15	V	
13	CMOS high-level output voltage	V_{OH}	2.4			V	I_{OH} = 8 mA on clk & fp output. I_{OH} = 4 mA other outputs
14	CMOS low-level output voltage	V_{OL}			0.4	V	I_{OL}= 8 mA on clk & fp output. I_{OL} = 4 mA other outputs

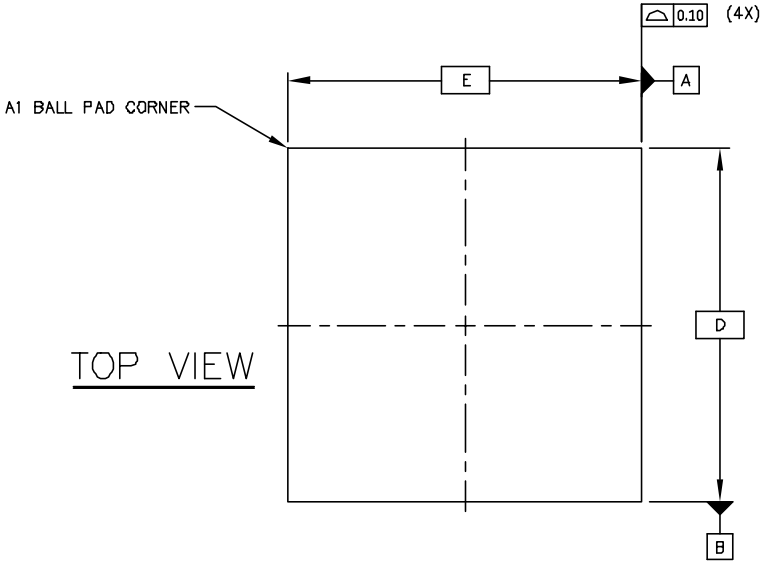
* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

Output Jitter Generation (CLK)

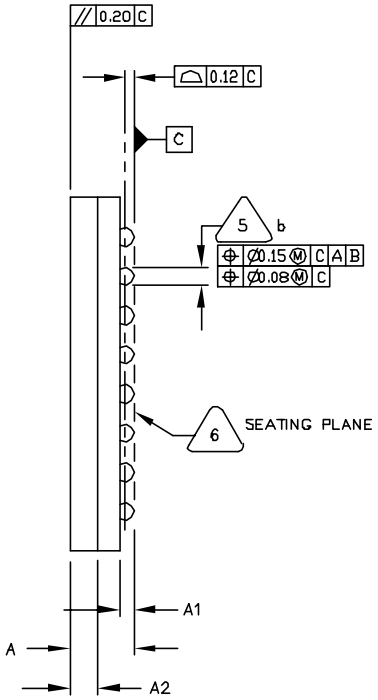
Output Frequency	Jitter Measurement Filter	Jitter Generation		
		Typ[1]	Max[2]	Units
25 MHz	unfiltered	5.6	7.8	ps_{RMS}
		49.2	89.6	ps_{P-P}
25 MHz	637 kHz to Nyquist	1.5	1.7	ps_{RMS}
		12.6	14.4	ps_{P-P}

[1] Typical jitter specifications are measured when operating at nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

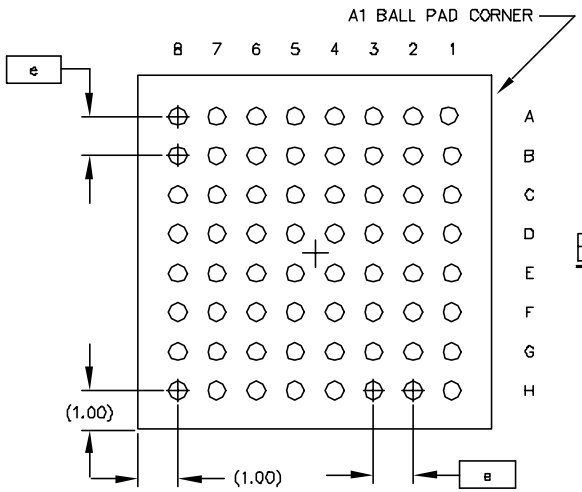
[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all outputs enabled.



TOP VIEW



SIDE VIEW



BOTTOM VIEW

64 SOLDER BALLS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D		9.00 REF.	
E		9.00 Ref.	
e		1.0 Ref	
n		64	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039

For more information about all Zarlink products
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TECHNICAL DOCUMENTATION - NOT FOR RESALE