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CMOS **MT88E41**

Extended Voltage Calling Number Identification Circuit (ECNIC)

Data Sheet

DS5717 Issue 3 February 1998

Features

- 1200 baud BELL 202 and CCITT V.23 Frequency Shift Keying (FSK) demodulation
- Compatible with Bellcore GR-30-CORE and SR-TSV-002476
- High input sensitivity: -36dBm minimum FSK Detection Level
- Simple serial 3-wire data interface eliminating the need for a UART
- Power down mode
- Internal gain adjustable amplifier
- Carrier detect status output
- Uses 3.579545 MHz crystal
- 2.7 - 5.5V operation
- Low power CMOS technology

Applications

- Calling Number Delivery (CND), Calling Name Delivery (CNAM) and Calling Identity on Call Waiting (CIDCW) features of Bellcore CLASS^{SM} service
- Feature phones
- Phone sets, adjunct boxes
- FAX machines
- Telephone answering machines
- Database query systems
- Battery powered applications

Ordering Information

MT88E41AE	16 Pin Plastic DIP
MT88E41AS	16 Pin SOIC
MT88E41AN	20 Pin SSOP

-40 °C to +85 °C

Description

The MT88E41 Extended Voltage Calling Number Identification Circuit (ECNIC) is a CMOS integrated circuit providing an interface to various calling line information delivery services that utilize 1200 baud BELL 202 or CCITT V.23 FSK voiceband data transmission schemes. The ECNIC receives and demodulates the signal and outputs data into a simple 3-wire serial interface.

Typically, the FSK modulated data containing information on the calling line is sent before alerting the called party or during the silent interval between the first and second ring using either CCITT V.23 recommendations or Bell 202 specifications.

The ECNIC accepts and demodulates both CCITT V.23 and BELL 202 signals. Along with serial data and clock, the ECNIC provides a data ready signal to indicate the reception of every 8-bit character sent from the Central

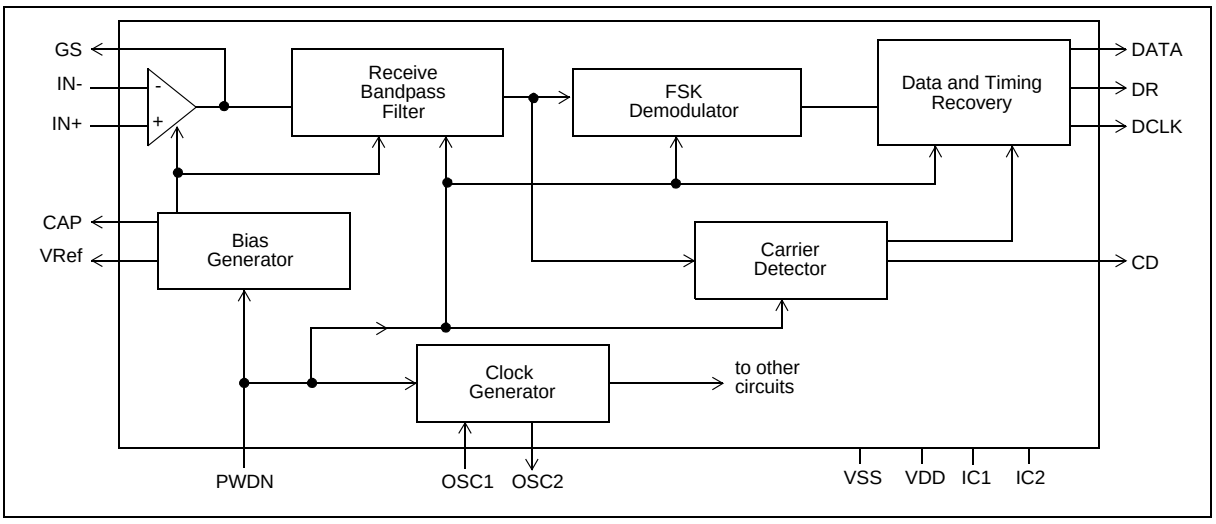

Figure 1 - Functional Block Diagram

CLASS^{SM} is a service mark of Bellcore

Office. The received data can be processed externally by a microcontroller, stored in memory, or displayed as is, depending on the application.

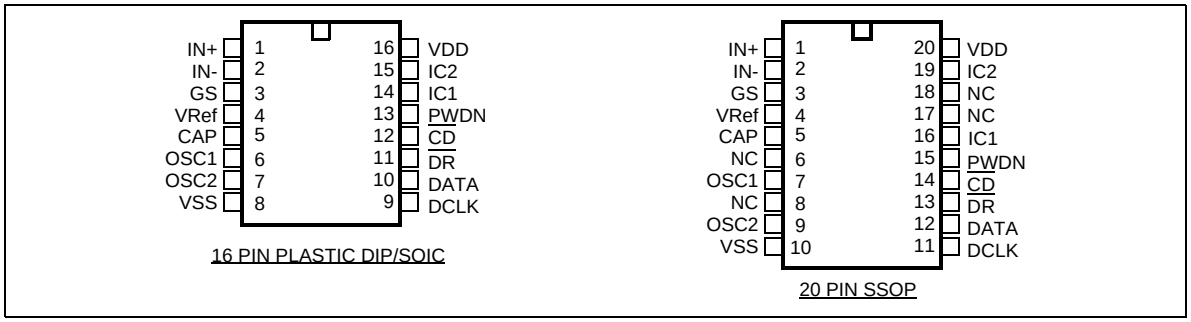

Figure 2 - Pin Connections

Pin Description Table

Pin #		Name	Description
16	**20**		
1	1	IN+	**Non-inverting Op-Amp (Input).**
2	2	IN-	**Inverting Op-Amp (Input).**
3	3	GS	**Gain Select (Output).** Gives access to op-amp output for connection of feedback resistor.
4	4	V_{Ref}	**Voltage Reference (Output).** Nominally $V_{DD/2}$. This is used to bias the op-amp inputs.
5	5	CAP	**Capacitor.** Connect a 0.1µF capacitor to V_{SS}.
6	7	OSC1	**Oscillator (Input).** Crystal connection. This pin can be driven directly from an external clocking source.
7	9	OSC2	**Oscillator (Output).** Crystal connection. When OSC1 is driven by an external clock, this pin should be left open.
8	10	V_{SS}	Power supply ground.
9	11	DCLK	**Data Clock (Output).** Outputs a clock burst of 8 low going pulses at 1202.8Hz (3.5795MHz divided by 2976). Every clock burst is initiated by the DATA stop bit start bit sequence. When the input DATA is 1202.8 baud, the positive edge of each DCLK pulse coincides with the middle of the data bits output at the DATA pin. No DCLK pulses are generated during the start or stop bits. Typically, DCLK is used to clock the eight data bits from the 10 bit data word into a serial-to-parallel converter.
10	12	DATA	**Data (Output).** Serial data output corresponding to the FSK input and switching at the input baud rate. Mark frequency at the input corresponds to a logic high, while space frequency corresponds to a logic low at the DATA output. With no FSK input, DATA is at logic high. This output stays high until $\overline{CD}$ has become active.
11	13	$\overline{DR}$	**Data Ready (Open Drain Output).** This output goes low after the last DCLK pulse of each word. This can be used to identify the data (8-bit word) boundary on the serial output stream. Typically, $\overline{DR}$ is used to latch the eight data bits from the serial-to-parallel converter into a microcontroller.
12	14	$\overline{CD}$	**Carrier Detect (Open Drain Output).** A logic low indicates that a carrier has been present for a specified time on the line. A time hysteresis is provided to allow for momentary discontinuity of carrier.

Pin Description Table (continued)

Pin #		Name	Description
16	**20**		
13	15	PWDN	**Power Down (Input).** Active high, Schmitt Trigger input. Powers down the device including the input op-amp and the oscillator.
14	16	IC1	**Internal Connection 1.** Connect to V_{SS}.
15	19	IC2	**Internal Connection 2.** Internally connected, leave open circuit.
16	20	V_{DD}	Positive power supply voltage.
	6, 8, 17, 18	NC	No Connection.

1.0 Functional Description

The MT88E41 Extended Voltage Calling Number Identification Circuit (ECNIC) is a device compatible with the Bellcore proposal (GR-30-CORE) on generic requirements for transmitting asynchronous voiceband data to Customer Premises Equipment (CPE) from a serving Stored Program Controlled Switching System (SPCS) or a Central Office (CO). This data transmission technique is applicable in a variety of services like Calling Number Delivery (CND), Calling Name Delivery (CNAM) or Calling Identity Delivery on Call Waiting (CIDCW) as specified in Custom Local Area Signalling Service (CLASS^{SM}) calling information delivery features by Bellcore.

With CND, CNAM and CIDCW service, the called subscriber has the capability to display or to store the information on the calling party which is sent by the CO and received by the ECNIC.

In the CND service, information about a calling party is embedded in the silent interval between the first and second ring. During this period, the ECNIC receives and demodulates the 1200 baud FSK signal (compatible with Bell-202 specification) and outputs data into a 3-wire serial interface.

In the CIDCW service, information about a second calling party is sent to the subscriber, (while the subscriber is engaged in another call). During this period, the ECNIC receives and demodulates the FSK signal as in the CND case.

The ECNIC is designed to provide the data transmission interface required for the above service at the called subscriber location either in the on-hook case as in CND, or the off-hook case, as in CIDCW. The functional block diagram of the ECNIC is shown in Figure 1. Note however, for CIDCW applications, a separate CAS (CPE Alerting Signal) detector is required.

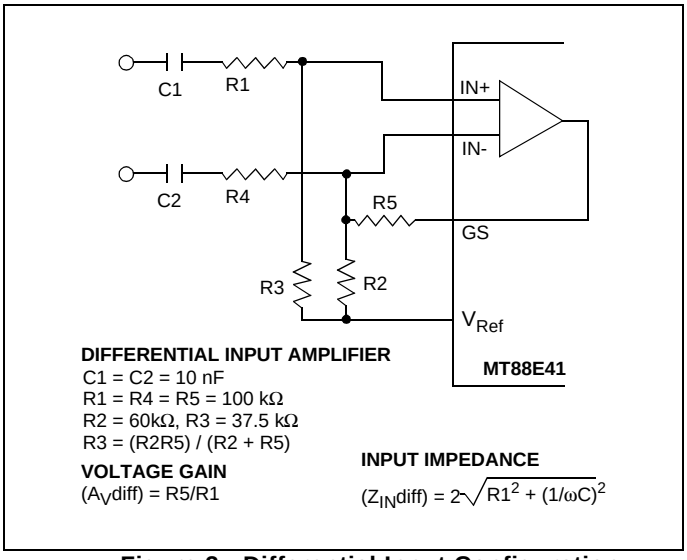

Figure 3 - Differential Input Configuration

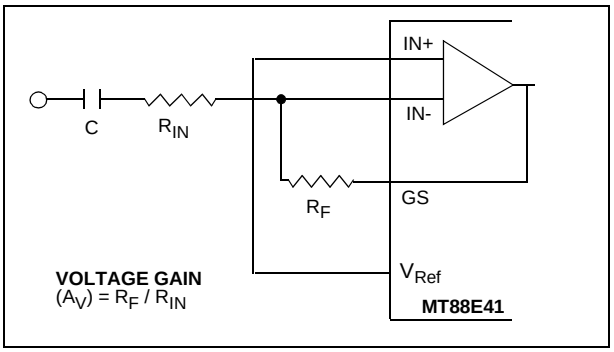

Figure 4 - Single-Ended Input Configuration

In Europe, Caller ID and CIDCW services are being proposed. These schemes may be different from their North American counterparts. In most cases, 1200 baud CCITT V.23 FSK is used instead of Bell 202. Because the ECNIC can also demodulate 1200 baud CCITT V.23 with the same performance, it is suitable for these applications.

Although the main application of the ECNIC is to support CND and CIDCW service, it may also be used in any application where 1200 baud Bell 202 and/or CCITT V.23 FSK data reception is required.

1.1 Input Configuration

The input arrangement of the MT88E41 provides an operational amplifier, as well as a bias source (V_{Ref}) which is used to bias the inputs at $V_{DD/2}$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 4.

Figure 3 shows the necessary connections for a differential input configuration.

1.2 User Interface

The ECNIC provides a powerful 3-pin interface which can reduce the external hardware and software requirements. The ECNIC receives the FSK signal, demodulates it, and outputs the extracted data to the DATA pin. For each received stop bit start bit sequence, the ECNIC outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each clock rising edge corresponds to the centre of each DATA bit cell (providing the incoming baud rate matches the DCLK rate). DCLK is not generated for the stop and start bits. Consequently, DCLK will clock only valid data into a peripheral device such as a serial to parallel shift register or a micro-controller. The ECNIC also outputs an end of word pulse (data ready) at the DR pin. The data ready signal indicates the reception of every 10-bit word sent from the Central Office. This output is typically used to interrupt a micro-controller. The three outputs together, eliminate the need for a UART (Universal Asynchronous Receiver Transmitter) or the high software overhead of performing the UART function (asynchronous serial data reception).

Note that the 3-pin interface may also output data generated by voice since these frequencies are in the input frequency detection band of the device. The user may choose to ignore these outputs when FSK data is not expected, or force the ECNIC into its powerdown mode.

1.3 Power Down Mode

For applications requiring reduced power consumption, the ECNIC can be forced into power down when it is not needed to receive FSK data. This is done by pulling the PWDN pin high. In powerdown mode, the crystal oscillator, op-amp and internal circuitry are all disabled and the ECNIC will not react to the input signal. DATA and DCLK are at logic high, and DR and CD are at high impedance or at logic high when pulled up with resistors.The ECNIC can be awakened for reception of the FSK signal by pulling the PWDN pin to ground (see Figure 9).

1.4 Carrier Detect

The presence of the FSK signal is indicated by a logic low at the carrier detect ($\overline{CD}$) output. This output has built in hysteresis to prevent toggling when the received signal is shortly interrupted. Note that the $\overline{CD}$ output is also activated by voice since these frequencies are in the input frequency detection band of the device. The user may choose to ignore this output when FSK data is not expected, or force the ECNIC into its powerdown mode.

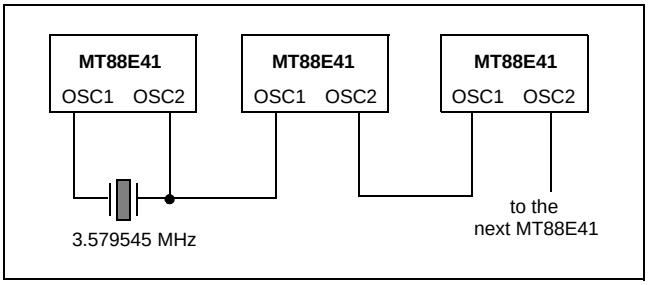

Figure 5 - Common Crystal Connection

1.5 Crystal Oscillator

The ECNIC uses a crystal oscillator as the master timing source for filters and the FSK demodulator. The crystal specification is as follows:

Frequency:	*3.579545 MHz*
Frequency tolerance:	*±0.1%(-40°C+85°C)*
Resonance mode:	*Parallel*
Load capacitance:	*18 pF*
Maximum series resistance:	*150 ohms*
Maximum drive level (mW):	*2 mW*

e.g. CTS MP036S

A number of MT88E41 devices can be connected as shown in Figure 5 such that only one crystal is required. The connection between OSC2 and OSC1 can be D.C. coupled as shown, or A.C. coupled using 30pF capacitors. Alternatively, the OSC1 inputs on all devices can be driven from a CMOS buffer (dc coupled) with the OSC2 outputs left unconnected.

1.6 VRef and CAP Inputs

V_{Ref} is the output of a low impedance voltage source equal to $V_{DD/2}$ and is used to bias the input op-amp. A 0.1µF capacitor is required between CAP and V_{SS} to suppress noise on $V_{Ref.}$

2.0 Applications

The circuit shown in Figure 6 illustrates the use of the MT88E41 device in a typical FSK receiver system. Bellcore Special Report SR-TSV-002476 specifies that the FSK receiver should be able to receive FSK signal levels as follows:

Received Signal Level at 1200Hz:

-32dBm to -12dBm

Received Signal Level at 2200Hz:

-36dBm to -12dBm

This condition can be attained by choosing suitable values of R1 and R2. The MT88E41 configured in a unity gain mode as shown in Fig. 6 meets the above level requirements.

For applications requiring detection of lower FSK signal level, the input op amp may be configured to provide adequate gain.

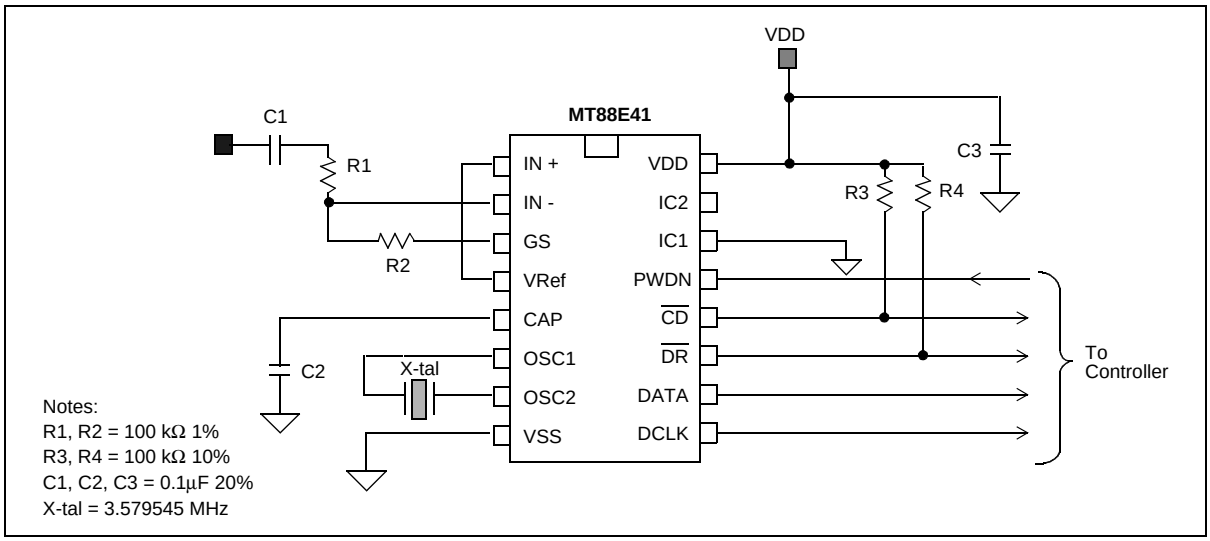

Figure 6 - Application Circuit (Single-Ended Input)

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage V_{DD} to V_{SS}	V_{DD}	-0.3	6	V
2	Voltage on any pin	V_P	-0.3	V_{DD}+0.3	V
3	Current at any pin (except V_{DD} and V_{SS})	$I_{I/O}$		±10	mA
4	Storage Temperature	T_{ST}	-65	+150	°C
5	Package Power Dissipation	P_D		500	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	2.7		5.5	V	
2	Clock Frequency	f_{OSC}		3.579545		MHz	
3	Tolerance on Clock Frequency	Δfc			±0.1	%	
4	Operating Temperature		-40		+85	°C	

DC Electrical Characteristics†

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	SUPPLY	Standby Supply Current V_{DD}=2.7V V_{DD}=5.5V	I_{DDQ}		 7 15	 14 28	 µA µA	PWDN=V_{DD}
2		Operating Supply Current V_{DD}=2.7V V_{DD}=5.5V	I_{DD}		 1 3	 2 5	 mA mA	PWDN=V_{SS}
3	DATA DCLK	Low Level Output Voltage High Level Output Voltage	V_{OL} V_{OH}	 V_{DD}-0.4		0.4	V V	I_{OL}=2.5mA I_{OH}=0.8mA
4	$\overline{DR}$ $\overline{CD}$	Sink Current	I_{OL}	2.5			mA	V_{OL}=0.4V
5	PWDN	Schmitt Input High Threshold Schmitt Input Low Threshold	V_{T+} V_{T-}	0.48*V_{DD} 0.28*V_{DD}		0.68*V_{DD} 0.48*V_{DD}	V V	
6		Schmitt Hysterisis	V_{HYS}	0.2			V	
7		Input Current	I_{IN}			10	µA	$V_{SS} \le V_{IN} \le V_{DD}$
8	VRef	Output Voltage	V_{Ref}	0.5V_{DD} - 0.05		0.5V_{DD} + 0.05	V	No Load
9		Output Resistance	R_{Ref}			2	kΩ	

† DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
* Typical figures are at 25°C and are for design aid only.

Electrical Characteristics† - Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Leakage Current	I_{IN}			1	µA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input Resistance	R_{in}	5			MΩ	
3	Input Offset Voltage	V_{OS}			25	mV	
4	Power Supply Rejection Ratio	PSRR	30	40		dB	1kHz ripple on V_{DD}
5	Common Mode Rejection	CMRR	30	40		dB	$V_{CMmin} \le V_{IN} \le V_{CMmax}$
6	DC Open Loop Voltage Gain	A_{VOL}	30	32		dB	
7	Unity Gain Bandwidth	f_C	.2	0.3		MHz	
8	Output Voltage Swing	V_O	0.5		V_{DD}-0.5	V_{pp}	Load ≥ 50kΩ
9	Maximum Capacitive Load (GS)	C_L			100	pF	
10	Maximum Resistive Load (GS)	R_L	50			kΩ	
11	Common Mode Range Voltage	V_{CM}	1.0		V_{DD}-1.0	V	

† Electrical characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FSK Detection

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Input Detection Level		-36 12.3		-9 275	dBm mV	1, 2, 3 1, 2, 3
2	Input Baud Rate		1188	1200	1212	baud	7
3	Input Frequency Detection Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	
4	Input Noise Tolerance 20 log(	SNR	20			dB	2, 3, 4, 5

† AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Timing

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	PWDN OSC1	Power-up time	t_{PU}		35	50	ms	
2		Power-down time	t_{PD}		100	1000	µs	11
3	$\overline{CD}$	Input FSK to $\overline{CD}$ low delay	t_{IAL}			25	ms	
4		Input FSK to $\overline{CD}$ high delay	t_{IAH}	8			ms	
5		Hysteresis		8			ms	
6	DATA	Rate		1188	1200	1212	bps	6,12
7		Input FSK to DATA delay	t_{IDD}		1	5	ms	
8	DATA DCLK	Rise time	t_R			200	ns	8
9		Fall time	t_F			200	ns	8
10		DATA to DCLK delay	t_{DCD}	6	416		µs	6, 7, 10
11		DCLK to DATA delay	t_{CDD}	6	416		µs	6, 7, 10
12	DCLK	Frequency		1200	1202.8	1205	Hz	7
13		High time	t_{CH}	415	416	417	µs	7
14		Low time	t_{CL}	415	416	417	µs	7
15	DCLK $\overline{DR}$	DCLK to $\overline{DR}$ delay	t_{CRD}	415	416	417	µs	7
16	$\overline{DR}$	Rise time	t_{RR}			10	µs	9
17		Fall time	t_{FF}			200	ns	9
18		Low time	t_{RL}	415	416	417	µs	7

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

***Notes:**

1. dBm=decibels above or below a reference power of 1mW into 600Ω.
2. Using unity gain test circuit shown in Figure 6.
3. Mark and Space frequencies have the same amplitude.
4. Band limited random noise (200-3200Hz).
5. Referenced to the minimum input detection level.
6. FSK input data at 1200 ±12 baud.
7. OSC1 at 3.579545 MHz ±0.2%.
8. 10k to V_{SS}, 50pF to V_{SS}.
9. 10k to V_{DD}, 50pF to V_{SS}.
10. Function of signal condition.
11. The device will stop functioning within this time, but more time may be required to reach I_{DDQ}.
12. For a repeating mark space sequence, the data stream will typically have equal 1 and 0 bit durations.

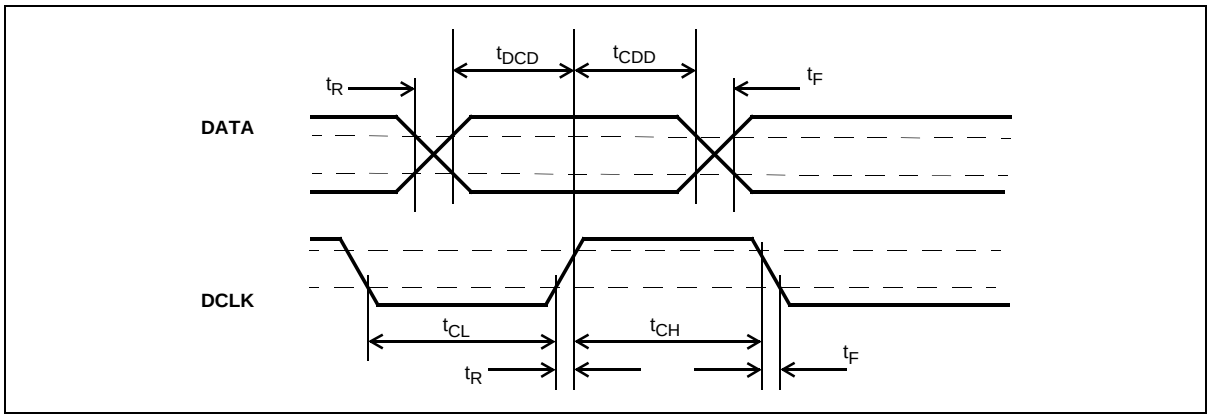

Figure 7 - DATA and DCLK Output Timing

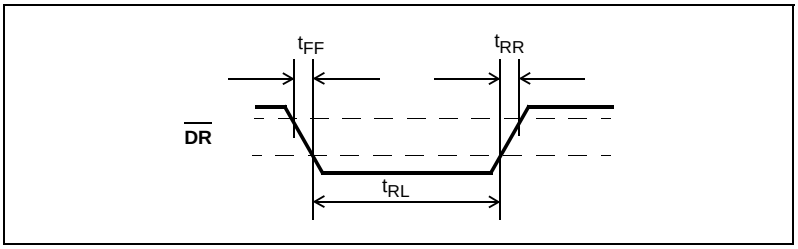

Figure 8 - $\overline{\text{DR}}$ Output Timing

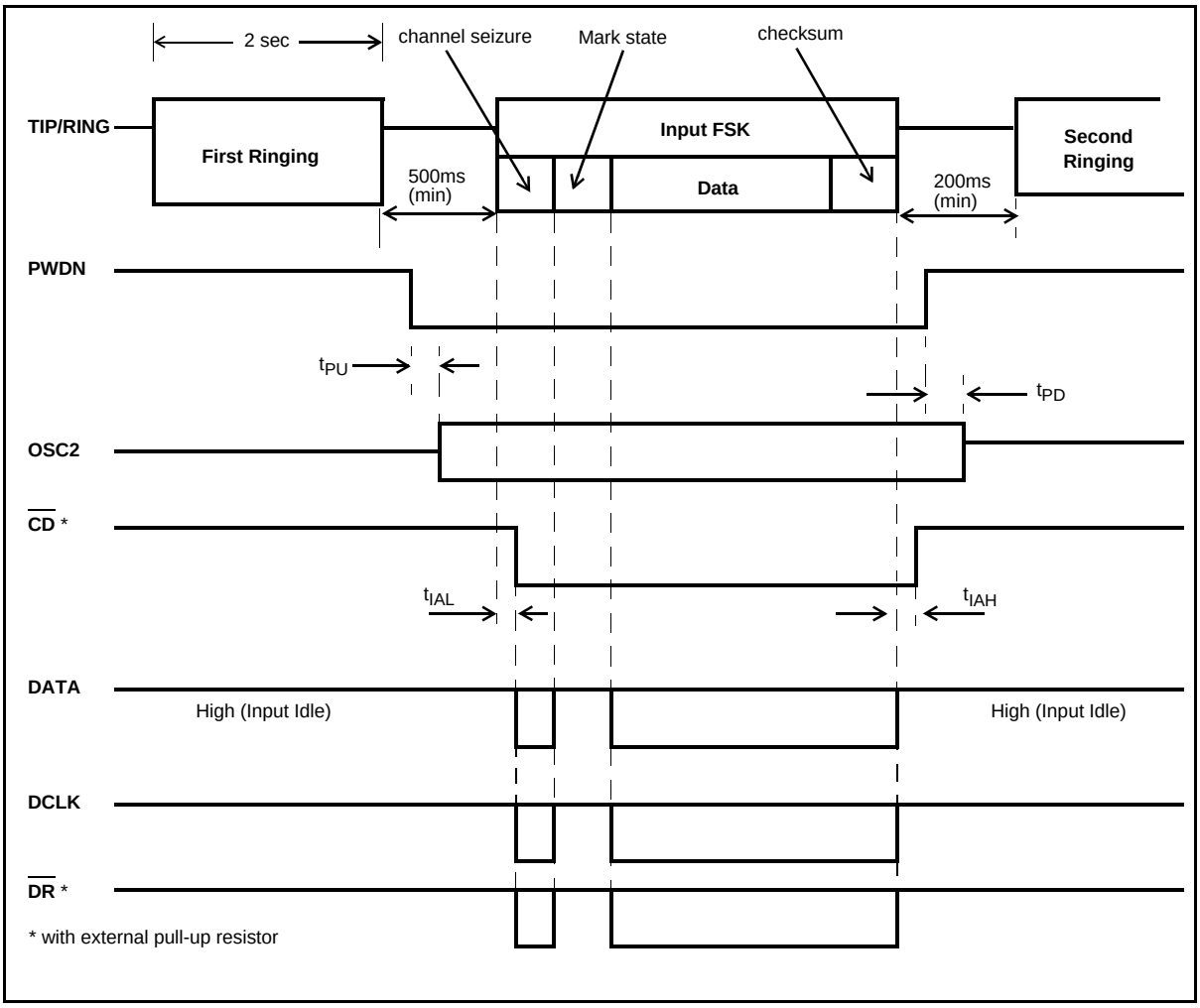

Figure 9 - Input and Output Timing (Bellcore CND Service)

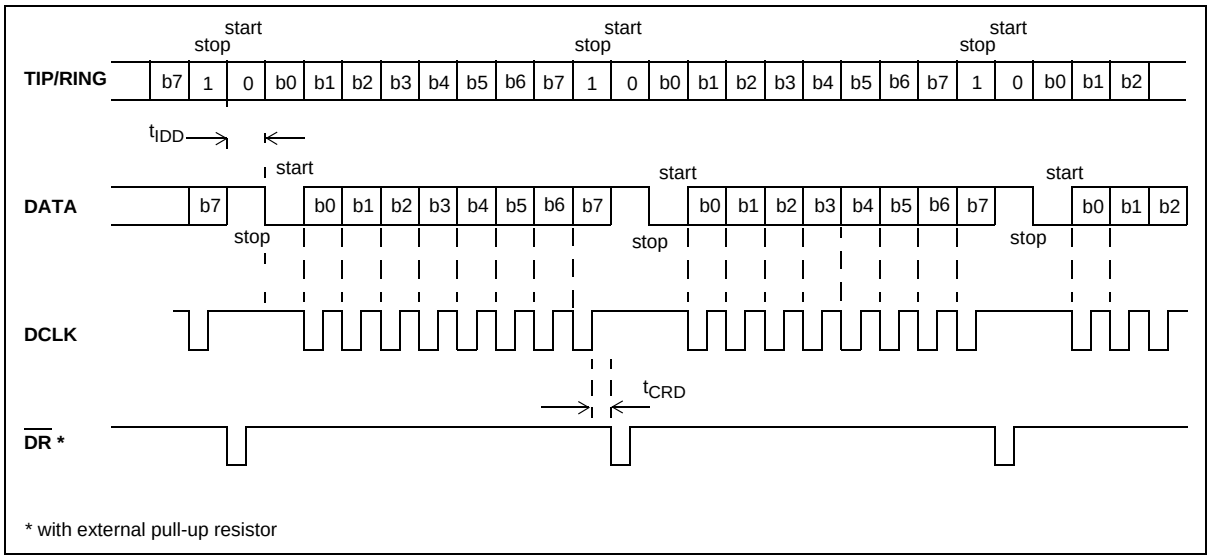

Figure 10 - Serial Data Interface Timing

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