Applications of the MT90503 External SRAM Memory

Application Note

Issue 1 February 2003

Contents

Related Documents

- "MT90503 2048 VC AAL1 SAR" Data Sheet, Zarlink Semiconductor, DS5509, Issue 2, September 2002
- "MT90503 API User Guide" Design Manual, Zarlink Semiconductor, Revision 2.2, November 2002
- "MT90503 Customer Evaluation Kit User Guide", Zarlink Semiconductor, Revision 2.2, December 2000
- "Minimizing the Number of External SSRAM Chips on Zarlink Packet Processors" Application Note, MSAN-222, Zarlink Semiconductor, Issue 2, December 2002
- "CY2308 Zero Delay Buffer", Cypress Semiconductor Corporation, Doc #38-07146
- "CY7C1352 256Kx18 Pipelined SRAM", Cypress Semiconductor Corporation, Doc #38-05080

1.0 Introduction

The MT90503 AAL1 SAR requires external data and control SRAM memory for its two independent memory interfaces, the control memory interface and the data memory interface. This application note will discuss the various aspects related to the selection and design of the external SRAM memories.

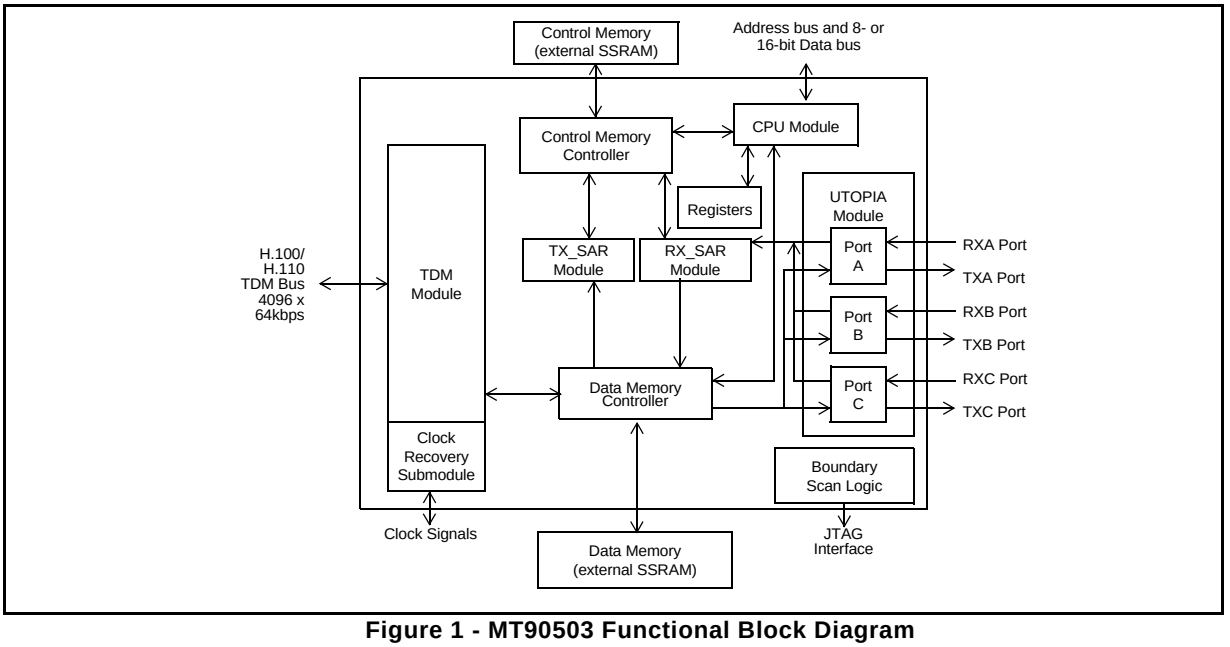

Figure 1 - MT90503 Functional Block Diagram

2.0 Control and Data Memory

The MT90503 supports flowthrough ZBT-SRAM, flowthrough SSRAM, pipelined ZBT-SRAM and pipelined SSRAM types of SRAM. With a 16-bit data bus, the MT90503 supports SRAM sizes of 128 KB, 256 KB, 512 KB and 1 MB using a 16-bit to 19-bit address bus, respectively.

2.1 Control Memory Interface

The control memory interface consists of a 16-bit data bus with parity and either a 19-bit address bus with one chip select or an 18-bit address bus with two chip selects. This allows the control memory interface to support up to 1 MB of SRAM, either in one chip of 512Kx18 or two chips of 256Kx18. This is a direct connection between the MT90503 and the SRAM chips. Figure 1, “MT90503 Control Memory SRAM Connection”, on page 3 shows the connection between the MT90503 control memory interface and a 512x18 SRAM.

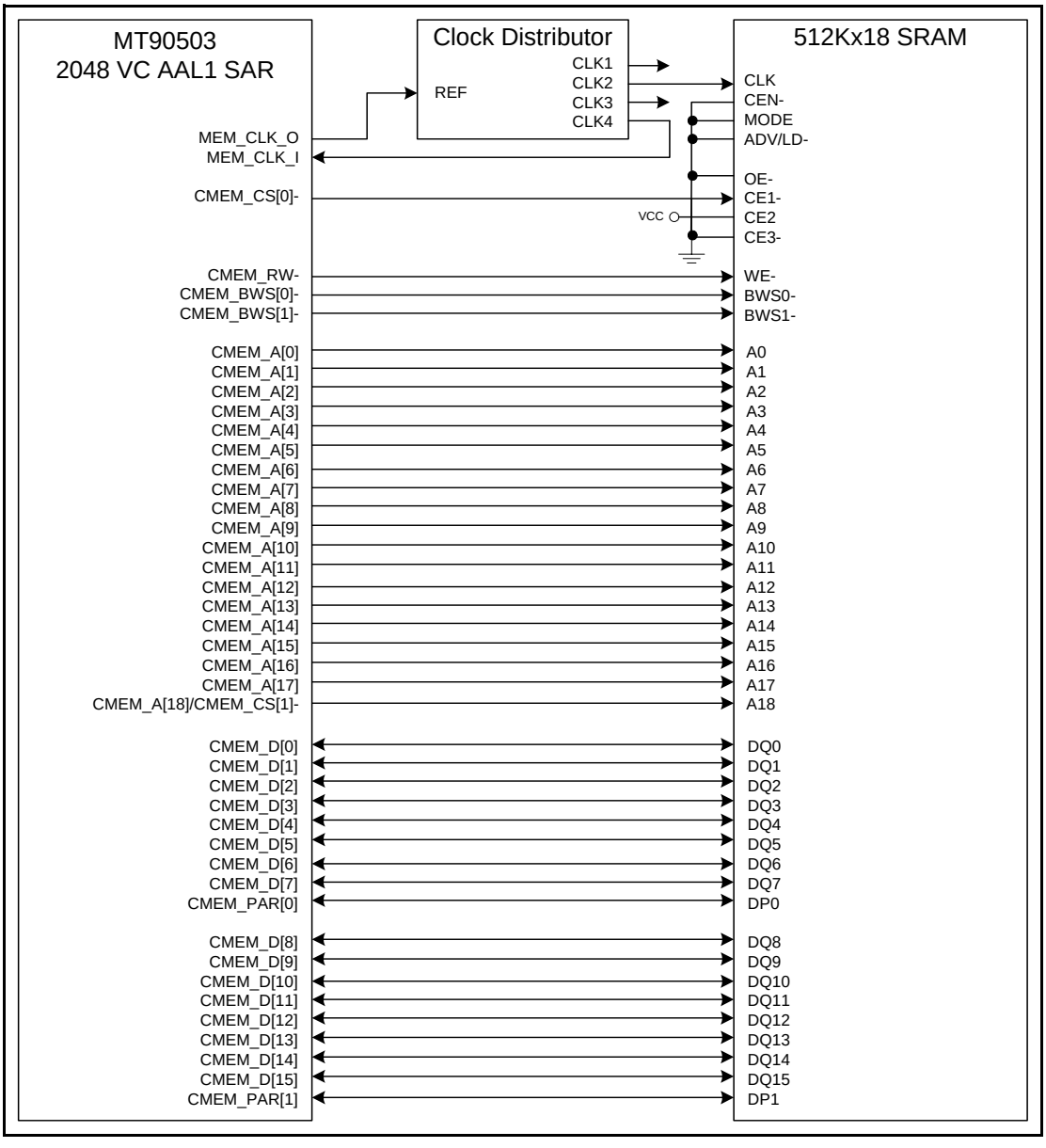

Figure 1 - MT90503 Control Memory SRAM Connection

2.2 Data Memory Interface

The data memory interface consists of a 16-bit data bus with parity, a 19-bit address bus and four chip selects. This allows the data memory interface to support up to 4 MB of SRAM in up to four memory chips. If support for 2 MB SRAM chips on this interface is desired, refer to MSAN-222 "Minimizing the Number of External SSRAM Chips on Zarlink Packet Processors". Figure 2, "MT90503 Data Memory SRAM Connection", on page 4 shows the connection between the MT90503 data memory interface and a 512x18 SRAM. Note that only one clock distributor is required on the board, but is shown in both Figure 1 and Figure 2. The unused DMEM_CS[x] from the MT90503 and CLKx from the clock distributor would control additional data memory SRAMs, if present.

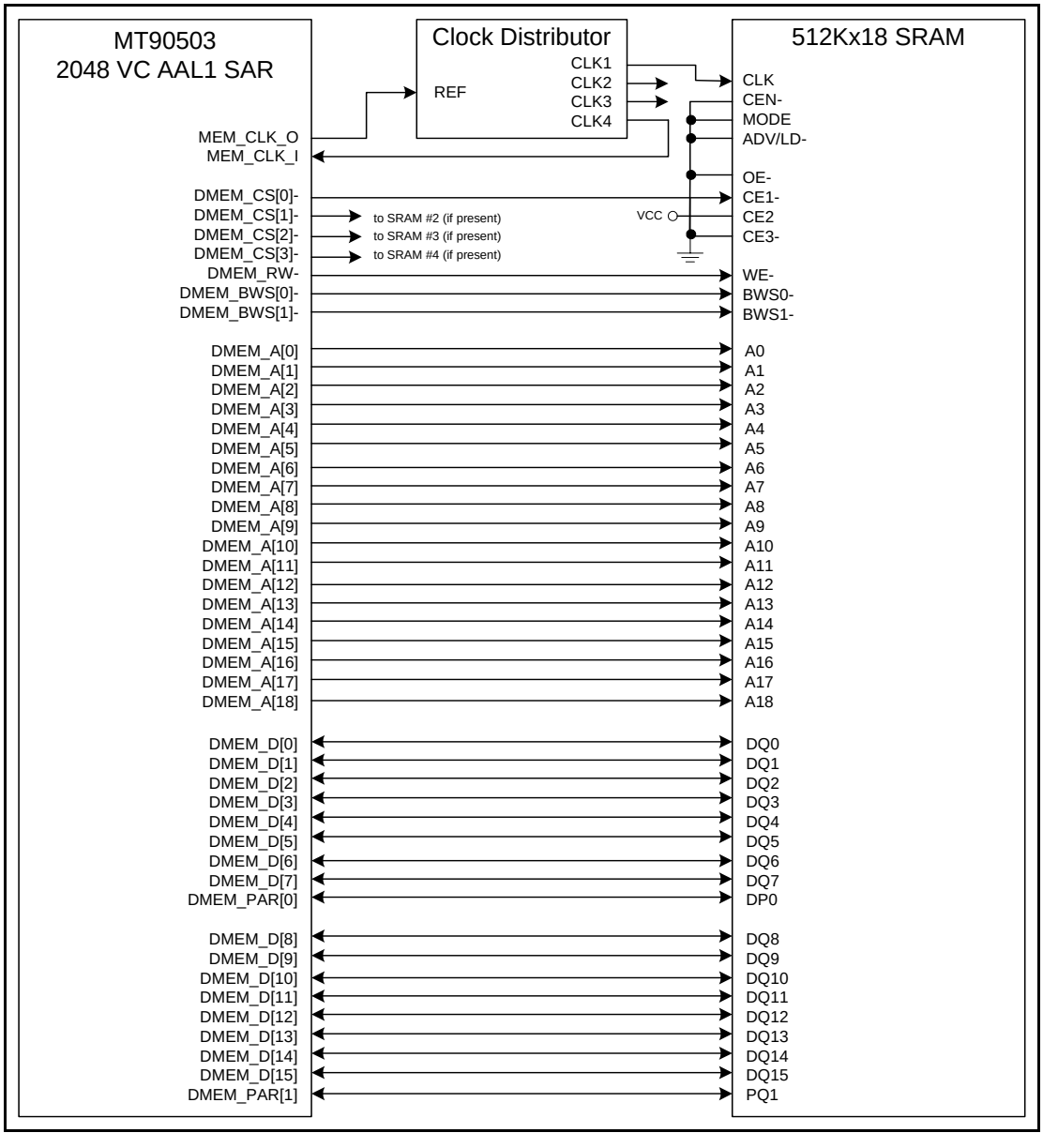

Figure 2 - MT90503 Data Memory SRAM Connection

3.0 Clock Distribution

The MT90503 is capable of providing an 80 MHz clock from its mem_clk_o pin to be utilized as the memory clock. This eliminates the need for an external oscillator. The 80 MHz clock is generated internal to the MT90503 using the mclk_src as the clock source. This memory clock is then distributed to each of the control and data SRAMs as well as the mem_clk_i pin on the MT90503. The maximum skew allowable between the memory clocks mem_clk_i on the MT90503 and CLK on the SRAMs is ±500 ps. On the MT90503 evaluation board this is achieved by using a zero delay buffer from Cypress Semiconductor (CY2308SC-1H) which has a maximum output-to-output skew of 200 ps.

4.0 Calculating External SRAM Required

4.1 Control SRAM Required

The control memory interface supports up to 1 MB of SRAM, which may be realized with either one SRAM chip sized 512Kx18 or with two SRAM chips each sized 256Kx18. The individual structures and buffers that reside in control memory is listed in Section 5.3.2 “Control Memory” of the MT90503 AAL1 SAR data sheet. The amount of control memory required is heavily dependent on the UTOPIA Look-Up Tables that utilize up to 256 KB per port. It is recommended that control memory support the full 1 MB of SRAM to allow for maximum flexibility of operation in the MT90503.

4.2 Data SRAM Required

The data memory interface supports up to 4 MB of SRAM, which may be realized across up to four SRAM chips. Using the technique described in MSAN-222 "Minimizing the Number of External SSRAM Chips on Zarlink Packet Processors”, the maximum amount of memory may be supported using two SRAM chips sized 1Mx18. The data memory contains the transmit circular buffers and the receive circular buffers that compensate for CDV. The amount of data memory required is dependent on the number of channels and the CDV of each channel.

4.2.1 Formulas

There are five possible VC types that may be opened on the MT90503. For each VC type a formula, given in Section 2.2.1 “mt90503_open_cbr_vc” of the MT90503 API User Guide, will calculate the required rx_circular_buffer_size given the desired CDV. This number is then used to determine to smallest buffer into which the channels in the VC may fit from the choices of 128 bytes, 256 bytes, 512 bytes and 1024 bytes. The tx_circular_buffer_size is, by design, the same size as the rx_circular_buffer_size and will occupy the same amount of memory. Note that there are a few bytes used in the circular buffer that are not accounted for by the simplified formulas below. Thus the actual size of circular buffer required may be slightly larger than anticipated by the formulas, potentially bumping up the buffer size if it is near the 128, 256, 512 or 1024 byte boundary.

1. T1 VCs with CAS using Strict Multi-framing

Value	Equation
rx_circular_buffer_size	((maximum_cdv[µs]/64) + (47/number_of_channels_in_VC) + 72) * 4/3
SRAM_per_channel	round_up(rx_circular_buffer_size) * 2
SRAM_per_VC	SRAM_per_channel * number_of_channels_in_VC
SRAM_for_x_VCs	number_of_VCs * SRAM_per_VC

Table 1 - SRAM Required for T1 VCs with CAS using Strict Multi-framing

2. T1 VCs with CAS using FASTCAS

Value	Equation
rx_circular_buffer_size	((maximum_cdv[µs]/64) + (47/number_of_channels_in_VC) + 48) * 4/3
SRAM_per_channel	round_up(rx_circular_buffer_size) * 2
SRAM_per_VC	SRAM_per_channel * number_of_channels_in_VC
SRAM_for_x_VCs	number_of_VCs * SRAM_per_VC

Table 2 - SRAM Required for T1 VCs with CAS using FASTCAS

3. E1 VCs with CAS using Strict Multi-framing

Value	Equation
rx_circular_buffer_size	((maximum_cdv[µs]/64) + (47/number_of_channels_in_VC) + 48) * 2
SRAM_per_channel	round_up(rx_circular_buffer_size) * 2
SRAM_per_VC	SRAM_per_channel * number_of_channels_in_VC
SRAM_for_x_VCs	number_of_VCs * SRAM_per_VC

Table 3 - SRAM Required for E1 VCs with CAS using Strict Multi-framing

4. E1 VCs with CAS using FASTCAS

Value	Equation
rx_circular_buffer_size	((maximum_cdv[µs]/64) + (47/number_of_channels_in_VC) + 32) * 2
SRAM_per_channel	round_up(rx_circular_buffer_size) * 2
SRAM_per_VC	SRAM_per_channel * number_of_channels_in_VC
SRAM_for_x_VCs	number_of_VCs * SRAM_per_VC

Table 4 - SRAM Required for E1 VCs with CAS using FASTCAS

5. Non Multi-framing VCs

Value	Equation
rx_circular_buffer_size	(maximum_cdv[µs]/64) + (47/number_of_channels_in_VC)
SRAM_per_channel	round_up(rx_circular_buffer_size) * 2
SRAM_per_VC	SRAM_per_channel * number_of_channels_in_VC
SRAM_for_x_VCs	number_of_VCs * SRAM_per_VC

Table 5 - SRAM Required for Non Multi-framing VCs

4.2.2 Non Multi-Framing Examples

A typical non multi-framing application will be utilized in this section. The assumptions for this application are that there are 64 VCs open, that each VC has 32 channels, and that each channel has the same circular buffer size to compensate for the same amount of CDV. The exact formula for this configuration is

Data SRAM [KB] = round_up(((2 x CDV [µs]) / 125) + 4) x 2) x 32 x 64 / 1024.

If a CDV of ±31.75 ms is desired for each of the 64 VCs, then 2048 KB of data memory would be required. Table 6, “SRAM vs. CDV for Non Multi-framing Application” on page 7 shows several examples of different target CDV support against the data SRAM required for the above configuration.

	Case #1	Case #2	Case #3	Case #4
Application	non-MF	non-MF	non-MF	non-MF
Target CDV support (ms)	±63.75	±31.75	±15.75	±7.75
rx_circular_buffer_size (bytes)	1024	512	256	128
SRAM_per_channel (bytes)	2048	1024	512	256
SRAM_per_VC (Kbytes)	64	32	16	8
SRAM_for_64_VCs (Kbytes)	4096	2048	1024	512

Table 6 - SRAM vs. CDV for Non Multi-framing Application

5.0 Miscellaneous Considerations

5.1 MT90503 Evaluation Board

The MT90503 evaluation board (MEB90503) uses Cypress CY7C1352-100AC 3.3V 256Kx18 SRAM chips. Two chips are used for control memory and four chips are used for data memory. The evaluation board schematics are available to use as a reference. The evaluation board ties the $\overline{OE}$ pin on the SRAMs to an FPGA. In normal operation the $\overline{OE}$ pin on each SRAM should be tied low. The evaluation board, as mentioned previously, uses the zero delay buffer CY2308SC-1H from Cypress Semiconductor.

5.2 Equivalent SRAM chips

The MT90503 evaluation board uses SRAM chips listed previously from Cypress Semiconductor. Below is a list of SRAM chips that are believed to provide equivalent functionality (ignoring the difference in sizes).

- Cypress CY7C1352 256Kx18 Pipelined SRAM with NoBL Architecture
- Cypress CY7C1354 256x36/512x18 Pipelined SRAM with NoBL Architecture
- Micron Pipelined ZBT MT55L256L18P1 (256K x 18)
- Motorola Pipelined ZBT MCM63Z818

5.3 External SRAM BIST

The MT90503 API has two functions, mt90503_open_cmem_bist and mt90503_open_dmem_bist, found in the mt90503_api_open.c file. These two functions are called internally by the API function mt90503_open when the chip is initialized in order to test the external control and data memory.

5.4 Memory Map

The control and data memory are mapped into the MT90503 address space at fixed locations, as listed in Table 34 “MT90503 Memory Map” of the MT90503 data sheet. The base address of control memory is 0x200000h. The base address of data memory is 0x400000h. These base addresses should not be modified.

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