Applications of the MT9088x Family Support SDT and UDT using the MT9072

Application Note

Issue 1 January 2003

Contents

Related Documents

- "MT90880/1/2/3 TDM to Packet Processors" Data Sheet, Zarlink Semiconductor, DS5568, Issue 2, December 2002
- "Performing Clock Recovery for Circuit Emulation when using the MT90880" Application Note, Zarlink Semiconductor, MSAN-198, Issue 1, August 2002
- "MT9072 Octal T1/E1/J1 Framer" Data Sheet, Zarlink Semiconductor, DS5063, Issue 4, September 2002

1.0 Circuit Emulation Service

The MT9088x family of TDM to Packet Processors may be used in combination with the MT9072 Octal T1/E1/J1 Framer to enable support for Circuit Emulation Service (CES) for Structured Data Transfer (SDT) and Unstructured Data Transfer (UDT) across an IP or Ethernet network. This application note will focus on the clocking scenarios, the data path and the configuration of the MT9072 and the MT90883. For information on performing clock recovery itself, refer to MSAN-198 "Performing Clock Recovery for Circuit Emulation when using the MT90880".

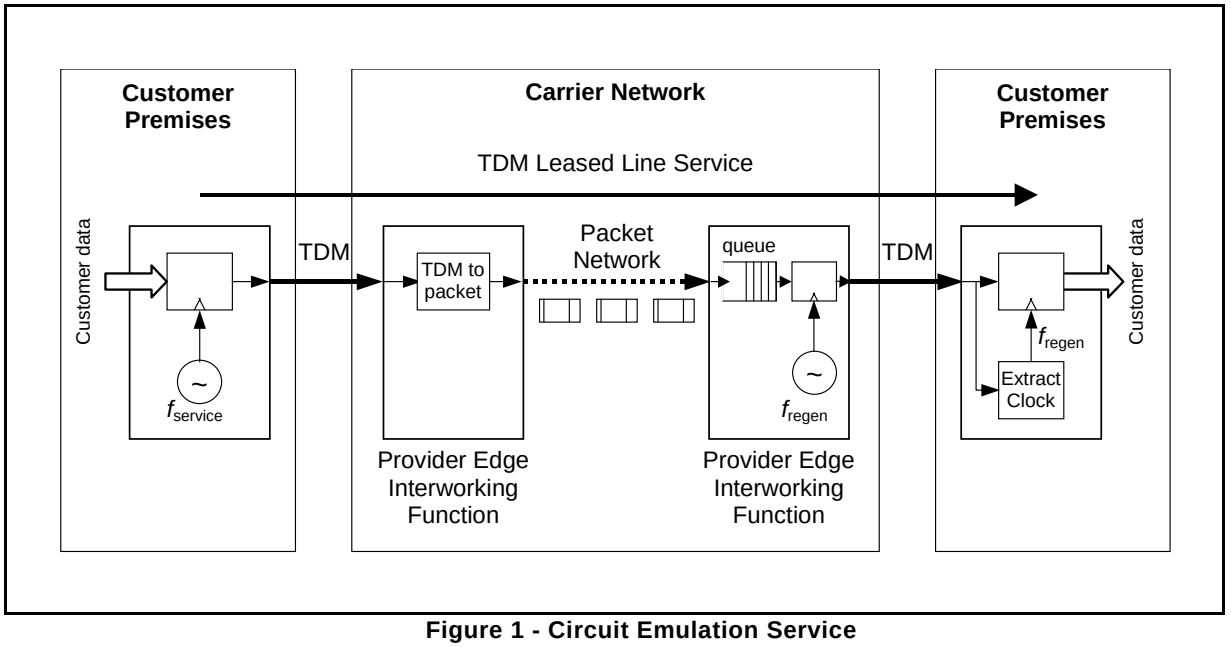

Figure 1 - Circuit Emulation Service

2.0 Flexible Design

The following two sections will discuss SDT and UDT support for synchronous and asynchronous operation. The term SDT refers to NxDS0 per channel service. The term UDT refers to unframed service, the emulating of an entire T1/E1 line without regard to channels or framing. The term synchronous refers to T1/E1 lines that are synchronized to a common clock and hence there will be no frequency differences between them. The term asynchronous refers to T1/E1 lines that do not share a common clock and hence may differ in frequency and data rate. The MT9072 is an octal T1/E1 framer that interfaces directly to an LIU on the line side and the mt90883 on the bus side. The MT9072 supports both termination mode (SDT) and transparent mode (UDT).

The overall architecture of the following design is capable of supporting SDT or UDT on each line independently. By way of example the following modes are supported - SDT synchronous, UDT synchronous, SDT asynchronous, UDT asynchronous, mixed mode SDT and UDT synchronous, mixed mode SDT and UDT asynchronous. Note, however, that for asynchronous operation, per-port clocking and clock recovery would be required. For synchronous operation only one PLL per card would be required and typically clock recovery would only be performed for two timing sources - one as the primary reference and one as a secondary reference to serve as a backup.

3.0 Synchronous Operation

The block diagram shown in Figure 2 “Synchronous TDM over Packet CES Block Diagram,” on page 3 will be discussed in this section. This design supports both SDT and UDT whether all lines are configured for SDT, all lines are configured for UDT or there is a mix of UDT and SDT lines.

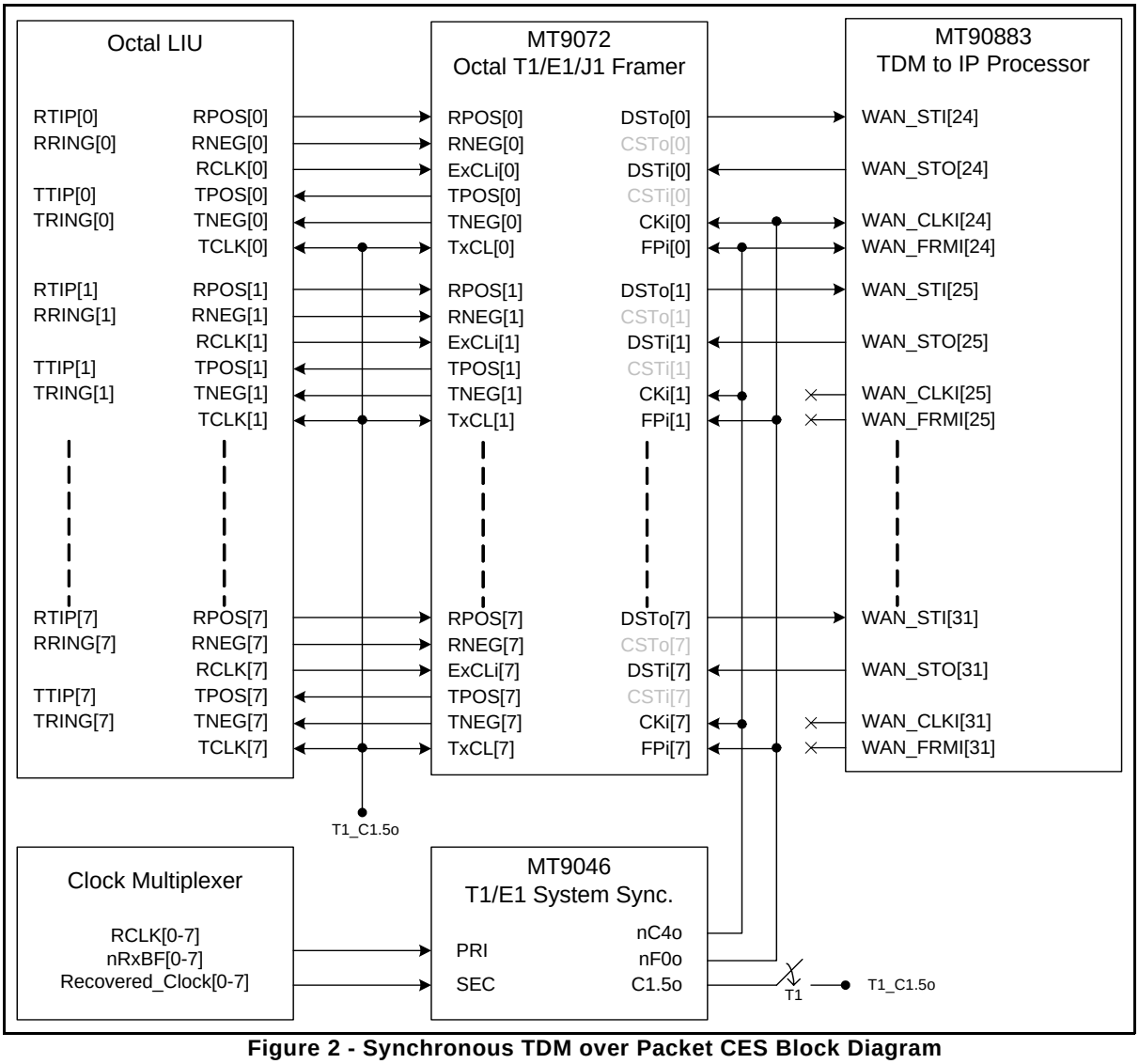

Figure 2 - Synchronous TDM over Packet CES Block Diagram

3.1 Synchronous UDT Operation

For synchronous UDT operation, the master clocking source on the card is the MT9046 PLL. The MT9046 generates the TDM bus clocks, C4o and F0o, which are driven to the MT9072 and the MT90883. The MT90883, operating in synchronous slave mode, will use the clock and frame pulse received on port 24 as its internal master TDM clock. For T1 operation, the MT9046 also generates a 1.544 MHz clock required as the transmit LIU clock, TxCL on the MT9072 and TCLK on the LIU. If the card synchronizes itself to the incoming T1/E1 line, then the primary and secondary reference sources for the MT9046 are taken from the RCLK on the LIU. If the card synchronizes itself to the timing received from the packet network, then the recovered clocks (either per port or two per card) are used to provide the primary and secondary reference sources to the MT9046.

The MT9072 is programmed for transparent mode of operation. In this mode, the MT9072 will pass data received from the LIU unaltered onto the TDM bus towards the MT90883. Likewise, data transmitted from the MT90883 towards the MT9072 will pass unaltered onto the LIU. Both the LIU and the MT9072 will be configured for uni-polar

or single rail NRZ operation, using only the RPOS and TPOS signals. For E1 operation, the MT90883 would construct an Ethernet packet using all 32 timeslots on the TDM bus, with a programmable number of frames per packet. An example UDT E1 Ethernet packet is shown in Figure 3 “UDT E1 Ethernet Packet,” on page 4.

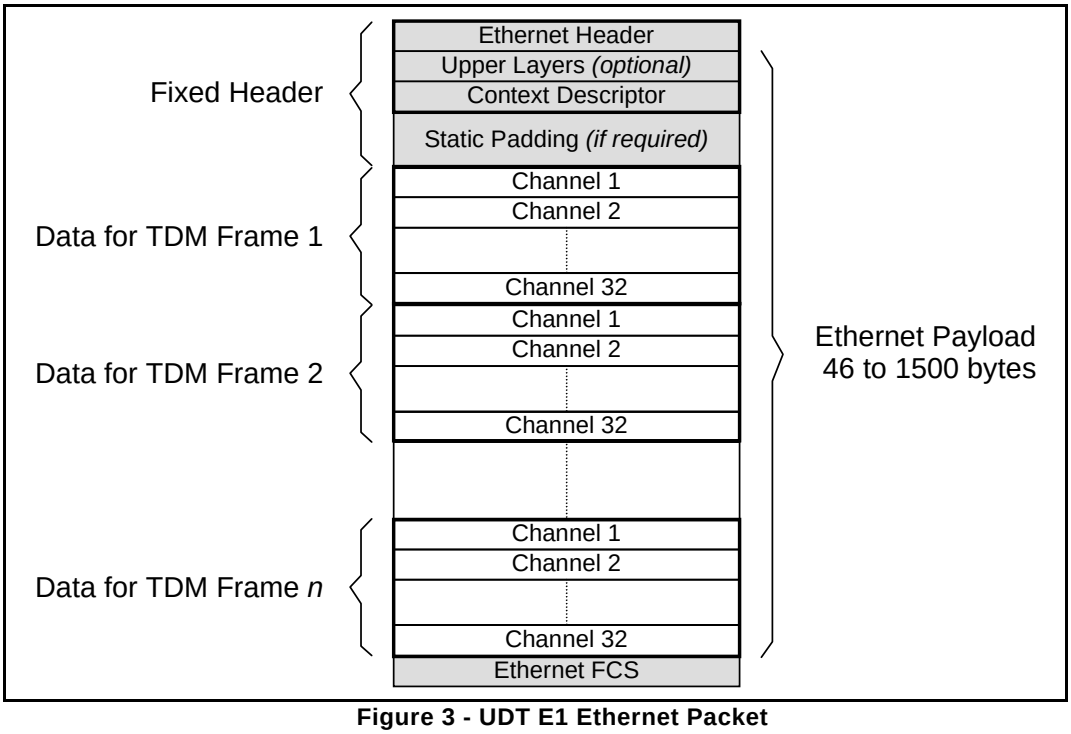

Figure 3 - UDT E1 Ethernet Packet

For T1 operation, the MT90883 would construct an Ethernet packet using the first 24 timeslots as well as the 32nd timeslot from the TDM bus. The 32nd timeslot contains the either the 193rd bit or the S-bit (if present), as well as 7 dummy bits. An example UDT T1 Ethernet packet is shown in Figure 4 “UDT T1 Ethernet Packet,” on page 5.

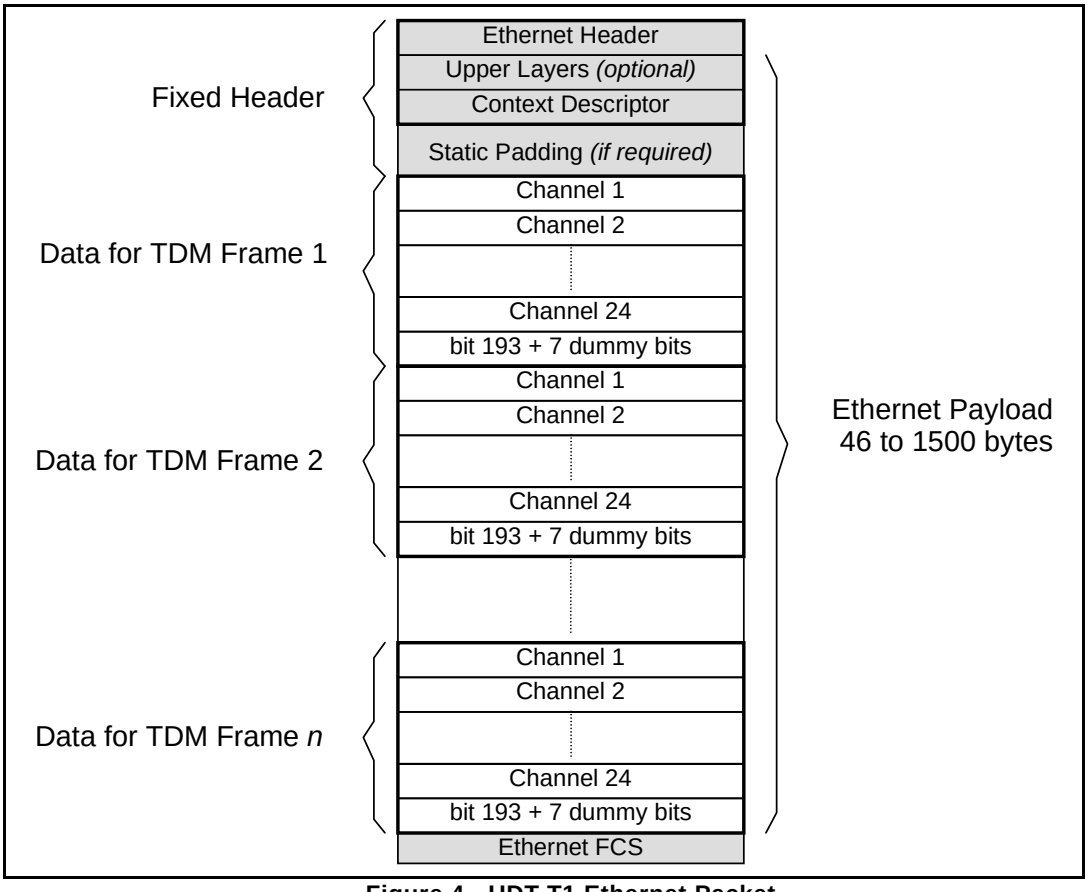

Figure 4 - UDT T1 Ethernet Packet

3.1.1 UDT LOS Transport

One important consideration for unstructured operation is that a loss of signal (LOS) reported by the LIU must be passed through the emulated circuit to the far end. The LOS is typically sent by replacing the data in the line with "all ones". In this design the LOS is carried across the network using functionality built-in to the MT9072. Once the microprocessor receives an LOS indication from the LIU, it will program the respective stream in the MT9072 to output the "all ones" data onto the TDM bus.

3.2 Synchronous SDT Operation

For synchronous SDT operation, the master clocking source on the card is the MT9046 PLL. The MT9046 generates the TDM bus clocks, C4o and F0o, which are driven to the MT9072 and the MT90883. The MT90883, operating in synchronous slave mode, will use the clock and frame pulse received on port 24 as its internal master TDM clock. For T1 operation, the MT9046 also generates a 1.544 MHz clock required as the transmit LIU clock, TxCL on the MT9072 and TCLK on the LIU. If the card synchronizes itself to the incoming T1/E1 line, then the primary and secondary reference sources for the MT9046 are taken from the RCLK on the LIU. If the card synchronizes itself to the timing received from the packet network, then the recovered clocks (either per port or two per card) are used to provide the primary and secondary reference sources to the MT9046.

The MT9072 is programmed for termination mode of operation. In this mode the MT9072 will effectively terminate the incoming T1 or E1 line and separate out its individual channels and pass them onto the MT90883 through each channel's respective timeslot on the TDM bus. The MT9072 will also operate on CAS or CCS by separating them

from the data or voice channels. The LIU and the MT9072 may be configured for either uni-polar or bi-polar operation. For either E1 or T1 operation the MT90883 will construct an Ethernet packet using a selected number of timeslots from the TDM bus. The number of channels in a connection or context may be as little as one channel or as many as all the channels across all the incoming lines. An example SDT Ethernet packet is shown in Figure 5 “SDT T1/E1 Ethernet Packet,” on page 6.

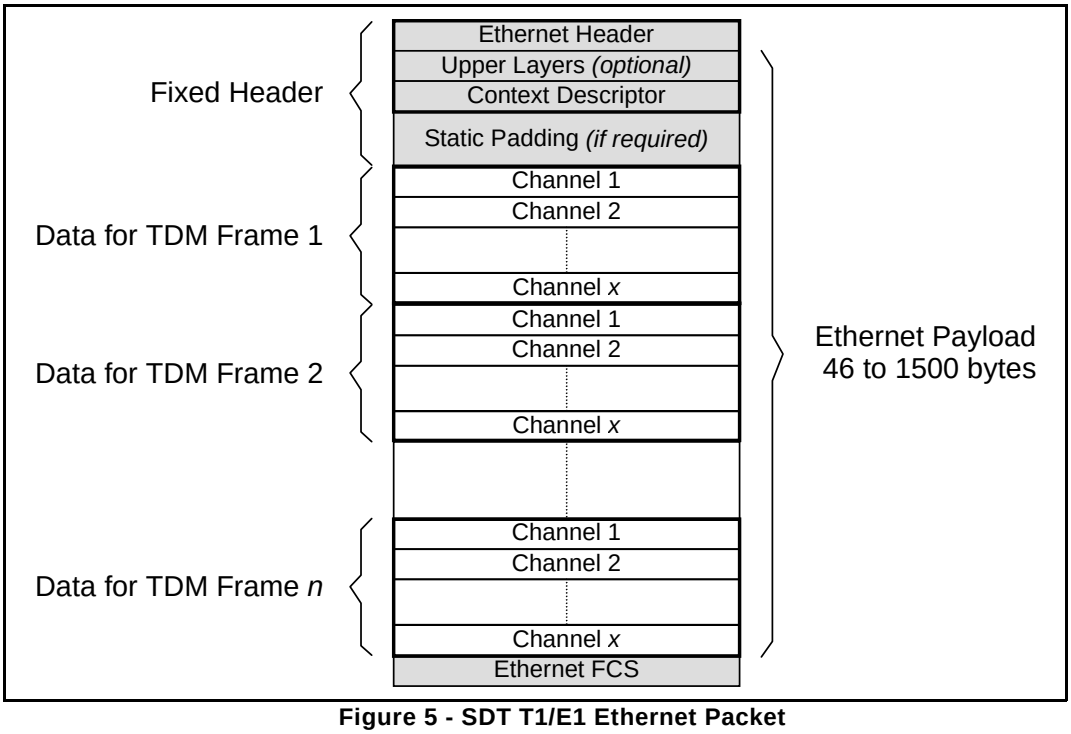

Figure 5 - SDT T1/E1 Ethernet Packet

3.2.1 Handling CCS Signalling

The MT9072 has the capability of passing the common channel signalling (CCS) received from the incoming T1/E1 line onto the control TDM bus (CSTo/CSTi). The selected timeslot(s) that carry CCS signalling would be assigned to specific timeslots on the CSTo line and passed onto the on-board microprocessor for processing. If it is desired that the CCS signalling be transported across the emulated circuit, the CCS signalling is also present on the matching DSTo timeslot. This timeslot could then be treated as a data channel by the MT90883, and be packetized and sent across the network.

3.2.2 Handling CAS Signalling

The MT9072 may be programmed to extract CAS from the incoming T1/E1 line. Likewise it may be programmed to inject CAS onto the outgoing T1/E1 line. The MT9072 handles CAS either through the microprocessor or through the control TDM bus.

If the MT9072 is programmed to handle CAS through the microprocessor then the CAS may be sent across the network using special CAS packets. The incoming CAS from the line would be stored in registers in the MT9072. An interrupt is generated by the MT9072 to notify the microprocessor whenever there is a CAS change on one of the channels. The microprocessor would then retrieve the new CAS value from the MT9072 register and create a special CAS signalling packet. This packet would be injected into the packet network through the mt90883 control bus (PCI) interface. The CAS signalling packet would then be received at the far end by another mt90883 and sent to the microprocessor on the far end card.

If the MT9072 is programmed to handle CAS through the control TDM bus then the CAS may be sent across the network using the same method as the data. It should be noted that this method of transporting CAS is non-standard, unlike the SDT with CAS standard utilized in ATM. As shown in Figure 6 “Synchronous TDM over Packet CES Carrying CAS,” on page 7, the control TDM bus would be connected to a port on the MT90883. The MT90883 would treat the timeslots on this port just as if they were carrying data. Thus the timeslots would be packetized by the MT90883 and sent across the network. Note that the figure shows only the first framer port connected to the first two MT0883 ports for simplicity.

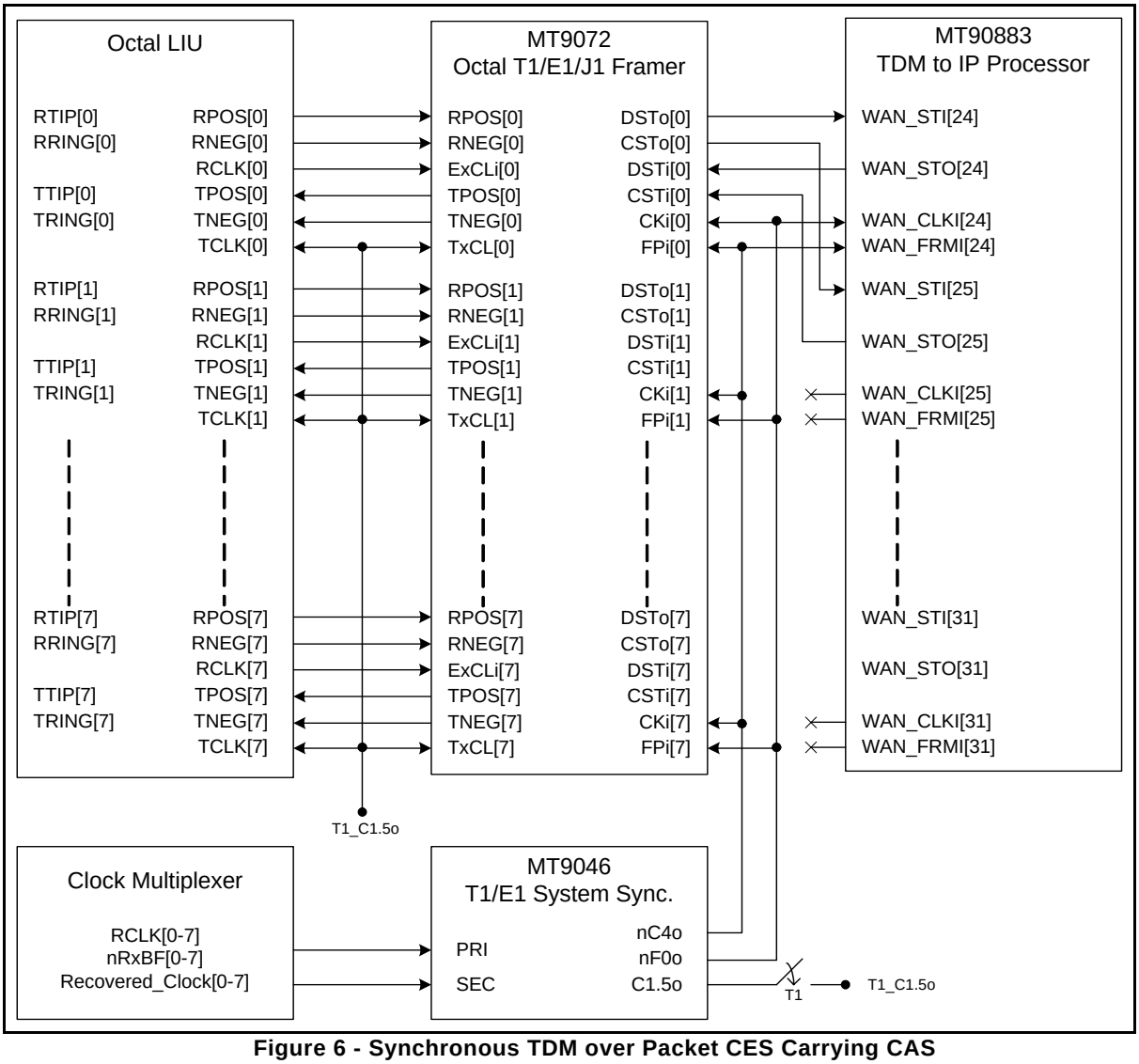

Figure 6 - Synchronous TDM over Packet CES Carrying CAS

By way of example, if there were 32 channels in a connection or context then the MT90883 would be configured to create a packet using the 32 timeslots on the data TDM bus and the 32 associated timeslots on the control TDM bus. This way the data and control timeslots would be passed together across the network and received together on the far end. The packet assembled by the MT90883 would be similar to Figure 7 “SDT T1/E1 CAS Ethernet Packet,” on page 8, assuming x equals 32. The downside to this approach is that the capacity of the MT90883 to carry data channels is halved. If originally all eight WAN ports were used to carry data channels, now a maximum of

four WAN ports would carry data (assuming of course that the other four WAN ports carried CAS). If two MT90883s (or one MT90881) operated in parallel then all eight incoming lines could be transported across the packet network with their associated CAS handled through the TDM bus. Additionally, in this configuration CAS is sent at an effective rate of 8 bits per frame (64 kbps) rather than 4 bits per multi-frame (2 kbps for E1, 1.3 kbps for T1). This increases the overall bandwidth utilization across the network.

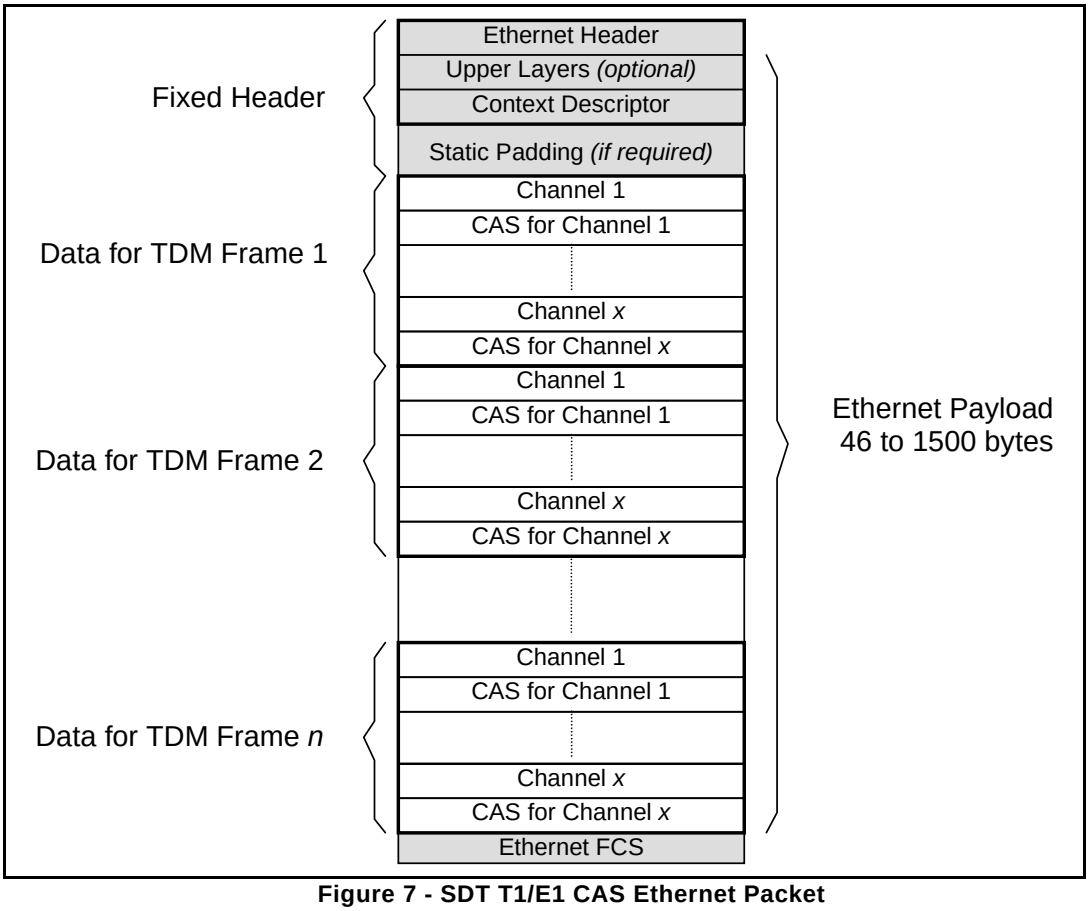

Figure 7 - SDT T1/E1 CAS Ethernet Packet

3.3 Synchronous Mixed SDT and UDT Operation

Each of the eight internal framers in the MT9072 is completely independent. On a framer-by-framer basis, each can be configured for either transparent or termination mode. For UDT lines the framer would be configured for transparent mode and for SDT lines the framer would be configured for termination mode. There is no change required in either the clocking structure of the card or the MT90883 operation to support mixed SDT and UDT operation.

4.0 Asynchronous Operation

The block diagram shown in Figure 8 “Asynchronous TDM over Packet CES Block Diagram,” on page 9 will be discussed in this section. This design supports both SDT and UDT whether all lines are configured for SDT, all lines are configured for UDT or there is a mix of UDT and SDT lines.

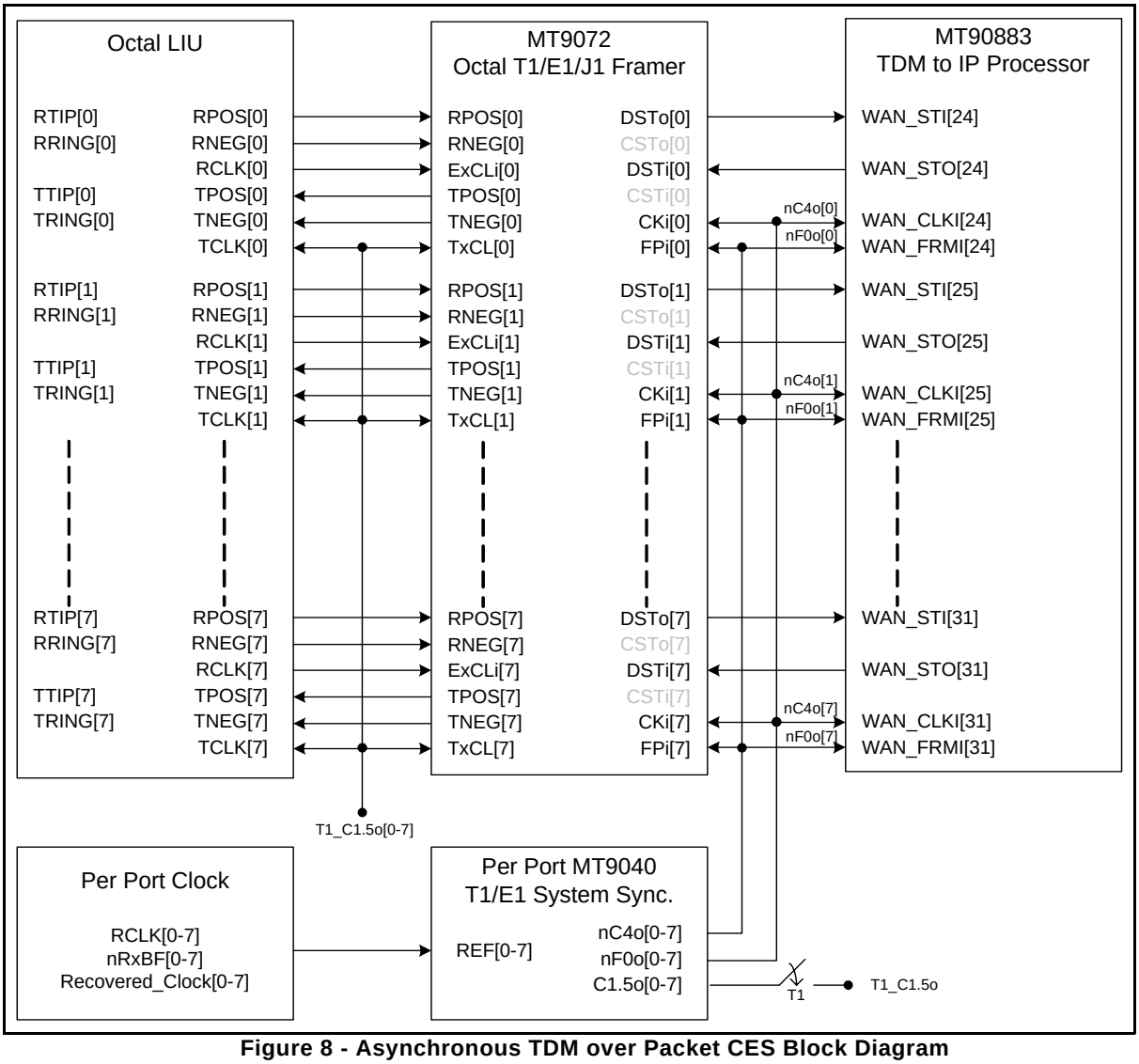

Figure 8 - Asynchronous TDM over Packet CES Block Diagram

4.1 Asynchronous UDT Operation

For asynchronous UDT operation, each line runs independently with respect to the timing. Each line could run at its own frequency, however the TX and RX links of the same line are assumed to be synchronous. Each line has a master clock sourced from its own MT9040 PLL. The MT9040 generates the TDM bus clocks, $\overline{C4o}$ and $\overline{F0o}$, which are driven to the MT9072 and the MT90883. The MT90883, operating in asynchronous mode, and the MT9072 will use the clock and frame pulse received on each port to clock data in and out of the device on a particular TDM port. For T1 operation, the MT9040 also generates a 1.544 MHz clock required as the transmit LIU clock, TxCL on the MT9072 and TCLK on the LIU. If the card synchronizes itself to the incoming T1 line, then the reference source for the MT9040 is taken from the RCLK on the LIU. If the card synchronizes itself to the timing received from the packet network, then the per port recovered clock is used to provide the reference source to the MT9040.

The MT9072 is programmed for transparent mode of operation. In this mode, the MT9072 will pass data received from the LIU unaltered onto the TDM bus towards the MT90883. Likewise, data transmitted from the MT90883

towards the MT9072 will pass unaltered onto the LIU. Both the LIU and the MT9072 will be configured for uni-polar or single rail NRZ operation, using only the RPOS and TPOS signals. For E1 operation, the MT90883 would construct an Ethernet packet using all 32 timeslots on the TDM bus, with a programmable number of frames per packet. An example UDT E1 Ethernet packet is shown in Figure 3 “UDT E1 Ethernet Packet,” on page 4. For T1 operation, the MT90883 would construct an Ethernet packet using the first 24 timeslots as well as the 32nd timeslot from the TDM bus. The 32nd timeslot contains the S-bit as well as 7 dummy bits. An example UDT T1 Ethernet packet is shown in Figure 4 “UDT T1 Ethernet Packet,” on page 5.

4.1.1 UDT LOS Transport

The UDT LOS Transport considerations in asynchronous UDT operation are the same as discussed in Section 3.1.1 “UDT LOS Transport” on page 5.

4.2 Asynchronous SDT Operation

For asynchronous SDT operation, each line runs independently with respect to the timing. Each line could run at its own frequency, however the TX and RX links of the same line are assumed to be synchronous. Each line has a master clock sourced from its own MT9040 PLL. The MT9040 generates the TDM bus clocks, C4o and F0o, which are driven to the MT9072 and the MT90883. The MT90883, operating in asynchronous mode, and the MT9072 will use the clock and frame pulse received on each port to clock data in and out of the device on a particular TDM port. For T1 operation, the MT9040 also generates a 1.544 MHz clock required as the transmit LIU clock, TxCL on the MT9072 and TCLK on the LIU. If the card synchronizes itself to the incoming T1/E1 line, then the reference source for the MT9040 is taken from the RCLK on the LIU. If the card synchronizes itself to the timing received from the packet network, then the per port recovered clock is used to provide the reference source to the MT9040.

The MT9072 is programmed for termination mode of operation. In this mode the MT9072 will effectively terminate the incoming T1 or E1 line and separate out its individual channels and pass them onto the MT90883 through each channel’s respective timeslot on the TDM bus. The MT9072 will also operate on CAS or CCS by separating them from the data or voice channels. The LIU and the MT9072 may be configured for either uni-polar or bi-polar operation. For either E1 or T1 operation the MT90883 will construct an Ethernet packet using a selected number of timeslots from the TDM bus. The number of channels in a connection or context is limited to 32 for E1 and 24 for T1 by the fact that each connection may only contain channels from the same line. This differs from synchronous operation where a connection may contain channels from any of the incoming lines. An example SDT Ethernet packet is shown in Figure 5 “SDT T1/E1 Ethernet Packet,” on page 6.

4.2.1 Handling CCS Signalling

Handling CCS signalling in asynchronous SDT operation is the same as discussed in Section 3.2.1 “Handling CCS Signalling” on page 6.

4.2.2 Handling CAS Signalling

Handling CAS signalling in asynchronous SDT operation is the same as discussed in Section 3.2.2 “Handling CAS Signalling” on page 6.

4.3 Asynchronous Mixed SDT and UDT Operation

Each of the eight internal framers in the MT9072 is completely independent. On a framer-by-framer basis, each can be configured for either transparent or termination mode. For UDT lines the framer would be configured for transparent mode and for SDT lines the framer would be configured for termination mode. There is no change required in either the clocking structure of the card or the MT90883 operation to support mixed SDT and UDT operation.

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