Contents

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1.0 The MT9076B Jitter Attenuator can Operate in 3 Different Timing Modes

1. System Bus Synchronous Mode (Figure 2 and 3)
2. Line Synchronous Mode (Figure 1 and 2)
3. Free-run Mode (Figure 1)

In all three timing modes the low jitter output of the on-chip digital PLL provides timing to the transmit side of the LIU.

2.0 MT9076B On-Chip PLL Brief Summary and Description

1. The MT9076 on-chip digital PLL attenuates jitter from 2.5 Hz with a roll-off of 20 dB/decade.
2. Locks to a 4.096 MHz input clock, or to the 1.544 MHz / 2.048 MHz extracted clock.
3. The intrinsic jitter is less than 0.02 UI.
4. Meets the jitter characteristics as specified in AT&T TR62411.
5. Meets the jitter characteristics as specified in ETS 300 011.

For the MT9076 in Bus-Sync mode operation, the C4b and F0b pins become inputs and C4b is used as the input reference to the on-chip digital PLL. In this case, C4b and F0b are generated by an external PLL referenced to the extracted line clock from the MT9076. The external PLL should have similar performance of the on-chip PLL.

3.0 Zarlink's Recommendation for External PLL used for MT9076 in Bus-Sync Mode

Zarlink's digital PLLs meet the MT9076 on-chip digital PLL requirements and should be used for providing the C4b and F0b inputs for the MT9076 due to the following reasons.

1. Network synchronization is a crucial and mandatory function in a system but is not something that our customers build their systems around or use to differentiate from competitors.
2. Zarlink's digital PLLs meet various telecommunications network synchronization standards.
3. Zarlink offers proven experience and expertise in providing reliable off-the-shelf standards compliant timing solutions.

Customers entrust this crucial network synchronization functionality to Zarlink. Zarlink recommends the following digital PLLs: MT9040, MT9043 and ZL30100, ZL30101 and ZL30102 for this application.

4.0 Examples for Various modes of Jitter Attenuation

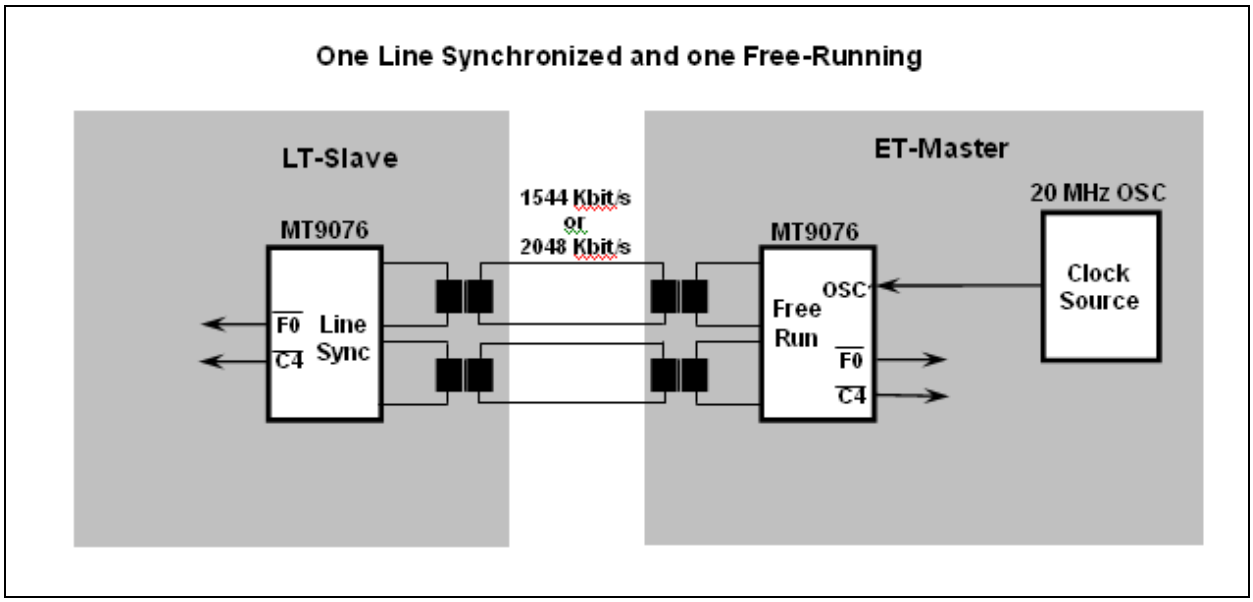

Figure 1 - Point to Point Master Slave Timing Configuration

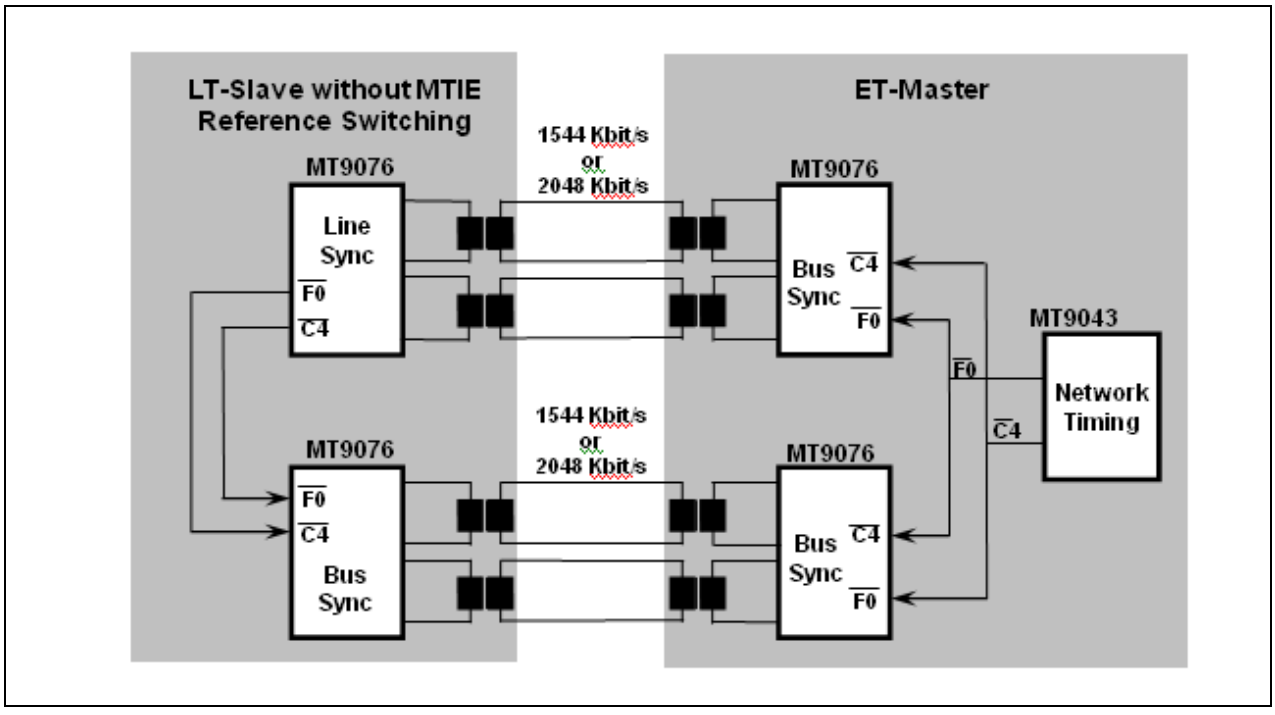

Figure 2 - Allows use of one PLL, but the timing will not be as robust as synchronization will be lost if the line in the slave link cards between two framers is broken.

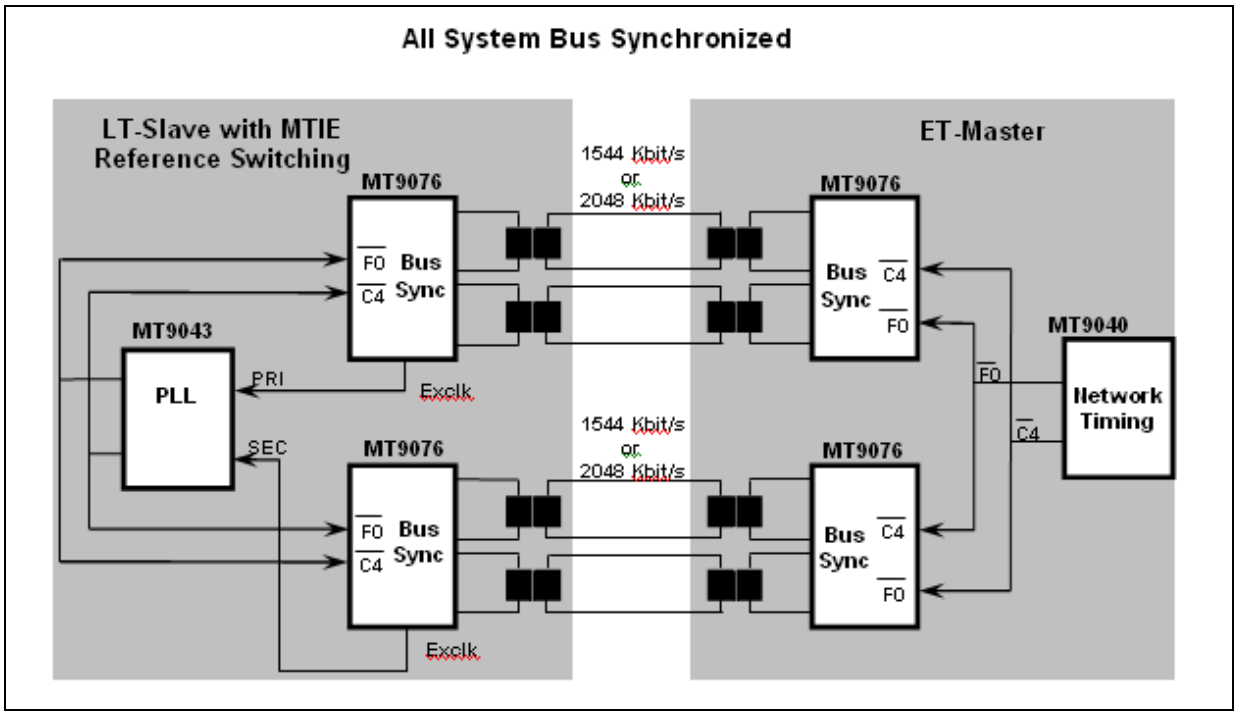

Figure 3 - A more resilient configuration, regarding an extra PLL with two reference inputs. The extracted clock is supplied to the MT9043 PLL which generates the synchronized timing for the system