SLIC Devices

Applications of the Zarlink SLIC Devices

Telephone Line card Powering Considerations with Monolithic SLIC Devices

Application Note

APPLICATION NOTE

This application note provides design considerations for reliable operation of all electronic devices on the line card printed circuit board (PCB), particularly when installing and removing line cards in active telephone switching equipment with powered backplanes. This application note only applies to Zarlink's non-battery switching SLIC devices.

GENERAL CHARACTERISTICS OF A MONOLITHIC SILICON CIRCUIT

Monolithic silicon circuits are designed and built with complex arrangements of both positive-doped and negative-doped regions on a bulk substrate of semiconductor silicon. In a bipolar process, such as that used in monolithic SLIC devices, individual transistors, diodes, and resistors are integrated on this substrate. The circuit is designed such that, under normal operating voltage polarities, different areas of the circuit are isolated by reverse-biased P-N junctions working as isolation barriers.

The substrate of Zarlink SLIC devices is electrically connected to the most negative voltage supply, which is nominally –48 to –56 V for a typical telephone line feed circuit. As long as other circuit elements on the same substrate are maintained at a positive electrical potential, with respect to the negative substrate, isolation is maintained. However, if an area of the circuit is connected to a voltage that is more negative than the substrate, a forward-biased P-N junction is formed and current may flow.

Because the substrate is physically large compared to the individual circuit areas, as current flows through the substrate, voltages develop across many circuit areas. If sufficient voltage potential exists across particular parts of the circuit, an area that previously served as an insulator can suddenly begin operating as a transistor. This is sometimes referred to as a *parasitic transistor* because its existence depends on abnormal bias conditions. This parasitic transistor normally has very poor gain characteristics because it is not designed to be part of the circuit. However, this parasitic device can cause unrelated circuit elements to become electrically tied together. If those elements are low impedance to different voltage levels, damaging currents can occur. Under some conditions, this causes severe damage to the entire device and can occur in any typical integrated circuit. It is not necessarily limited to monolithic SLIC devices.

Parasitic action as described above, or the application of above-specification voltages between pins, can subject the circuit paths in the device to very high current flow. These high currents actually can fuse the conduction path. The current may be high enough to completely fuse open the path or it may cause only partial destruction of that path. This path destruction releases conductive metal contamination or semiconductor doping elements that can permanently affect the performance of the surrounding silicon circuit elements, causing them to behave as if they were metal-doped in the manufacturing process. Because this type of failure can easily occur over an extended period, it may be misdiagnosed as a reliability problem when, in fact, it results from a stress-induced condition.

Any failure mechanism in a monolithic silicon device can be very complex. There are many potential internal reasons for a failure, and the final failure may be a secondary result of the primary cause.

Specific Considerations at the PCB Design Level

When a PCB is plugged into a system in which power and other signals are already applied and active, or in a system in which different power sources activate at a different rate, consider three very important issues:

1. **Always connect ground before applying any of the power supply voltages or other signals to the circuit.**

   In a complex integrated circuit that operates from more than one voltage supply, proper operation depends on appropriate polarities and voltage limits being maintained. If ground is not connected before power is applied, internal elements of the silicon device can be exposed to reverse polarity conditions. This can easily cause fault-producing currents in areas that normally are completely isolated from each other. (See previous circuit explanations.)

2. **Current from power supplies may require inrush limiting at the PCB.**

   Integrated circuit devices on PCBs typically have bypass capacitors mounted near the devices to help provide an electrically clean and noise-free environment. On an entire PCB with many IC devices, there may be many capacitors all connected between the power supply busses and ground. The capacitors initially have 0 V and as power is applied to the card, they begin to charge. The charge rate is limited primarily by source impedance of the supplies and impedances across the PCB. In this situation, very high currents can flow for a short time until these capacitances are charged. Because impedances are low and currents are high, during some multiple-supply voltage conditions the voltage buses can charge at different rates, and therefore, create abnormal voltage differences across circuit elements. If this occurs, some of the charging currents actually may pass through the IC devices and the currents can easily exceed the safe operating limits of the connection paths within an IC device, causing marginal or permanent damage. (See previous explanations and refer to VBAT rise time limits specified in data sheets to limit inrush current.)

   To reduce the large current upon card insertion, place an impedance in a series with the supply bus on the PCB, large enough to limit charge currents but small enough not to affect normal operation.

   Also, because unequal capacitance values charge to unbalanced voltages until all transient conditions become equalized, the IC device can be exposed to over-voltage or reverse polarity conditions. This is especially true if one supply bus on the line card begins to charge before another supply bus is connected. In this situation, place a zener diode on the IC side of the supply bus impedance. The zener diode conducts in the forward direction in the case of reverse polarity, and it conducts in the reverse direction to clamp the voltage within safe limits in the case of over-voltage.

3. **Prevent the control pins (C3–C1) from going negative with respect to ground.**

   Zarlink SLIC devices use an active trimming process in which, after the silicon die is installed in the package, the longitudinal balance is trimmed during production testing. The firing internal SCR circuits within the SLIC device perform this trimming process, which then cause a fusing of the trim elements. This process is very similar to the EPROM programming methods. The trim path and the fuse elements are connected between the SLIC device VEE (or VNEG, for a specific SLIC device) and VBAT pins. Pulling the control pins negative towards the VBAT voltage initiates the trimming. During this production step, the VEE current is very carefully controlled so that the fusing action is not destructive. Also, because the control pins normally operate between ground and +5 V, the SCR firing conditions are not seen in the SLIC device's normal operating modes. However, if a transient condition causes any one of the control pins to be pulled negative, its SCR can turn on. In normal line circuit applications, there is no controlled current limiting of VEE, and without this limiting, the resulting current through the SLIC device is destructive. The control pins usually do not see a negative voltage, but during charging transients, and especially if supply buses or grounds are being pulled as the result of capacitive charging, unusual conditions can exist. Plugging in the line card can cause this situation. If ground is not connected for a short time, capacitive charging can pull the +5 V logic negative, and this pulls the control pins negative. Notice that this is a situation difficult to simulate or model and usually occurs only in an actual system, not in an isolated single circuit.

Specific Recommendations for PCB Designs with Zarlink SLIC Devices

Listed below are PCB design guidelines for linecards using the Zarlink SLIC devices. Depending upon the design requirements, apply these recommendations as needed.

- **Apply ground before applying other supply voltages.**

  Zarlink SLIC devices are not intended to be sensitive to the order in which power supply voltages are applied, as long as ground is connected first. A negative voltage that is applied before ground becomes connected can momentarily pull the SLIC device ground pins negative during the charging period of capacitors on the board with unpredictable results. This situation actually causes a condition in which the absolute maximum limits are exceeded. Therefore, the PCB design must utilize a method ensuring grounds are connected before plugging the line card into the backplane. Also, because the internal trimming SCRs are fired through negative voltages

on the SLIC device control leads, C3–C1, the ground/power connection sequencing ensures that the positive and ground references are established on the SLIC device before any negative supplies are connected.

If the PCB uses card edge fingers that plug into a socket, make the critical path signal finger traces of different lengths. For some types of modular plugs and sockets, pins of different lengths can be specified. With several different lengths, you can select the order of electrical connection every time the board is plugged in. Typically, ground is connected with the longest pin(s); power is connected with the next shorter pins; and possibly even shorter pins are used for the remaining signals (see Figure 1). Figure 1 shows redundant grounds placed on opposite ends of the edge connector. Because there is almost invariably an angular tilting action between the card edge and its mating connector, placing a ground at either end helps ensure that ground is first connected during the insertion process.

If there is no mechanical solution to guarantee the order of pin connections, include alternate means of power connection on the line card. One design method that ensures ground is always applied before negative voltages are connected uses a MOSFET circuit, or even a 5 V relay to switch on the negative supply voltages. A relay, powered between the +5 V (VCC) supply and ground does not energize until its coil power, including ground, is available. This ensures that ground is connected before the relay is energized. The contacts of the relay then switch on the –5 V VEE (or VNEG, if so connected) and –48 V (battery) supplies, only after the relay is energized and ground is applied. This relay scheme does not eliminate any effects from +5 V being applied before ground is applied, but this typically is not an issue. The major concern is a negative voltage being applied before ground.

■ **Provide current limiting to the –5 V (VEE) supply at the PCB level.**

The capacitor connected to the VBAT pin initially is charged to 0 volts before the line card is plugged in. If –5 V (VEE) is applied before battery is applied, then the VEE supply may attempt to charge the VBAT capacitor through the SLIC device substrate. This charging path is shown in Figure 2. The impedance of this path is low, and if the board and supply impedances also are low, this may cause high enough currents within the SLIC device to cause internal damage. A 2 Ω resistor connected between the VEE supply and the VEE connections of all SLIC devices, or a 10 Ω resistor, if used for each SLIC device on the board, should limit the current to a safe level. There can even be a second shorter finger that shorts the resistor when the card is fully inserted, as shown in Figure 1. Noise can be reduced by adding a filter capacitor to ground on the SLIC device side of this resistor.

■ **Add a zener diode (6 to 7 V) between the SLIC device VEE supply and ground.**

When power is first applied, transient charging currents can cause the VEE bus to be pulled outside of its safe limits. This zener diode conducts in the forward direction to eliminate the SLIC device VEE pin going positive, and conducts in the reverse (zener) direction to limit the VEE supply from becoming too large at the SLIC device. Place the diode on the SLIC device side of the resistor. Figure 3 shows how to connect the zener.

■ **Provide current limiting to the –48 V (battery) supply at the PCB level.**

On SLIC devices, the rate at which the VBAT voltage rises must be limited (see the data sheet) to prohibit excessive current from charging the QBAT capacitor. The QBAT charging path is internal within the SLIC device and has a maximum safe charging current. On SLIC devices that do not have the switching regulator (and also do not have a QBAT pin), the rate at which the VBAT voltage rises is not as limited. However, due to possible dv/dt conditions and effects from those conditions, such as firing of SCRs within the SLIC device, include charging rate limits on all designs using SLIC devices. A 1 Ω resistor connected in series with the battery supply line should effectively provide the current limiting necessary. A capacitor on the SLIC device side of this resistor forms a time constant that helps limit the rise time.

■ **Ensure that all SLIC device grounds (BGND, AGND, and DGND) do not have a voltage difference between them that exceeds the specified data sheet limits (BGND with respect to AGND/DGND: +3 V to –3 V).**

The Zarlink SLIC devices have more than one ground connection on the device. The BGND connection is the ground reference for the battery voltages and signals that are referenced to the tip/ring circuits. The AGND and BGND connections serve as references for low voltage circuits. While grounds usually are considered to be at the same potential, separate system distribution and routing typically is done to avoid ground loops or other impairments. The SLIC devices have an absolute maximum specified limit (see the data sheets) to the voltage difference that can exist across the ground connections. If this limit is exceeded, device damage can result. For grounds connected together on a PCB, this is usually not a concern. However, if the grounds are wired to different pins on the card edge connector, it is possible for one of the grounds to make contact before the other, causing the maximum limits to be exceeded. If system performance considerations require the grounds to be

separated, a pair of back-to-back diodes placed across the grounds to limit voltage differences at card plug-in time is one possible solution.

Summary

Monolithic SLIC devices are designed to operate in an environment of different voltage ranges, all existing on a common piece of monolithic silicon that has been designed to reliably accommodate them. While all possible application designs cannot be covered in this single document, appropriate design considerations to help ensure the robustness and reliability of designs using Zarlink SLIC devices are provided. As in all design methodology, a thorough analysis of the specific line circuit design and understanding of each specific device's data sheet requirements is warranted.

Figure 1. The Use of Different Length Fingers

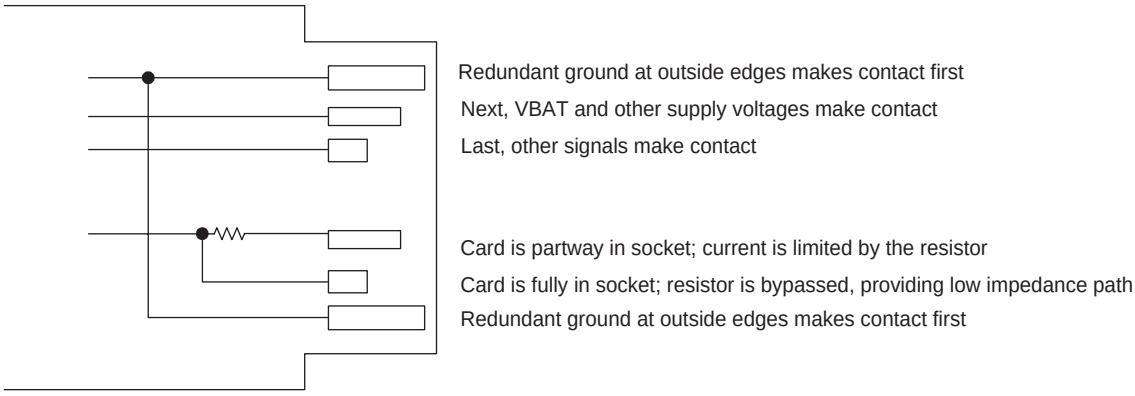


Figure 2. VEE to VBAT Path through Substrate

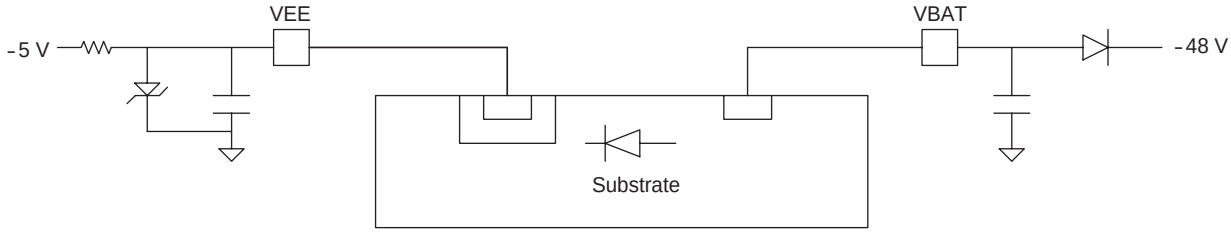
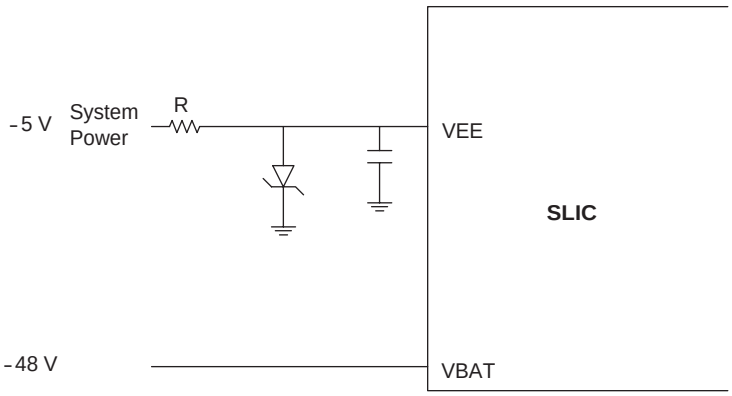


Figure 3. The Use of a Zener Diode on VE



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