



SLIC Devices

Applications of the Zarlink SLIC Devices

Longitudinal Balance of Zarlink Subscriber Line Interface Circuits (SLICs)

Application Note

APPLICATION NOTE

The purpose of this application note is to show the user how to predict the worst-case longitudinal balance, which can be expected in an application using most Zarlink SLIC devices (ASLIC and ISLIC™ devices are not affected due to their architecture). This document presents graphs of data that show the worst-case performance for various conditions for CCITT and North American systems. The “Internal SLIC Device Model” section on page 7 presents the circuit models and equations used to obtain the graphs so that any special conditions or additional simulations can be performed to predict either the longitudinal to transverse (L-T) balance, or the longitudinal to four-wire (L-4) balance of an application using a Zarlink SLIC device.

The longitudinal balance of an application circuit using the SLIC device will not be exactly the same as the SLIC device longitudinal balance listed on the data sheet. There are two reasons for this: (1) errors in the components around the SLIC device will add to the error in the integrated circuit, and (2) the circuit configuration in a linecard will usually be different from the component test circuit.

The circuit model presented is accurate in or near the audio band and could even be used for modeling transmission parameters; although for that purpose, a simpler unbalanced model would suffice. The circuit model is also applicable to longitudinal generation, but no longitudinal generation results are presented.

BACKGROUND

Longitudinal balance measures how well a telephone line circuit rejects longitudinal (i.e., common mode) signals. Because telephone wire pairs are twisted, it is difficult for noise sources to induce noise between the wires. However, it is very easy for noise sources to induce common mode noise equally on both wires relative to earth ground (i.e., longitudinally). If the line circuit is balanced relative to earth, this longitudinal noise has no effect and the telephone users cannot hear it; however, any imbalance in the line circuit will transform some of the longitudinal signal into a transverse signal between the wires (metallic signals) and into a signal at the four-wire output of the line interface circuit. The transverse (metallic) signal is audible to the near-end user. The four-wire signal is audible to the far-end user. Longitudinal balance is important, because the earth ground path is inherently very noisy.

Also, the telephone wire pair is typically packed into a cable with many other wire pairs for a considerable distance and it can pick up longitudinal noise from the other wire pairs.

There are two longitudinal balance test methods in general use: 1) a CCITT method described in the Blue Book's Recommendation O.121; and 2) a North American method described in ANSI/IEEE Standard 455-1985. In most cases, the two methods will give almost the same results. The CCITT method is implemented by the Wandel & Goltermann PCM-4 PCM Channel Measuring Set. The North American method is implemented by the Wilcom T207 Longitudinal Balance Test Set. Zarlink tests its SLIC devices in the factory with the ANSI/IEEE method; however, for many SLIC devices, Legerity changes the tester impedance per leg from 370 Ω to 300 Ω (see the SLIC data sheets).

In North America, the main longitudinal balance specifications are in Bellcore document number FR-000064 (LSSGR) for central office equipment or EIA/TIA document number 464-A for PBX equipment. In general, North America has the most stringent requirements on this specification. A primary CCITT specification for longitudinal conversion loss (the CCITT term for longitudinal balance) is given in Recommendation Q.552.

GRAPHS FOR COMMON SETUPS

The most important parameters affecting the application circuit's longitudinal balance are the balance of the SLIC IC and the error in the fuse resistors. Therefore, the device specification balance (see the SLIC data sheets) of the SLIC IC is used as the horizontal axis of the graphs, and the fuse resistor error per leg in ohms is used to parameterize the curves on the graphs.

For all of the graphs here, the source impedance (Z_S) for application testing is assumed to be the same as for component testing, either $Z_S = 300 \Omega$ or $Z_S = 370 \Omega$. If this is not true, the data sheet balance must be adjusted by the difference in component test setup constants. If the application uses $Z_S = 300 \Omega$ and the component was specified with $Z_{SC} = 370 \Omega$, add 0.94 dB to the data sheet balance. If the application uses $Z_S = 370 \Omega$ and the component was specified with $Z_{SC} = 300 \Omega$, subtract 0.94 dB from the data sheet balance. Consult the SLIC data sheets for component test conditions.

The values of application fuse resistors (R_f) used in the graphs are either 20 Ω or 50 Ω .

The values of programmed SLIC application impedance (Z_{mx}) used in the graphs are: 560 Ω for a 600 Ω SLIC device with 20 Ω fuses; 500 Ω for a 600 Ω SLIC device with 50 Ω fuses; 860 Ω for a 900 Ω SLIC device with 20 Ω fuses; and 800 Ω for a 900 Ω SLIC device with 50 Ω fuses.

The line filter capacitors, C_{AX} and C_{BX} , are assumed to be perfect, so that $C_e = 0$.

The application tester is assumed to have 90 dB balance ($\epsilon_s = 32$ ppm) for all of the graphs in this document.

The same value of SLIC longitudinal impedance ($Z_{lx} = 25 \Omega$) is used for all of the graphs, because balance is not very sensitive to this parameter.

Figure 1. Graphs for 600 Ω CCITT Applications

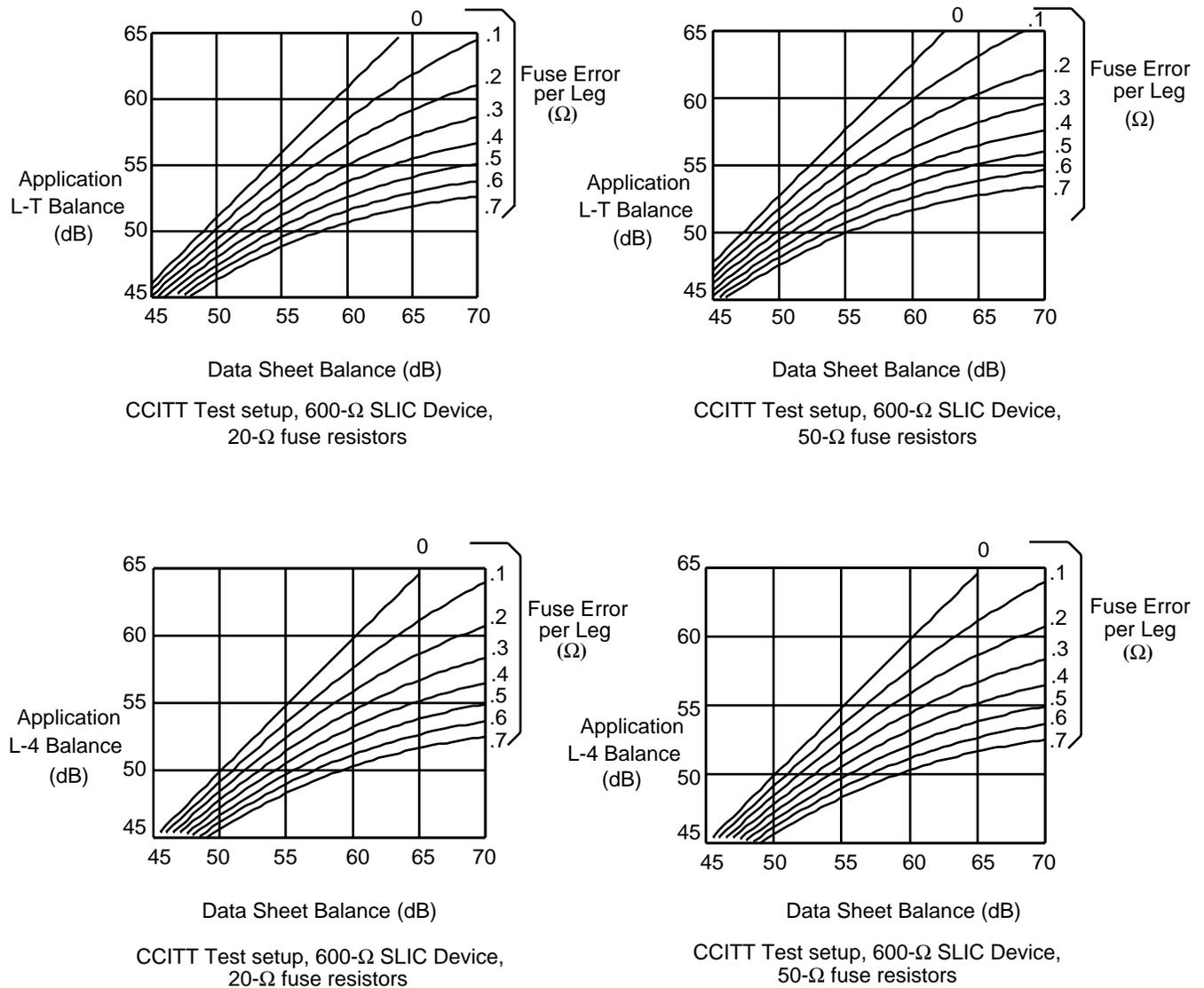
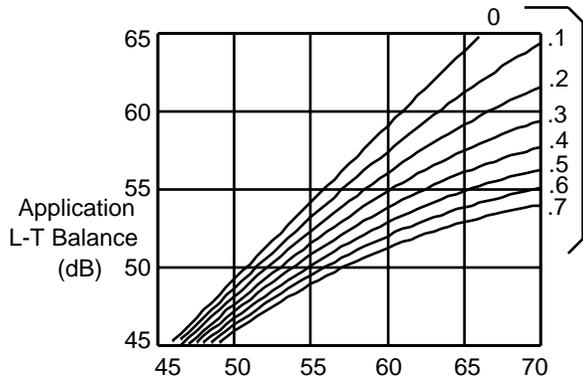
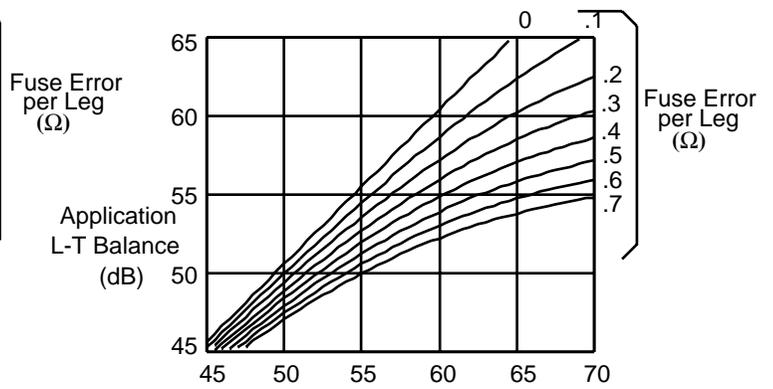


Figure 2. Graphs for 900 Ω CCITT Applications



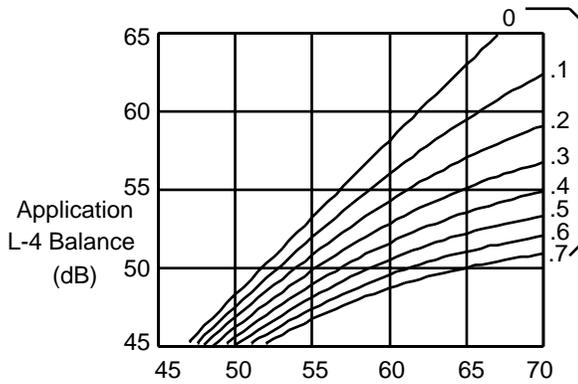
Data Sheet Balance (dB)

CCITT Test setup, 900-Ω SLIC Device,
20-Ω fuse resistors



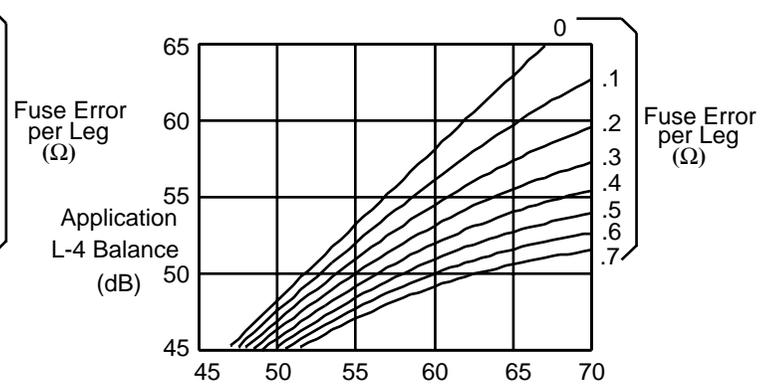
Data Sheet Balance (dB)

CCITT Test setup, 900-Ω SLIC Device,
50-Ω fuse resistors



Data Sheet Balance (dB)

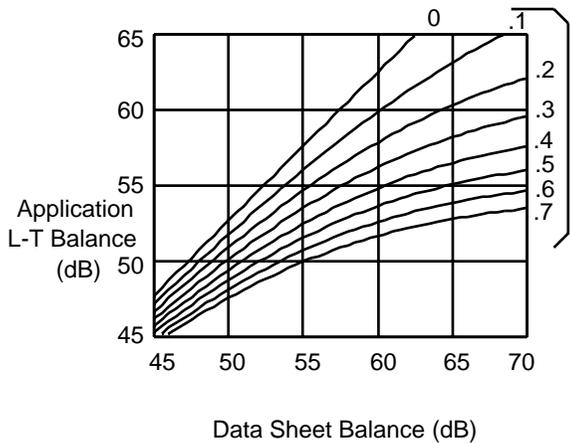
CCITT Test setup, 900-Ω SLIC Device,
20-Ω fuse resistors



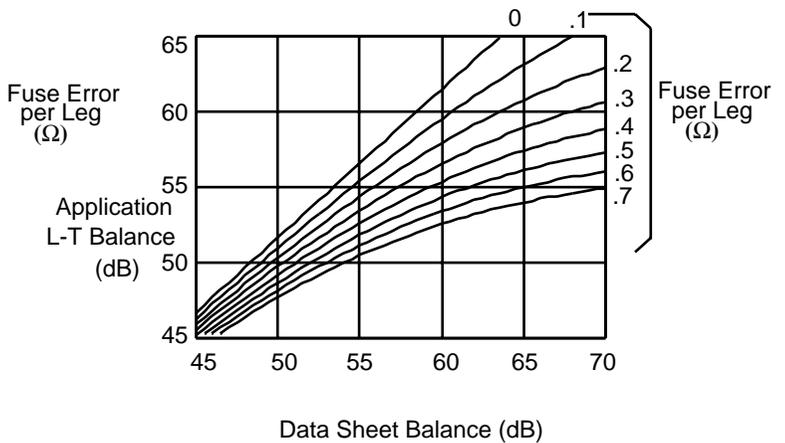
Data Sheet Balance (dB)

CCITT Test setup, 900-Ω SLIC Device,
50-Ω fuse resistors

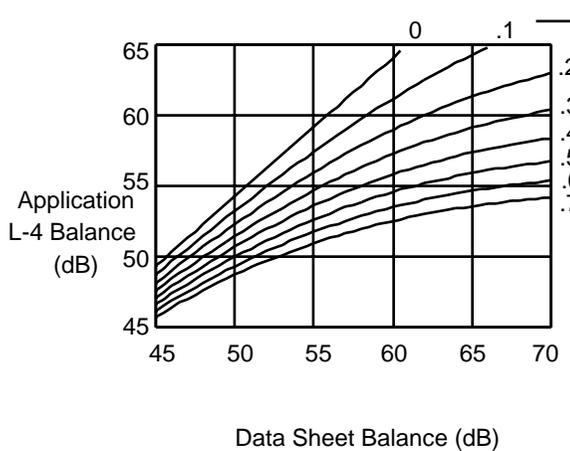
Figure 3. Graphs for 600 Ω North American Applications



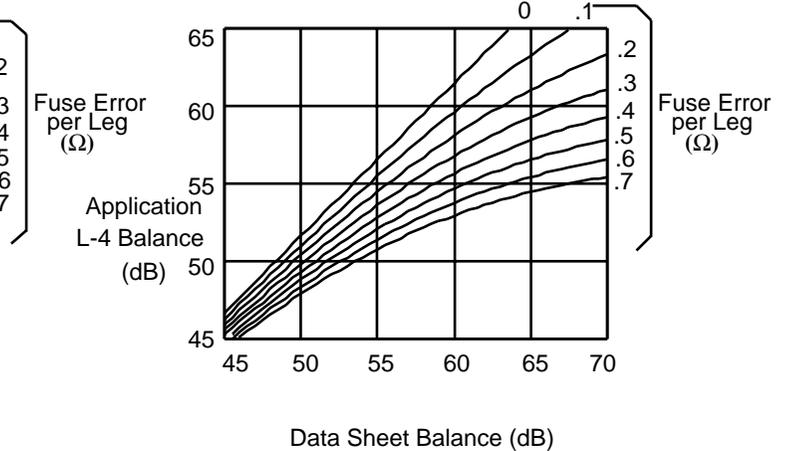
North American Test setup, 600-Ω SLIC Device,
20-Ω fuse resistors



North American Test setup, 600-Ω SLIC Device,
50-Ω fuse resistors

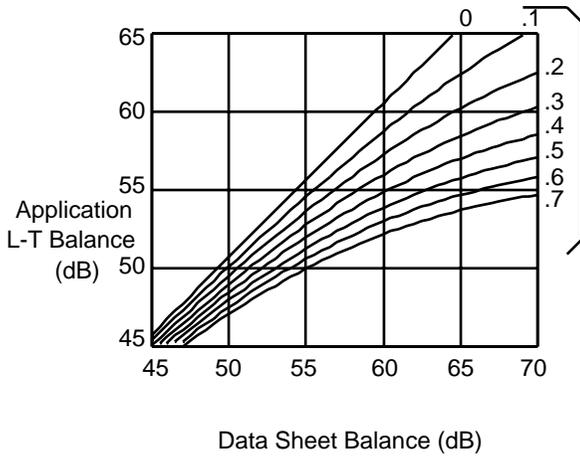


North American Test setup, 600-Ω SLIC Device,
20-Ω fuse resistors

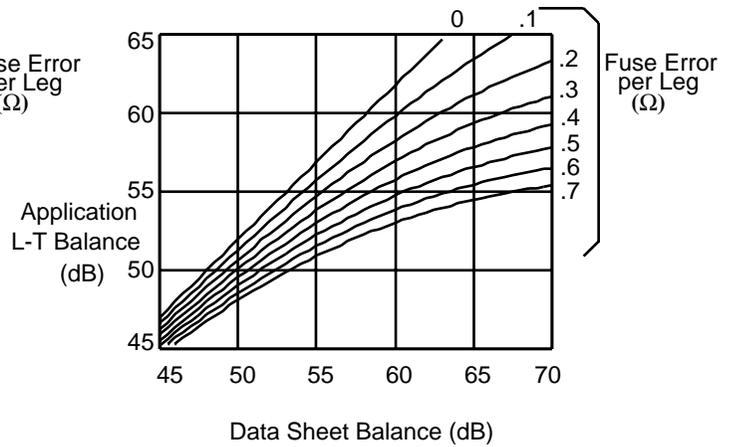


North American Test setup, 600-Ω SLIC Device,
50-Ω fuse resistors

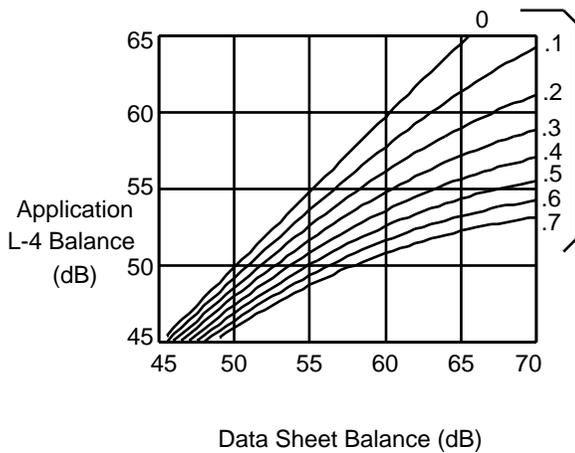
Figure 4. Graphs for 900 Ω North American Applications



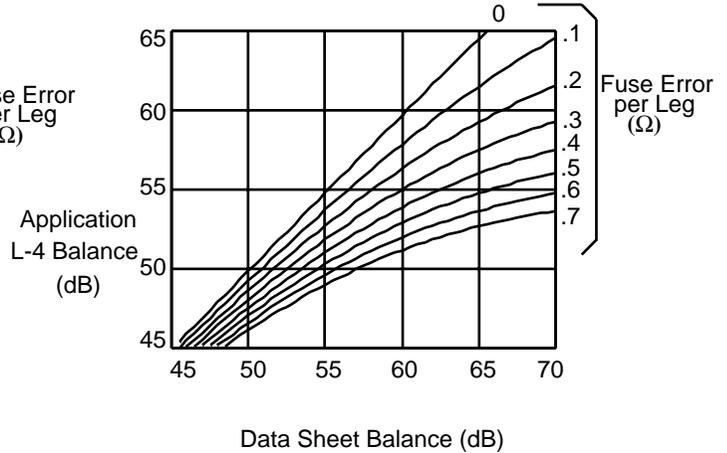
North American Test setup, 900-Ω SLIC Device,
20-Ω fuse resistors



North American Test setup, 900-Ω SLIC Device,
50-Ω fuse resistors



North American Test setup, 900-Ω SLIC Device,
20-Ω fuse resistors



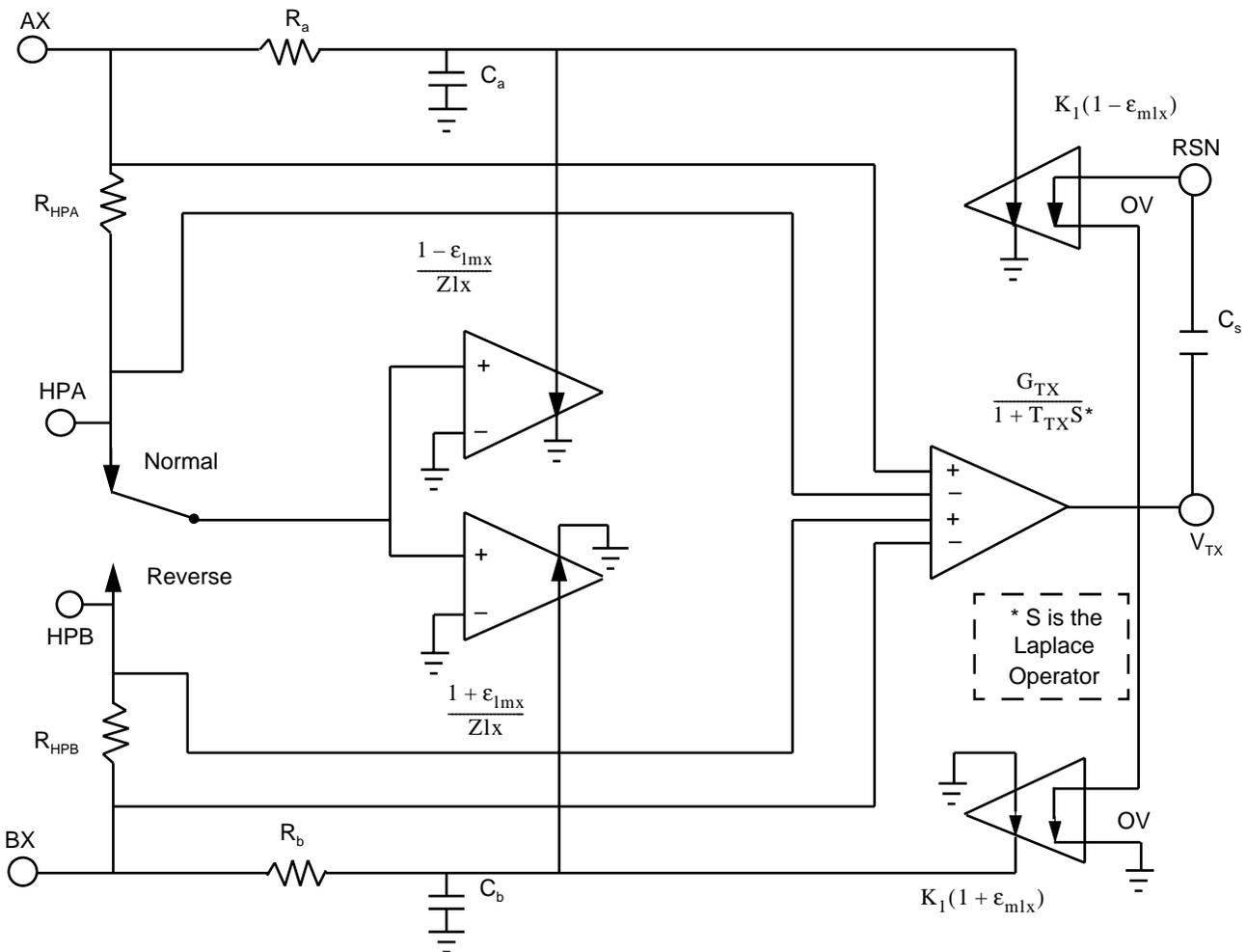
North American Test setup, 900-Ω SLIC Device,
50-Ω fuse resistors

INTERNAL SLIC DEVICE MODEL

This section explains the internal model of the Legerity SLIC device, which is used throughout this document, (see Figure 5). By entering this model and the external circuits into a circuit simulation program such as SPICE, it should be possible to duplicate the results in this document. Please note that the longitudinal-to-four-wire balance has been divided by the transmit gain of the SLIC device in the formula.

While longitudinal generation is not covered in this document, it is possible to use the chip model to simulate longitudinal generation test circuits. The longitudinal voltage is sensed from HPA or HPB rather than their average because of the Legerity SLIC device's unbalanced DC feed. While this makes no difference to the longitudinal balance, it has a dramatic impact on longitudinal generation at low frequencies.

Figure 5. Internal Legerity SLIC AC Model



Internal SLIC Parameters

Note that some of these parameters need not be included in the longitudinal balance model, but they are included here so that the model can also be used for simulation of transmission parameters.

Amplifier Capacitance — C_a , C_b , C_s

C_a and C_b are well balanced and have not been included in the balance equations. For transmission modeling, C_a and C_b should be assumed to be 18 nF each. The stray capacitance, C_s , is 2.5 pF.

Longitudinal to Metallic Current Coupling — ϵ_{lmx}

ϵ_{lmx} is the longitudinal to metallic current coupling per leg of the SLIC device. This coupling is a parasitic effect caused by amplifier gain mismatch. Its effect is almost entirely on the longitudinal balance and not on the longitudinal generation.

Metallic to Longitudinal Current Coupling — ϵ_{mlx}

ϵ_{mlx} is the metallic to longitudinal current coupling per leg of the SLIC device. This coupling is a parasitic effect caused by amplifier gain mismatch. Its effect is almost entirely on the longitudinal generation and not on the longitudinal balance.

Transmit Gain — G_{TX}

G_{TX} is the audio band voltage gain from the two-wire terminals of the SLIC device (V_{abx}) to its four-wire transmit output (V_{TX}). Most parts have unity gain, but metering parts have lower gain. (Consult the SLIC data sheets.)

Current Gain — K_1

K_1 is the current gain from the RSN input to the metallic line circuit. K_1 typically varies from 200 to 1000 depending on SLIC device type. (Consult the SLIC data sheets.)

Amplifier Series Resistance — R_a, R_b

R_a and R_b have very little effect on balance because they are inside a feedback loop; therefore, they have not been included in the balance equations. In a very accurate transmission model, R_a and R_b should be assumed to be 18Ω each.

Loop Filter Resistors — R_{HPA}, R_{HPB}

R_{HPA} and R_{HPB} combine with the external filter capacitor, CHP, to separate the audio and DC-feed circuits. They are approximately $212\text{ k}\Omega$ each. They have almost no effect on longitudinal balance; however, their size and matching affect longitudinal generation strongly.

Transmit Amplifier Time Constant — T_{TX}

The transmit amplifier behaves as a single pole low-pass filter with a time constant of $T_{TX} = 455\text{ ns}$. This time constant has little effect on balance and was not included in the equations; however, it would be needed in an accurate transmission model.

Longitudinal Impedance Per Leg — Z_{lx}

Z_{lx} is SLIC longitudinal impedance per leg in ohms. It is assumed to be $25\ \Omega$ in the calculations, but few of the calculations are very sensitive to its value.

APPLICATION CIRCUIT CONNECTED TO A TESTER

This section discusses a typical application circuit connected to a longitudinal balance tester (as shown in Figure 6) such as the Wilcom T207 test set. Figure 7 shows an idealized diagram of the metallic circuit with the error terms incorporated in order to allow better understanding of the equations. In this document, an “x” in a symbol usually means that the parameter refers directly to the chip without fuse resistors or line filter capacitors; thus, Z_{mx} is the metallic impedance of the SLIC device without fuses or filter capacitors.

Circuit Model

The application circuit is shown connected to a longitudinal test circuit in Figure 6. This diagram shows the location of important components and error terms.

Application Parameters**Line Filter Capacitance Error Per Leg — C_e**

C_e is the maximum application line filter capacitance error per leg (deviation of one capacitor from the mean of the two capacitors).

Line Filter Capacitance — C_x

C_x is the capacitance of C_{AX} and C_{BX} , which are the EMI-filter capacitors connected from AX and BX to ground. The common part of the two capacitors causes a negligible effect and can be ignored.

Loop Filter Capacitor — C_{HP}

C_{HP} is the capacitor that separates the audio band from the DC feed.

Test Source Impedance Fractional Error Per Leg — ϵ_s

ϵ_s is the maximum difference between the application test source impedances divided by the sum of those impedances.

Frequency — F

F is the measurement frequency.

Longitudinal to Transverse Balance — L-T

L-T is the longitudinal to transverse balance of the circuit. It is defined as:

$$L-T = -20 \log|V_{ab}/E_0|$$

Longitudinal to Four-Wire Balance — L-4

L-4 is the longitudinal to four-wire balance of the circuit (normalized to unity transmit gain). It is defined as:

$$L-4 = -20 \log|V_{TX}/E_0| + 20 \log|G_{TX} Z_{mx} / (Z_{mx} + 2R_f)|$$

Fuse Resistance Error Per Leg — R_e

R_e is the maximum application fuse resistance error per leg in ohms (deviation of one fuse resistor from the mean of the two fuse resistors).

Fuse Resistance Per Leg — R_f

R_f is the application fuse resistance per leg in ohms, including any other components in series with the fuses (such as switch contacts). While R_f is only resistive in this document, it could also be complex in some cases, for example if filter inductors were included.

SLIC Metallic Impedance Excluding Fuses — Z_{mx}

Z_{mx} is the metallic impedance in ohms programmed into the SLIC application circuit, excluding fuses and line filter capacitors, $Z_{mx} = (Z_T / (K_1 G_{TX}))$. The SLIC device also places an effective capacitance of a few nF in parallel with Z_{mx} , but this makes little difference to the balance and has been ignored.

Receive Impedance — Z_{RX}

Z_{RX} is used to program the SLIC receive gain.

Transversal Impedance — Z_T

Z_T is used to program the SLIC transverse (metallic) impedance.

Test Source Impedance Per Leg — Z_s

Z_s is the application test source impedance per leg in ohms. Two common values are in use: 300 Ω and 370 Ω .

Simplified Metallic Circuit

A very simplified diagram of the metallic circuit is shown in Figure 7 for the application setup. The error voltages arise from the interaction of the longitudinal currents with the imperfections in the circuit. All of the error voltages are proportional to the longitudinal current per leg (I_l). The symbol, $\epsilon_{l_{mx}}$, represents the longitudinal to metallic current coupling of the SLIC device, which is the primary chip contribution to longitudinal imbalance.

Figure 6. Application Circuit Connected to a Tester

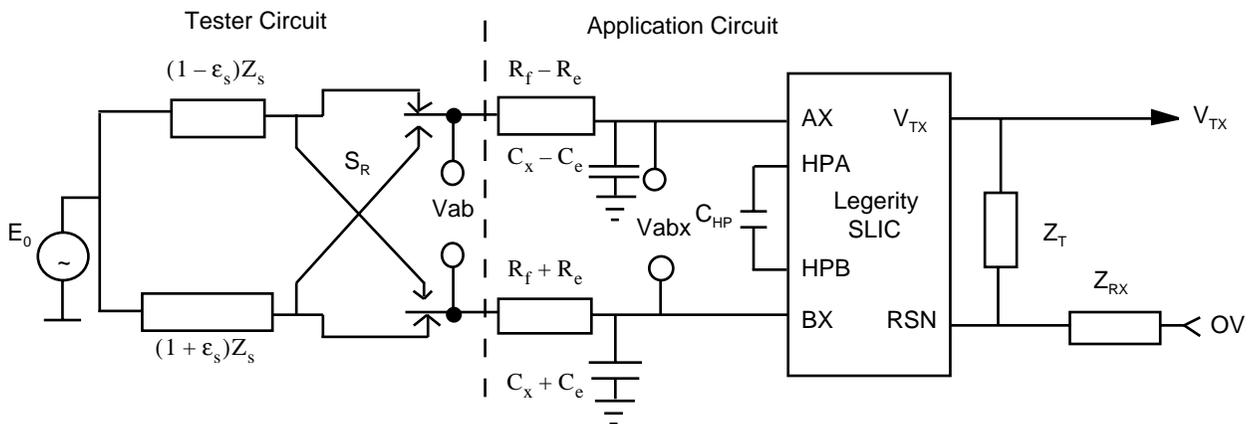
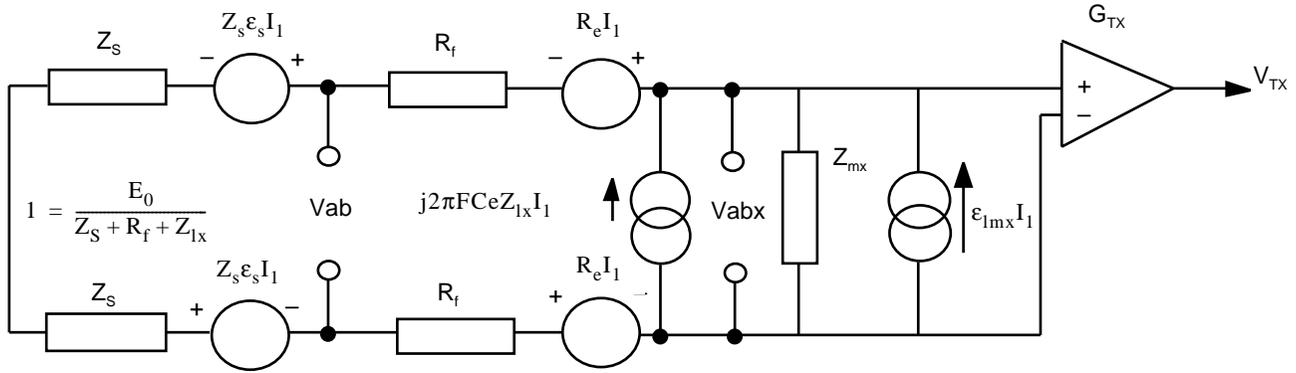


Figure 7. Simplified Metallic Circuit



Longitudinal Balance Equations

The longitudinal balance equations are too long to fit easily on a normal size page; therefore, in order to simplify the longitudinal balance equations, we will define test setup constants first. The test setup constant is the difference in dB between the measured balance and the actual internal balance of the chip if the test setup had perfect resistors and capacitors.

L-T Application Test Setup Constant (C)

$$C = -20 \cdot \log \left| \frac{2Z_s \cdot Z_{mx}}{(2Z_s + 2R_f + Z_{mx}) \cdot (Z_s + R_f + Z_{1x})} \right| \text{dB}$$

L-4 Application Test Setup Constant (D)

$$D = -20 \cdot \log \left| \frac{2(Z_s + R_f) \cdot (Z_{mx} + 2R_f)}{(2Z_s + 2R_f + Z_{mx}) \cdot (Z_s + R_f + Z_{1x})} \right| \text{dB}$$

L-T and L-4 Component Test Setup Constant (Cc)

$C_c = +0.70$ dB for a 300Ω component test setup.

$C_c = -0.24$ dB for a 370Ω component test setup.

The balance equations below use the test setup constants and parameters defined previously. They are written as functions of the balance (B) guaranteed on the applicable data sheet, which is used as the independent variable in the preceding graphs. The worst-case can be obtained by assuming that the real and imaginary parts of each term are positive, so that there is no cancellation.

Application L-4 Balance Function

$$L4 = D - 20 \cdot \log \left| 10^{-\frac{B - C_c}{20 \text{ dB}}} - \frac{R_e}{Z_s + R_f} + j2\pi F \cdot C_e \cdot Z_{1x} + \frac{Z_s}{Z_s + R_f} \epsilon_s \right| \text{dB}$$

Application L-T Balance Function

$$LT = C - 20 \cdot \log \left| 10^{-\frac{B - C_c}{20 \text{ dB}}} - \frac{2R_e}{Z_{mx}} + j2\pi F \cdot C_e \cdot Z_{1x} + \frac{Z_{mx} + 2R_f}{Z_{mx}} \epsilon_s \right| \text{dB}$$



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