
Abstract:

This application note discusses the need for protection and presents ways to minimize stresses on the LCAS device. The LCAS has built-in protection but requires external protection circuitry to limit excessive voltages, currents, and transients into the LCAS, which is critical for reliable LCAS operation. Component suggestions are provided, however the system integrator should validate any protection scheme before committing a design to mass production or field deployment.

1.0 LCAS DEVICES

This application note applies to the Le75181, Le75183, and Le75282 Line Card Access Switch devices. The Le75181 device provides ringing access and break switch functionality. The Le75183 device provides test out, test in, ringing test, ringing access, and break switch functionality. The Le75282 provides test, ringing access, and break switch functionality. The Le75181 and Le75183 have several suffix variations which define state control and integrated protection; the Le75282 is a dual LCAS device. All devices are simply referred to as LCAS devices throughout this document. Refer to the respective LCAS data sheets for more information.

2.0 ELECTRICAL ENVIRONMENT

Figure 1 illustrates the environment in which the LCAS must operate.

On the line connection of the LCAS, over-voltage can occur in longitudinal mode where both conductors (A/Tip and B/Ring) are exposed to the hazard in the same manner. Also possible are metallic applications of hazardous voltage inserted between the two conductors. A longitudinal surge can also become a metallic surge if the primary or secondary over-voltage protector present on one lead triggers before the over-voltage protector of the other lead.

Lightning disturbances are a common source of over-voltage stress. In addition, since telephone cables often share space with ac utility power cables, electromagnetic coupling from a power system can produce power induction or a ground potential rise which can result in a longitudinal over-voltage in the telephone cabling. Also power lines can make direct electrical contact (power cross) with the telephone conductors.

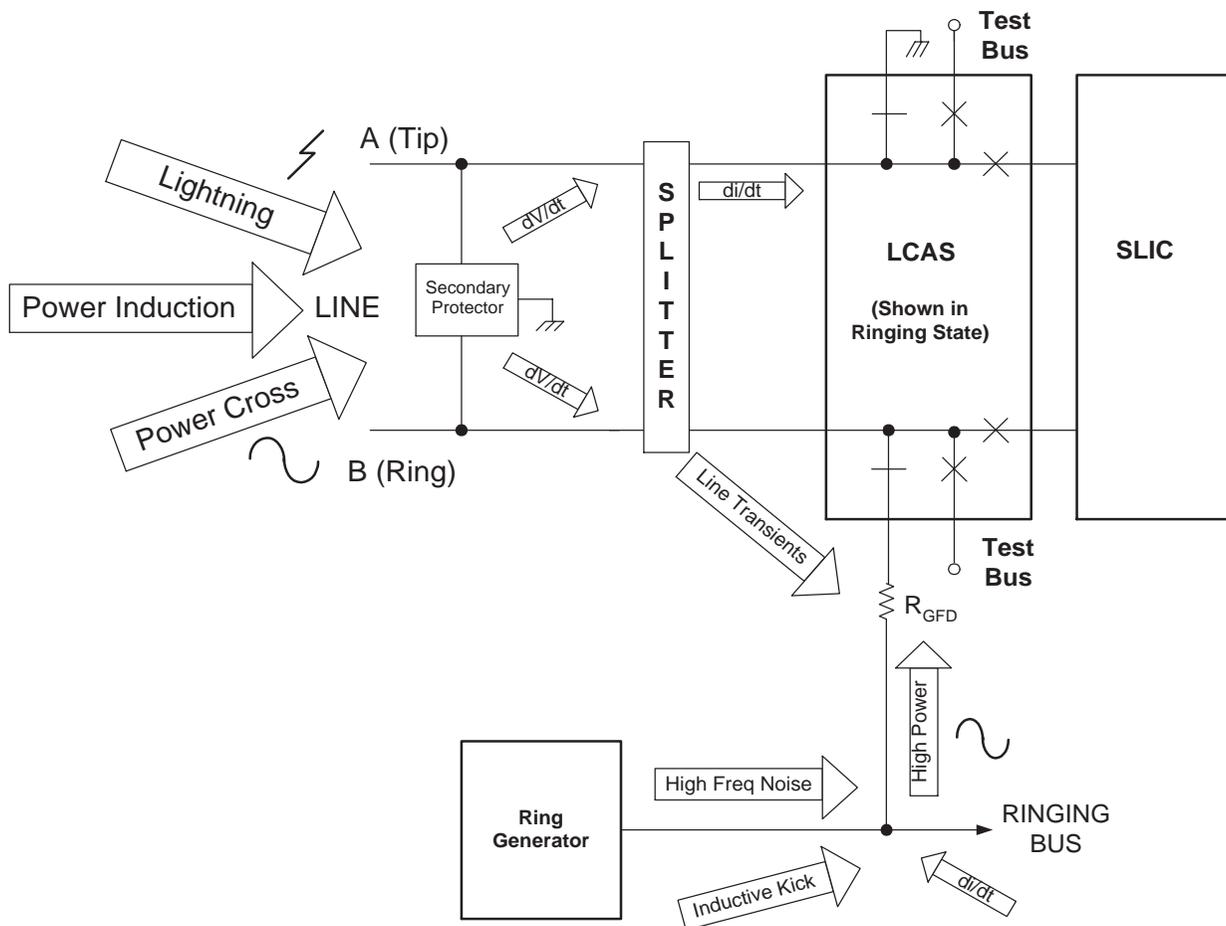
The first level of protection are the primary protectors that typically reside in the main distribution frame. Secondary protection must be deployed on the line card to deal with residual and sneak-under voltages and fault currents from the primary protector, as defined in standards such as Telcordia GR-1089 and ITU-T Recommendation K.20/21/45. Another concern is that the secondary protector itself subjects the LCAS to high voltage dv/dt transients when it turns on and crowbars.

There are additional concerns associated with the ring generator connection to the LCAS. The ring generator can subject the LCAS to high frequency switching noise. Inductive kicks from the ringing signal can generate excessive voltage spikes and switching ringing signals on and off can generate di/dt's on the ringing bus. Also transients from the line side can be passed through to the ring feed resistor and ringing bus.

In IVD environments where POTS splitters reside on the telephone line, the POTS splitters can generate a di/dt kickback into the LCAS.

The need for protection against severe electrical stresses becomes clear. The LCAS must be protected from over-voltage, excessive current, and fast transients.

Figure 1. LCAS Electrical Environment



3.0 LINE SIDE SECONDARY PROTECTION

Line card designs require secondary protection against damage from lightning and power cross situations. Even intra-building deployments should be protected to increase robustness and minimize field returns. External secondary protection components are required; these are discussed in Section 4.

As part of the overall protection scheme, to protect the LCAS and subsequent SLIC circuitry from over-voltage and over-current fault situations, the LCAS provides internal tertiary protection.

3.1 Integrated Protection

Integrated protection is provided by a combination of the current-limiting and current-foldback feature of the LCAS, the thermal shutdown mechanism, the All Off state, and a diode bridge voltage clamp circuit. In addition, the Le75181 and Le75183 offer a battery referenced crowbar SCR option.

3.1.1 Current-Limit Feature

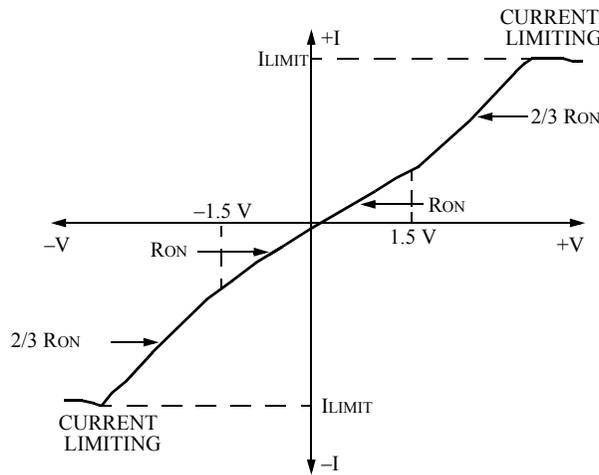
Utilized on: Le75181 - Tip Break Switch & Power Ring Return Switch

Le75183 - Tip Break Switch, Power Ring Return Switch, & Test Out Switches

Le75282 - Test Access Switches

The current-limiting feature (Figure 2) limits the current through the switch during fault conditions. For normal operation, the switch will operate in the region labeled as R_{ON} . As current increases, R_{ON} decreases by 2/3 and beyond that current-limiting occurs. This feature prevents excess current damage to the LCAS and reduces the fault current that the integrated diode bridge/SCR or diode bridge must shunt away from the SLIC.

Figure 2. DC Current-Limiting Characteristic



3.1.2 Current-Foldback Feature

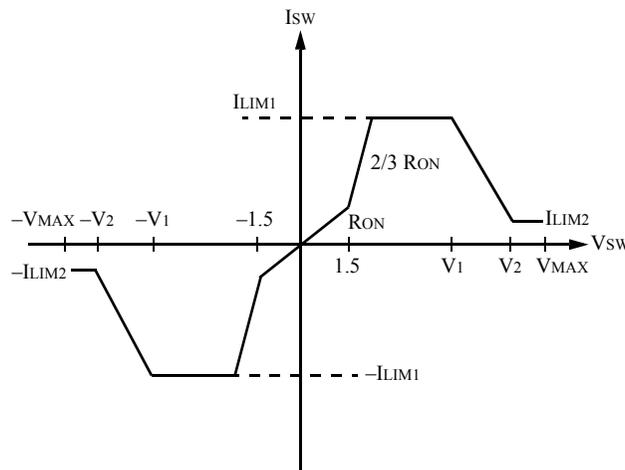
Utilized on: Le75181 - Ring Break Switch

Le75183 - Ring Break Switch

Le75282 - Break Switches & Power Ring Return Switch

A switch with current-foldback (Figure 3) operates like the current-limiting switch up to the current-limit region. In current-limiting, as voltage increases across the device, the switch crowbars into a second lower current region of operation. The reason for the crowbar feature is to reduce power through the switch during a fault condition. This allows for higher secondary protector trigger voltages, such as may be required in an IVD application.

Figure 3. DC Current-Foldback Characteristic



3.1.3 Thermal Shutdown Feature

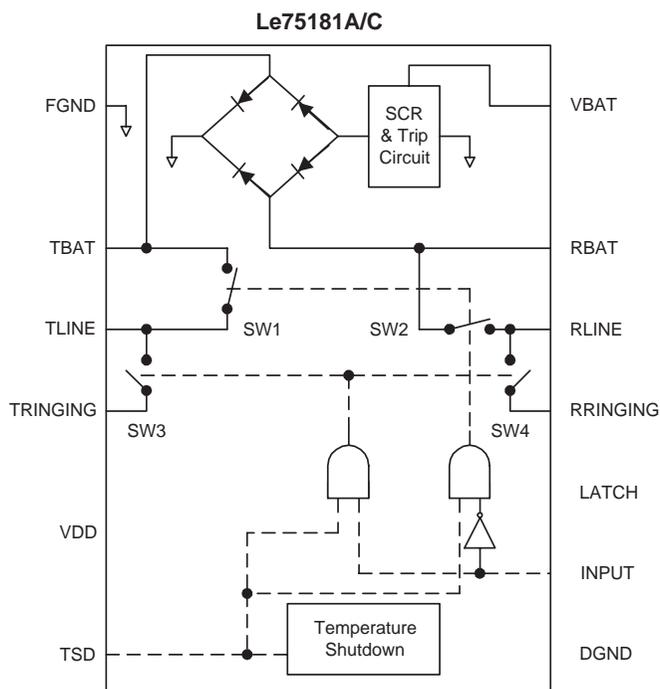
The thermal shutdown feature offers protection to the LCAS and subsequent circuitry from damage due to thermal heating from excess power dissipation, as may be experienced during extended power cross events. Due to the relatively short duration of lightning events, the thermal shutdown mechanism will not activate during lightning.

3.1.4 Integrated Over-voltage Protection Circuitry

In any line card design, the voltage seen at the inputs to the SLIC must be clamped below the maximum rating of that device. This is typically in the range of $60 V - 80 V$. Additionally, fault current must be shunted away from the SLIC input to ground, or, in some cases, this current may also be directed to battery.

The LCAS offers integrated over-voltage clamping circuitry. Over-voltage protection is provided by a diode bridge/SCR clamping circuit or simply by a diode bridge/SCR clamping circuit. See Figure 4 for an example of the diode bridge/SCR clamping circuit.

Figure 4. Le75181A/C LCAS – Diode Bridge and SCR Circuitry



3.1.4.1 Operation During Lightning Disturbances

During a positive lightning event, fault current is directed to ground via steering diodes in the diode bridge. Voltage at the SLIC input is clamped to a diode drop above ground. For this clamping to be effective, the LCAS FGND pin must be closely connected to the SLIC BGND pin.

During a negative lightning event, negative lightning is directed to battery via steering diodes in the diode bridge. In the SCR version, negative lightning causes the SCR to conduct and fault currents are directed to ground via the SCR and steering diodes in the diode bridge. Note that for the SCR to foldback or crowbar, the current pulled from the VBAT rail must exceed the SCR gate trigger current and the current drawn after turn ON must exceed the holding current. A capacitor is located on the VBAT pin and provides the gate trigger current under a fast rising lightning surge.

During a lightning event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dynamic current-limit response of the break switches (assuming idle/talk state). In the case of lightning (or a high voltage dv/dt), the current-limit circuitry will force the break switches into an off state. When the voltage seen at the line nodes of the LCAS is properly clamped by an external secondary protector, upon application of a 1000 V, 10 x 1000 pulse (Telcordia lightning), the current through the break switch will typically be a pulse of magnitude 2 A – 2.5 A and of a duration less than 0.5 μ s. The key in choosing between the SCR or no SCR version of the LCAS device is if the battery supply is designed so that it can stand a pulse of this order. The key parameter is the input capacitance. The equation is:

$$i = C \, dv/dt$$

Where $i = 2.5 \text{ A}$, $dt = 0.5 \mu\text{s}$, $C =$ input capacitance of the power supply, and $dv =$ the change on the battery created by dumping 2.5 A for 0.5 μ s. Given the specific input capacitance of the supply, will the dv created have any negative impact?

3.1.4.2 Operation Under Power Cross Situations

For power cross and power induction faults, in both versions, the positive cycle of the residual fault is clamped to a diode drop above ground and fault currents steered to ground. As previously discussed, the battery rail must provide

the SCR gate trigger current in order for the SCR to crowbar. Considering the slow rise time of an AC fault, the VBAT capacitor will not be sufficient to provide that current and the battery rail must be capable of sourcing it. Otherwise, the battery rail may be pulled more negative by the external surge until the SLIC breakdown voltage is exceeded. A zener diode located on the battery rail can be used to protect the SLIC against such condition and will provide the gate current required by the LCAS SCR. In the SCR version, the negative cycle will cause the SCR to trigger when the voltage exceeds the battery reference voltage by two to four volts. When the SCR triggers, fault current is steered to ground. In the non-SCR version, the negative cycle of the power cross is steered to battery.

During a power cross event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the DC current-limit response of the break switches (assuming idle/talk state). The DC current-limit is specified over temperature between 100 mA and 250 mA. The current-limit circuitry has a negative temperature coefficient. Thus, if the device is subjected to an extended low-level power cross, the value of current passed by the break switch will decrease as the device heats due to the fault. If sufficient heating occurs, the temperature shutdown mechanism will activate and the device will enter an All Off mode. This occurs when the device temperature reaches a minimum of 110°C. The thermal shutdown mechanism activates and forces the device into an All Off mode, regardless of the logic input pins. Pin TSD (as on the Le75282, or when used as an output on the Le7518x devices), will read 0 V when the device is in the thermal shutdown mode and V_{DD} during normal operation. Once in the thermal shutdown mode, the device will cool and exit the thermal shutdown mode, thus re-entering the state it was in prior to thermal shutdown. Current, limited to the DC current-limit value, will again begin to flow, and device heating begins again. This cycle of entering and exiting thermal shutdown will last as long as the low-level power cross fault is present. The frequency of entering and exiting thermal shutdown will depend on the magnitude of the power cross.

If the magnitude of the power cross is larger, then the ring break switches (and tip break switch on the Le75282) will go into current fold-back, thereby further reducing the power dissipation in the LCAS. The external secondary protector will probably also trigger, shunting all current to ground. When the LCAS break switch goes into current fold-back or the external secondary protector crowbars, there is insufficient heating to put the LCAS into the thermal shutdown All Off mode.

3.2 Utilizing the All Off State on the Le75282 LCAS during Power Cross

When a power cross condition occurs, it is desirable to isolate the line card from the fault. If the Le75282 LCAS is controlled by the Le79228x ISLAC, the ISLAC will detect the ac fault condition. When an ac fault is detected, the LCAS should be programmed to its All Off state.

If the power cross occurs during idle or active states, the ISLAC will detect the fault and the LCAS can be programmed into the All Off state and the SLIC into the disconnect state.

If the power cross occurs during a ringing state, the ISLAC needs to first ring trip due to the power cross. In order for the ISLAC to ring trip on power cross with external ringing, the power cross ring trip bit (PC_RT) must be set (Command 60/61h CCR3). After the ISLAC ring trips, the ISLAC will enter the idle or active state determined by the programming of the ISLAC Automatic Ring Exit State control (Command 24/25h). Then in idle or active state the power cross will be detected by the fault detector and the line can be isolated by putting the LCAS into the All Off state and the SLIC into the disconnect state.

3.2.1 Le75282 All Off State

To isolate the LCAS during a power cross event with the Le79228x ISLAC, perform the following steps. Note, this functionality is built into the call control of the Zarlink VoiceEdge™ Control Processor (VCP) device, so with a VCP implementation no user action is required.

Initialize IFTA setting in DC Feed Parameters (C6h) to 05h. This sets the AC fault threshold to 22.5 mArms.

Poll Signaling Register or perform interrupt processing.

When ACFAULT is detected on a given channel, immediately write ISLAC device State Register (56h) ST2-ST0 bits to 110 respectively. This sets SLIC to disconnect state.

Set the LCAS OFFx bit low. If using the ISLAC I/O bit to control All Off, write I/O Register (52h) I/Ox bit to 0.

And immediately write Activate CODEC (0Eh). This allows the ISLAC to monitor the AC fault.

When the SLIC is in disconnect and the codec is activated, the A lead voltage appears on the IMT output and the B lead voltage appears on the ILG output. Those voltages can be sampled by reading registers

VIMT (A9h) or VILG (ABh). However, the values will be fluctuating up and down at 60 Hz and many samples will be required to identify the peak.

A better solution is to set the device into test mode and connect VIMT or VILG to the test tool box input. Then, filter 1 and filter 2 can be used to implement a high-pass filter, the math block can square all output samples, and the test integrator can add them up over n cycles of 60 Hz. Bit TVD of CCR2 can be used to start an integration period and monitor when it completes, or a TESTX interrupt can be generated upon completion. At this time the Test Result register (DDh) can be read to get TSTR, the result of the integration. This will be the sum of the current squared. It can be simply compared with a threshold, or a square-root can be done to calculate an RMS value. This measurement has to be done alternating between the A lead and the B lead because the foreign voltage may not be present on both leads.

When the fault is no longer present, the line can be put back into service.

4.0 EXTERNAL SECONDARY PROTECTION

External secondary protection consists of over-voltage and over-current protection components. Schematics are presented in Figures 5 – 7. Component values are listed in Table 1.

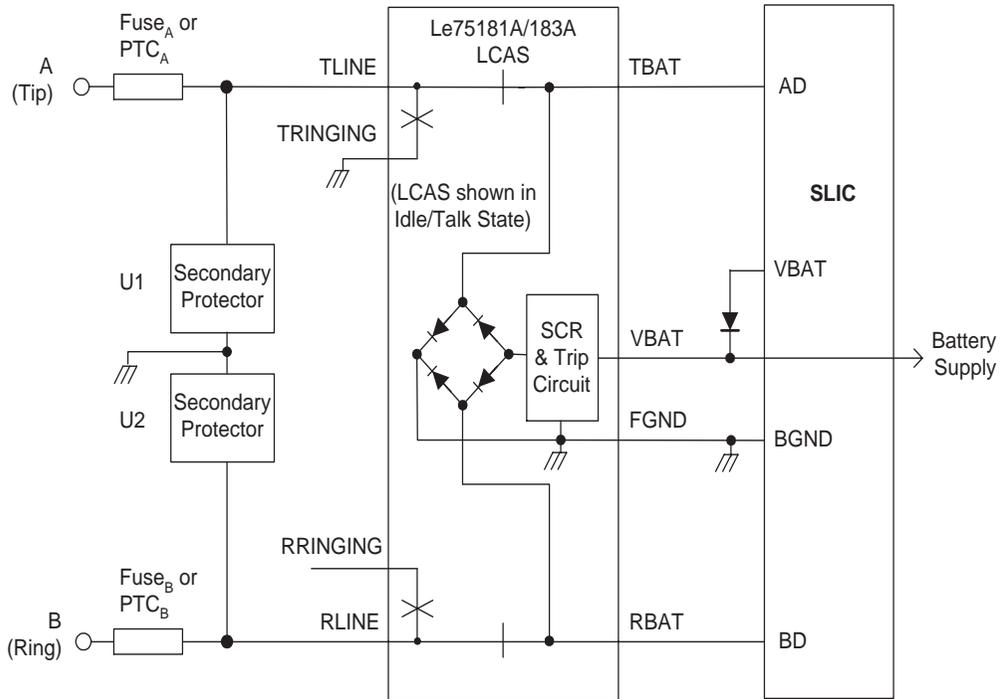
4.1 Protection Architectures

An external over-voltage protector is required on the line side to ensure that voltages applied to the LCAS do not exceed the maximum ratings of the device.

Figure 5 shows a protection scheme for the Le75181A or Le75183A LCAS using a fuse or PTC for over-current protection.

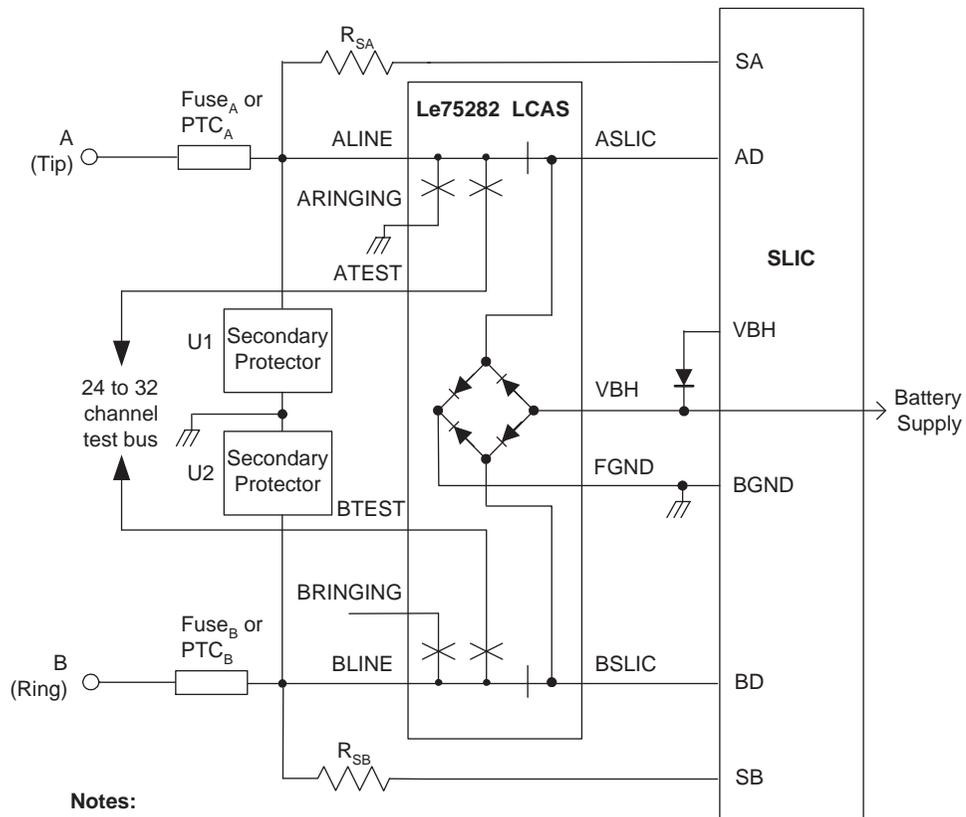
Figures 6 and 7 show protection schemes for the Le75282 LCAS. When used with an Le79232 ISLIC device, the ISLIC can sense A/B voltage on either side of the over-current protection device. Voltage is sensed through the sense resistors R_{SA} and R_{SB} . The power and surge rating of these resistors is determined by their placement. If a fuse or PTC is used for over-current protection and the A/B voltage is sensed inside the over-current element (as shown in Figure 6), a lower wattage sense resistor can be used. The disadvantages with this approach are that the longitudinal balance is subject to the resistance matching of PTC elements and foreign voltage can not be sensed if a PTC is in its high impedance state. The advantages of sensing A/B voltage outside a PTC as shown in Figure 7 are that longitudinal balance is not subject to the resistance matching of the PTC elements and foreign voltage can still be sensed when the PTC is in its high impedance state. However, the sense resistors must be surge rated and some state control is required (like that provided by the Zarlink VoiceEdge™ Control Processor (VCP)) to place the ISLIC into a disconnect state when a fault is detected.

Figure 5. External Secondary Protection - Le75181A & Le75183A



Test out, test in, and ringing test switches not shown for Le75183A
 See Protection Components section for component values

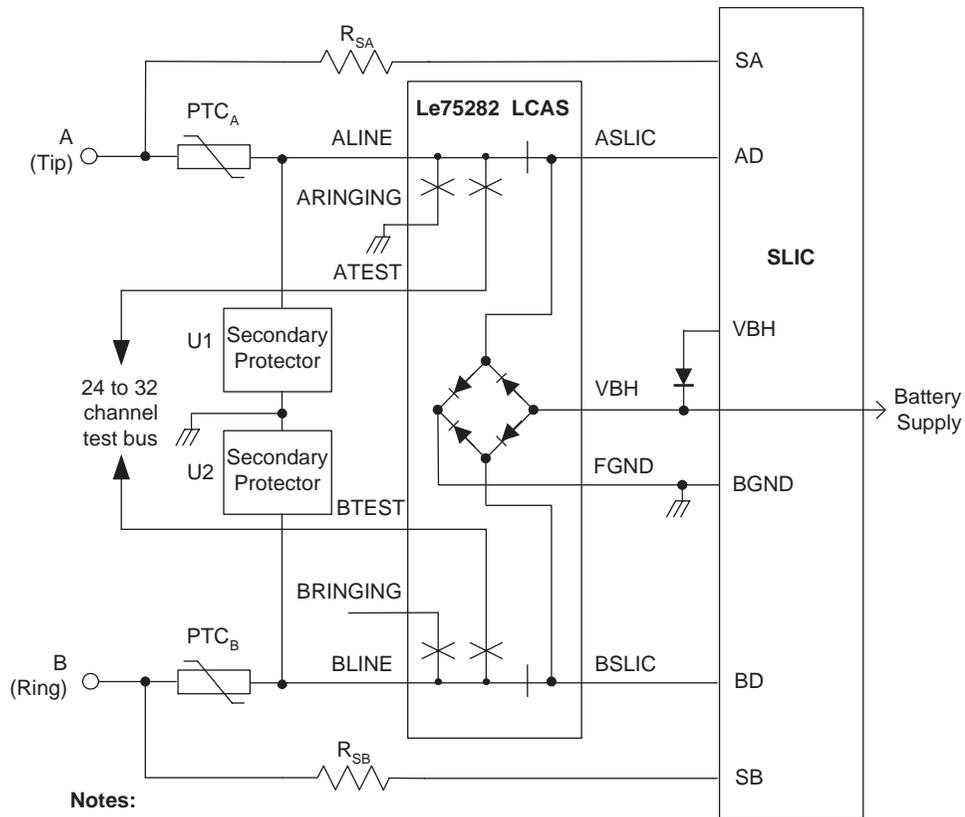
Figure 6. External Secondary Protection - Le75282 Sense Inside Over-current Protection



Notes:

LCAS shown in Idle/Talk State.
See Protection Components section for component values.

Figure 7. External Secondary Protection - Le75282 Sense Outside Over-current Protection



Notes:

LCAS shown in Idle/Talk State.

See Protection Components section for component values.

4.2 Protector Selection

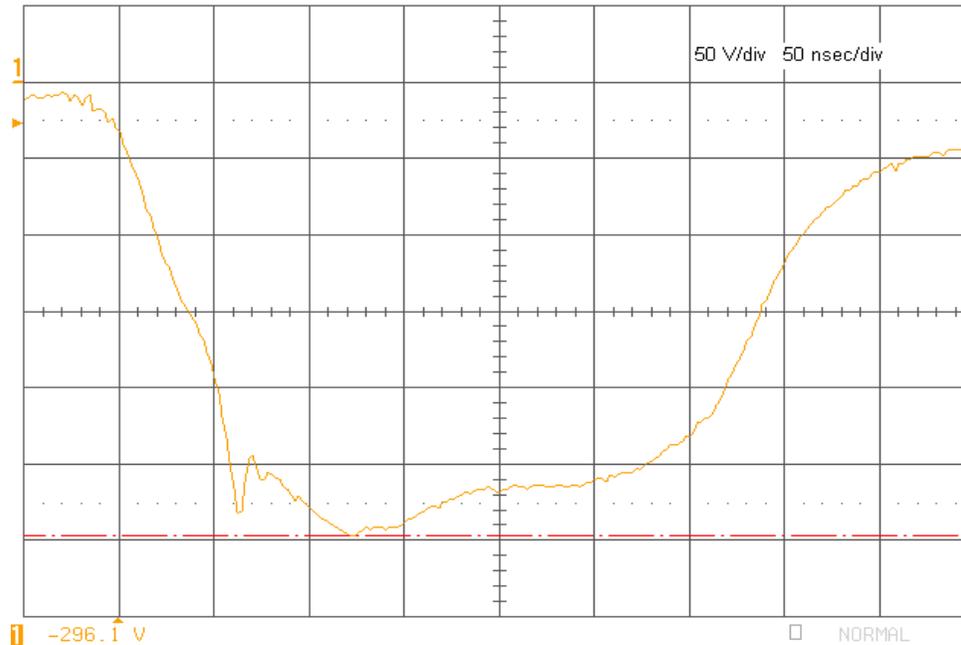
When the LCAS is used with a SLIC device, the SLIC "battery referenced" protector is replaced with a "fixed" voltage protector placed in front of the LCAS as shown in the previous figures. It is imperative that the correct zener and break-over voltage be selected for the fixed voltage protector.

A solid-state bidirectional thyristor over-voltage protector is recommended for LCAS protection. The LCAS provides unbalanced battery backed or unbalanced earth backed ringing. The line will see worst case operational voltages during ringing. The peak ringing signal plus dc bias provides the peak voltage which is the minimum stand-off voltage that can not be clamped. This is normally specified as the peak off-state voltage (V_{DRM}). Beyond this threshold the thyristor device enters a zener region, clamping the over-voltage. As fault voltage increases, current increases through the thyristor device and the zener voltage increments higher until the break-over current (I_{BO}) or switching current (I_S) value is exceeded. This defines the thyristor's break-over voltage (V_{BO}) or switching voltage (V_S). This break-over voltage value can not exceed the LCAS device's isolation (breakdown) voltage.

The break-over voltage of the thyristor is often specified as a typical value. For design purposes, the worse case break-over voltage value must be determined. The worse case value is the typical value plus the break-over voltage tolerance, plus increased voltage due to temperature coefficient, plus increased voltage due to rate of rise overshoot (dv/dt). The protectors are normally specified for dv/dt overshoot at a relatively low dv/dt value. Actual dv/dt values need to be considered when selecting a thyristor. A unipolar 2500 V, $2 \times 10 \mu s$ impulse waveform, as specified by GR1089, rises to 2500 V in $2 \mu s$. The waveform has an exponential rise, so at the thyristor triggering voltage of about 250 V, the rate of rise is extremely fast, on the order of $5000 V/\mu s$ or greater. This fast dv/dt can cause considerable overshoot in a thyristor. Figure 8 shows a scope capture of a thyristor subjected to a negative 2500 V surge at room temperature. This thyristor is rated for a typical break-over at -260 V. You can see that the thyristor exhibits 36 V of overshoot and the actual break-over voltage is -296.1 V. This in itself does not exceed the breakdown voltage of the LCAS, but could cause excessive voltage if combined with an inductive kick of an unclamped splitter as discussed in the next section or with the effects of battery or the ring generator on the subscriber side of the switch. Overshoot

due to break-over voltage tolerance, temperature, and dv/dt varies between different thyristor architectures, be sure to characterize a given thyristor for its applicability to LCAS protection.

Figure 8. Secondary Protector Overshoot



Using the bidirectional thyristor over-voltage protectors listed in Table 1. For a negative voltage on the B lead and battery backed ringing, the protector clamps voltages at -190 V (V_{DRM}) (refer to the protector data sheet for voltage-current characteristics). The device remains in this clamped state until fault voltage rises to the devices' break-over voltage, typically -250 V (V_{BO}). In break-over, the device crowbars into a low voltage state thereby drastically reducing the power dissipation in the protector device and removing the voltage stress from the LCAS device. Note, while the values listed here are typical, protector clamp and break-over voltages must be chosen by the system integrator per the system's unique requirements.

For a positive fault voltage on the B lead, the clamp and break-over voltage can occur at a lower voltage. Utilizing asymmetrical protection for the B lead (with respect to positive and negative voltage) is a prudent choice. If a protector with a symmetrical break-over voltage were to be used, when a high voltage power cross occurs on the line, the secondary protector would clamp the voltage at 250 V , and as the polarity changes, clamp the voltage at 250 V in the opposite direction. This subjects the LCAS to a rapidly changing 500 V dv/dt . When a large voltage is present (as is the case when a power cross is present on the line and at its positive peak and the ringing signal on the ringing bus is at its negative peak) and the LCAS is subjected to a fast dv/dt , the ringing access switch can turn-on. This will not hurt the LCAS switch, but the fault can then pass into the ringing bus and subject the ringing feed resistor to excessive power. If an asymmetrical protector with a rating of -190 V (V_{DRM}), -250 V (V_{BO}) and $+100\text{ V}$ (V_{DRM}) and $+125\text{ V}$ (V_{BO}) is employed, the differential voltage across the LCAS device during an excessive power cross is reduced to an absolute V_{BO} voltage or 375 V . Under most conditions, this will eliminate fault feed-through to the ringing bus.

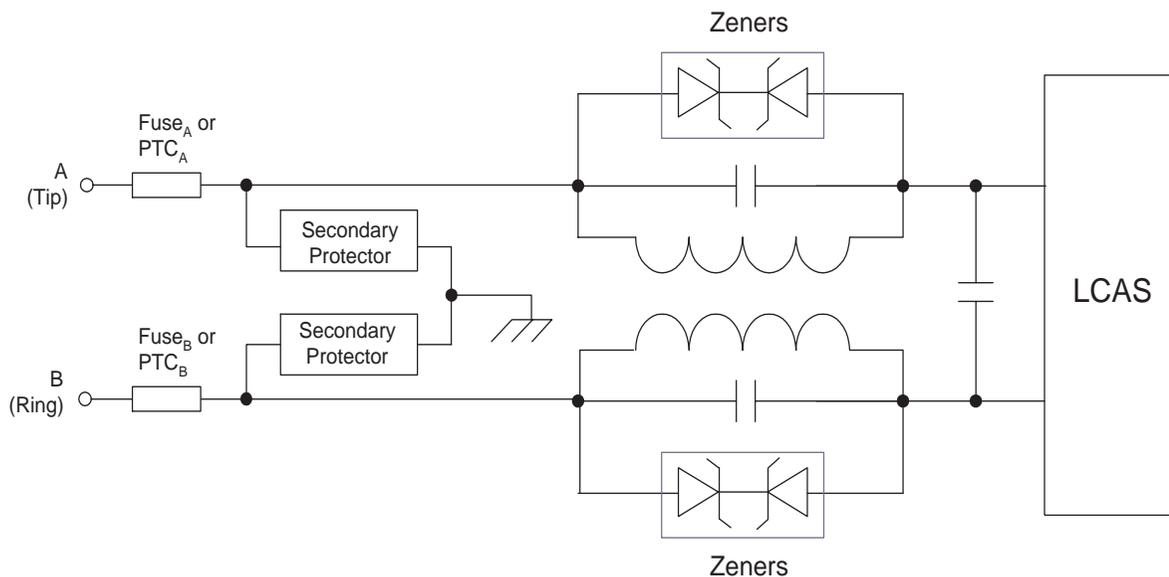
For the A lead and battery backed ringing, both negative and positive fault voltages can usually be clamped at a lower voltage. A symmetrical $\pm 100\text{ V}$ (V_{DRM}), $\pm 125\text{ V}$ (V_{BO}) protector can be used on the A lead.

4.3 External Secondary Protector with POTS Splitter

If an IVD POTS splitter is used with an LCAS device, the splitter can be positioned on the line side of the secondary protector or between the secondary protector and the LCAS. If the latter architecture is used, additional components to suppress counter emf generated by the splitter coil are required. A pair of 16 V zener diodes should be used across the splitter coil to avoid clipping of the DSL signal. Proper deployment is illustrated in Figure 9. Another alternative is to use transient voltage suppressors (as those described in section 5.0) on each LCAS lead to ground.

Note:

If the ISLIC is used, for stability reasons the POTS splitter must be outside the A/B voltage sense point.

Figure 9. POTS Splitter Application - Splitter between Secondary Protection and LCAS

See Protection Components section for component value

4.4 Over-current Protection

The LCAS break switches will limit current to the SLIC, but the secondary protector and the ringing access switch are not current-limited protected. Short circuit, long duration power fault tests as specified by Telcordia and ITU make an external current-limiting component a necessity. Fuses, line feed resistors (LFR), and resettable PTC's are the most widely used components to perform this function.

The PTC is a positive temperature coefficient device that exhibits a dramatic resistance change when its operating temperature is exceeded due to an increase in current flow. The device cools to approximately its original resistance when the excess current is removed. PTC's are in effect resettable fuses. They are available in polymer and ceramic material. Polymer is more suited for higher voltages and lower line resistances. The lower the resistance of the series element, the higher the current rating of the over-voltage protector needs to be. Also note that the matching of the series resistance between the tip and ring elements may have a significant influence on the longitudinal balance.

4.5 Test Switch Protection Considerations

The most robust design has proper capacitive termination of the test access switches. For a 24 or 32 channel test bus, when all the test leads are tied together, the overall capacitance of the test bus provides adequate termination for the test access switches. For a test bus with less than 24 channels, tie all the leads together and add a single test bus capacitor on ATESTx (or TTESTout) to ground and on BTESTx (or RTESTout) to ground with a value of 32 pF for each channel less than 24. For any termination scheme, capacitance to ground on the test nodes should be kept less than 10 nF.

Systems that do not use the test access switch functionality must also add capacitance to the test switch node or short the test switches. If the test access switches are not to be used:

For the Le75183 device, place a 1 nF, 100 V capacitor on TTESTout to ground. Likewise, place a 1 nF, 100 V capacitor on RTESTout to ground. Alternatively, the test access switches can be shorted out. TTESTout can be shorted to TLINE and RTESTout shorted to RLINE.

For the Le75282 device, ATEST1 and ATEST2 can be tied together with a 1 nF, 100 V capacitor on this node to ground. Likewise, tie BTEST1 and BTEST2 together with a 1 nF, 100 V capacitor on this node to ground. Alternatively, the test access switches can be shorted out. ATESTx can be shorted to ALINEx and BTESTx shorted to BLINEx.

4.6 Grounding Considerations

If the grounding architecture is such that the secondary protection ground is not directly connected to the LCAS and SLIC ground (not using a single ground plane) the possibility of a ground bounce must be taken into consideration when selecting the secondary protector break-over voltage. It is quite common to experience lightning hits or AC induction faults that affect more than one line. In this case, the secondary protector current, as defined by the over-current protection device and by the type of primary protection, will flow through the secondary protection ground and cause a small voltage shift. This voltage shift will increase in magnitude as more and more secondary protection devices enter their conduction state such that the last device to trigger will experience the worst increase in its effective break-over voltage. The resistance of the over-current devices, the break-over voltage of the secondary protectors, and the ground plane current carrying capacity must all be considered to avoid exceeding the LCAS ratings.

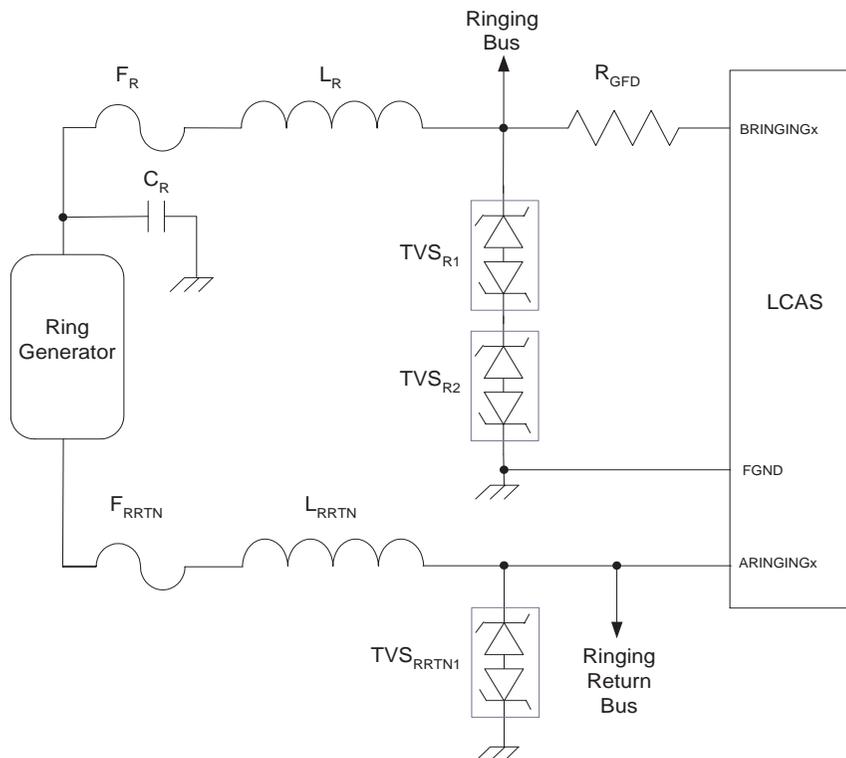
5.0 RINGING BUS PROTECTION

With proper line secondary protection the ringing access switch is well protected from transients occurring on the telephone line. What is often overlooked are transients that can occur from the ringer itself. There is no inherent LCAS protection from over-voltages on the ringing bus. Noise from the ring generator or simply rapid change in current draw from an inductive generator can cause a high voltage dv/dt which can easily exceed the breakdown voltage of the LCAS.

Figure 9 illustrates a protection scheme for the ringing generator. Only one circuit is required per generator. The circuit consists of a decoupling capacitor (C_R) on the ring generator output to reduce high frequency switching noise. Fuses (F_x) in both the ringing and ringing return paths. A series 10 mH choke (L_x) to attenuate di/dt 's and transient voltage suppressors (TVS_x) shunted to LCAS fault ground. The TVS devices are bidirectional voltage clamping elements.

On the ringing bus two 100 V TVS devices are used in series to obtain a stand-off voltage of 200 V. The clamping voltage of a TVS is higher than the stand-off voltage and should be chosen not to exceed the LCAS breakdown voltage. The ringing return bus operating voltage is at ground or at battery voltage (earth back ringing), so only one TVS should be required on the ringing return node.

Figure 10. Ring Bus Protection



See Protection Components section for component values

5.1 Ringing Feed Resistor

The ringing feed resistor (R_{GFD}) limits current in the ringing path and through the LCAS during ringing and when a phone goes off-hook prior to ring trip. The resistor will dissipate significant power when off-hook and needs to be sized accordingly. In addition, the resistor can be subjected to surge currents when a fault occurs in the ringing state; or subjected to pass-through current if a fault occurs in an active LCAS state where the break-over voltage of the ringing access switch is exceeded. This can occur during power cross when ringing is at a negative peak on the ringing bus and power cross is at a positive peak on the line side. The positive voltage will increase to the protector break-over voltage as current flows through the break switch and the diode bridge to ground. As the break switch goes from its current-limit characteristic to its foldback characteristic and the secondary protector crowbars, a dv/dt is generated. This dv/dt in conjunction with the high voltage potential across the LCAS at this instance can momentarily turn-on the ringing access switch. The ringing access switch will not be damaged in this break-over condition if the ringing feed resistor maintains its integrity.

Since the ringing feed resistor is subjected to transient power, the ringing feed resistor needs to be a wirewound or surge rated resistor. Wirewound resistors are better suited for pulse handling than ceramic resistors. The power dissipation needs to be a minimum of 2 W. Often use of two wirewound or surge rated resistors is desirable so smaller components can be used and the power dissipation can be shared.

6.0 PROTECTION COMPONENTS

Table 1 lists specific part numbers for the protection components shown in the circuits of Figures 5–7 and 9, 10. These components or a suitable equivalent part can be used for LCAS protection. It is expected that the system integrator will perform due diligence and system validation of these components prior to manufacturing production or field deployment.

Table 1 Protection Devices

Figure	Item	Description	Part #	Value	Tol.	Rating	Manufacturer of Specified Part #	Additional Manufacturers	
5, 6	F _A , F _B	Fuse	B1250T	1.25 A		600 V	Bourns®	Littelfuse®, Raychem®	
6	R _{SA} , R _{SB}	Chip resistor	ERJ-12NF2003V	200 kΩ	1%	0.5 W	Panasonic®	Welwyn Components®	
7	R _{SA} , R _{SB}	Pulse withstanding chip resistor	PWC2010-200KF	200 kΩ	1%	0.75 W	Welwyn Components®		
		Wirewound resistor	WSC0002200K0F			2 W	Vishay®		
5–7	U1	Over-voltage Protector	TISP4125H3	±125 V			Bourns®	Littelfuse®	
5–7	U2	Asymmetrical Over-voltage Protector	TISP4A250H3	+125 V, -250 V			Bourns®		
5–7	PTC _A , PTC _B	Over-current protection	Resistance value can be any value between 3 Ω and 50 Ω						Littelfuse®, Raychem®
			61509	50 Ω			Vishay®		
			CMF-RL50	50 Ω			Bourns®		
9		Zeners	DZ23C16	16 V		0.3 W	Diodes Inc.®		
10	C _R	Capacitor	Value per ring generator manufacturer specification						
10	F _R , F _{RRTN}	Fuse	Size accordingly to ring generator output capability			Slow Blow	Raychem®		
10	L _R , L _{RRTN}	Choke	RL-1256-4-10000	10 mH			Renco Electronics, Inc.®		
10	TVS _{R1} , TVS _{R2} , TVS _{RRTN1}	Bidirectional Transient Voltage Suppressor	5KP100CA 5KP100C	100 V			Microsemi®		
			Transil™	BZW50-100B	100 V			ST®	
10	R _{GFD}	Wirewound Resistor	WA83Z511RG	511 Ω	2%	2 W	Welwyn Components®		
			WSC0002511R0G	511 Ω	2%	2 W	Vishay®		
		Pulse withstanding chip resistor	PWC2512-1K02F	1.02 kΩ	1%	1.5 W	Welwyn Components®		
			Use two resistors in parallel						

7.0 SUMMARY

Without protection, telephone line voltages and excessive fault potentials can be destructive to solid-state line card devices. With its built-in protection features and its SLIC protection, the LCAS is a rugged device, but no match to high voltage transients that exceed its rating. Line card robustness can greatly be increased by employing the line and ringing bus protection circuitry discussed herein and with proper component selection.



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a license under the Philips I²C Patent rights to use these components in an I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL, the Zarlink Semiconductor logo and the Legerity logo and combinations thereof, VoiceEdge, VoicePort, SLAC, ISLIC, ISLAC and VoicePath are trademarks of Zarlink Semiconductor Inc.

TECHNICAL DOCUMENTATION - NOT FOR RESALE
