ZARLINK SEMICONDUCTOR

Application Note **MSAN-161**
Application Hints for the MT90840

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Introduction

Some applications in distributed communication systems require a large amount of bandwidth to be transported or shared between stations that can be physically separated within a specific location or a campus. Depending on the type of traffic to be transported between the stations in a campus or between campus remotely located, certain basic requirements have to be met.

This application note covers some of these basic requirements, suggests one solution for the implementation of distributed transport systems and provides some hints on how to use the MT90840 device when implementing an add/drop, switching or multiplexing functions for 155 Mb/s transport backbones.

Unified Transport Infrastructure for Multimedia

Existing multimedia requirements focus on a new type of application which combines voice, data and video information in such a way that computers can be used as real-time, two-way communication entities in addition to their traditional data processing applications.

Emerging applications will provide not only video and audio play-back but also interactive, two-way, multi-party communications from desktop to desktop across local and wide area networks. From a communications perspective, multimedia can be classified into two types of operations. The first type is a playback application where a user interacts with a database to gain specific information. For enterprise networks, this application is implemented through network servers that contain the information to be retrieved. Some examples of playback applications are: educational and entertainment server-based video playback, Home Video Distribution, video mail, real estate House/ neighbourhood viewing, travel agency hotel/room display, medical imaging, sound and video production, CAD file retrieval, library text/audio/video retrieval.

The second type of operation falls into the delay-sensitive class of service where real time video and voice information must be delivered to the user with a certain acceptable quality. Applications that fall into this category are: video conferencing and video phones, interactive video classes, multimedia work

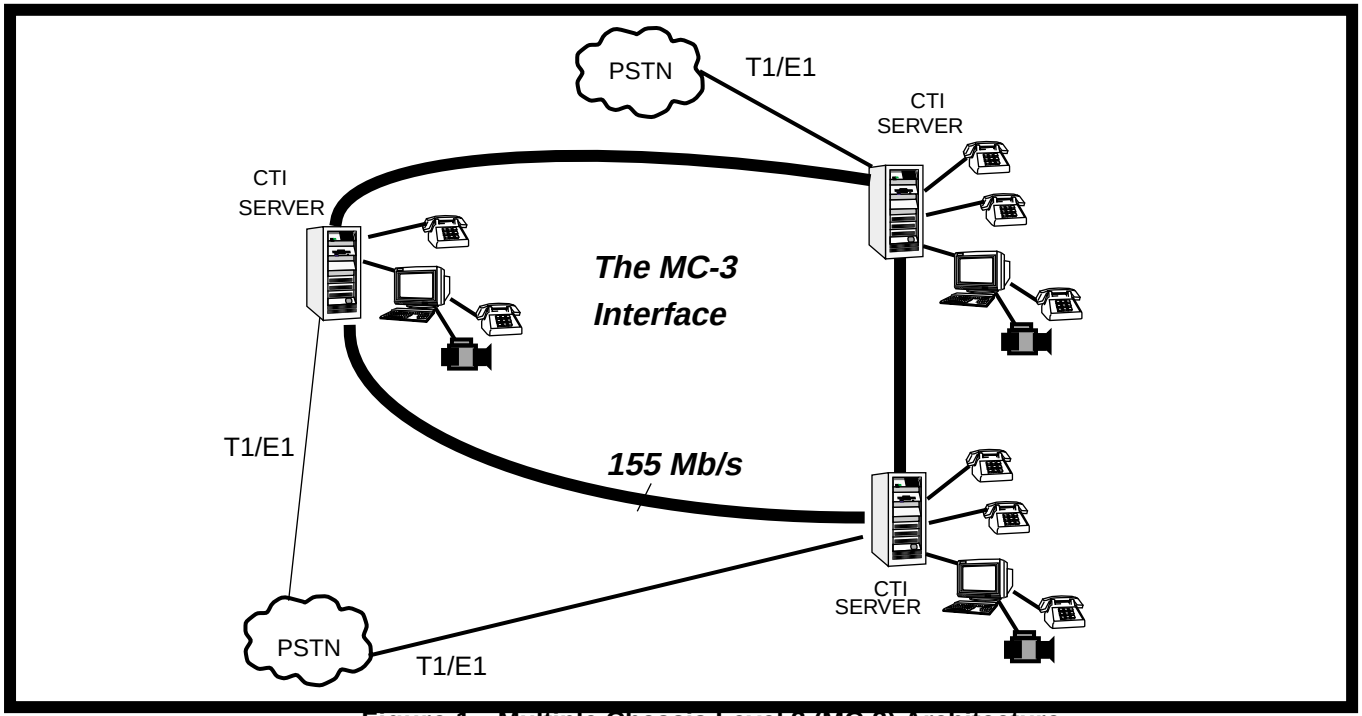


Figure 1 - Multiple Chassis Level 3 (MC-3) Architecture

collaboration (document sharing), home telecommuting and concurrent CAD/CAM.

These two classes of operation have some specific requirements in three key parameters: bandwidth required to transport the service, data transfer delay through the physical network and synchronization with existing wide area network.

The bandwidth parameter varies according to the amount of raw data that has to be carried from different sources to its destination. The bandwidth requirements depend on which segments of the network are discussed. For example, in a multimedia LAN environment, a desktop connection must support relatively few applications at a time when compared with a backbone connection that can consume a large amount of bandwidth. As an example, in an interactive real time application such as a H.261 video conference, the bandwidth requirements vary from 64 to 1920 kb/s. Most of the video conference calls across the WAN still remain at small amount of kb/s (e.g; switched 56 kb/s and ISDN 128 kb/s) although services provided by most of the long distance carriers allow for up to 1.5 Mb/s connections.

Considering video conferencing applications internally to the enterprise, the Local Area Network must be capable of carrying the aggregate bandwidth of potentially hundreds of users. An MPEG or JPEG video server, for example,needs a backbone that supports dozens of video streams at time. In this scenario an internal backbone operating at tens of Mb/s can be easily justified.

Considering data transfer delay in a multimedia network, applications such as video playback do not have the same stringent requirements as real time interactive services. For a continuous playback video, users will not mind even a couple of seconds of delay before the video stream arrives. However, delay requirements of real time interactive multimedia applications such as video conferencing are very tight.

Video conferencing normally occurs over a wide area connection and includes video and audio compression, both of which incurs delays. Today's video codecs require from 50ms to 250ms to perform coding and decoding. Therefore, the LAN connection as well as LAN to WAN interface, must contribute the minimum delay possible during a wide area video conference. As an example, for the implementation of a H.320 conference, video and audio sent over the LAN and then across the WAN and then back to the LAN, requires stringent design rules for LAN bandwidth, delay, jitter and especially end-to-end synchronization.

Wide Area Network synchronization is an important requirement in mixed network environments to maximize the potential and usefulness of a LAN-based video conference application. The H.320 standard defines how video conferencing services in a LAN should be provided across the WAN. The reality of WANs is that they are predominantly synchronized to an 8kHz reference signal and transport real time services using Time Division Multiplexed (TDM) technology. This type of network is called "Isochronous" which can be interpreted as being a series of repetitive/periodic time-slots for the transmission of constant bit rate services at the physical bit transmission level.

As a result, the H.320 video and audio information is framed with the network 8kHz reference clock. Any real time multimedia connection from the LAN across the WAN must recover these synchronized frames with minimal loss and delay. To solve this problem, distributed communication systems that can support the transport of isochronous traffic by utilizing Time Division Multiplex technology have the unique ability to provide seamless connection to the existing WAN.

Low latency isochronous backbones based on TDM switching and transport technologies provide the capabilities necessary for the deployment of systems that require cost effective implementation, high bandwidth, predictable data transfer delays and direct synchronization with the wide area network.

The Need for Real-Time Switching in Computer Telephony Integration (CTI)

Certain applications in Computer Telephony Integration require a large amount of bandwidth to be handled or processed simultaneously in real time within a server. Let’s take an example: Unified Messaging systems. In unified messaging systems, multiple DSP resources residing within a CTI server have to process user commands in real time providing reasonable answer times upon specific functions like retrieve or send a fax, play voice mail, play e-mail, store message, etc. Typically, unified messaging systems may receive user commands either from the desktop (via LAN connection) or from the public network (T1/E1, ISDN,etc).

Current implementations of such systems employ a PC-chassis with internal switching buses such as the MVIP™ (Multi Vendor Integration Protocol™) which allows fast switching and routing of the user’s 64 kb/s channels from the public network to the local

available DSP resources in the server. Existing products implemented with MVIP buses can handle up to 512 simultaneous 64kb/s connections in real time. This proven technology is found within many different products ranging from voice mail or unified messaging systems, audio and video conferencing bridges, small PBXs, PC-based bandwidth managers, Interactive Voice Response (IVR) systems and others.

Large CTI & High Bandwidth Processing Systems

Some CTI implementations require multiple T1/E1, ISDN or Analog trunks to be terminated within the systems allowing thousands of users to have the access to the DSP resources and benefit from the service. Examples of such systems are the ones provided by some RBOCs or service bureaus which sometimes have to terminate over 50 T1 or E1 trunks to connect its service users in the local operating area. Due to the demand for large systems as well as the limited processing power that the CPU in a single PC-chassis may deliver, the CTI industry has adopted what is called multiple-chassis architecture.

In multi-chassis systems every PC can terminate a specific number of trunks (say for example, 6 to 10 E1 trunks) and it is connected to a network of PCs through an isochronous transport backbone so that if the local DSP resource within a single PC is full, the other available resources in the network of PCs can be shared. Moreover, by employng a fast switching and transport backbone between the CTI servers also allows the fast routing and retrieval of audio messages from a source located anywhere in the network of servers to any of the multiple exit trunks available. This is the typical scenario when implementing large voice mail, IVR or teleconferencing systems.

Therefore, a fully distributed network can be deployed where the applications can access the resources located in one or multiple chassis connected to the same backbone. This is similar to the existing legacy LANs where remote servers can be accessed by many users through a fast data link such as FDDI or Fast Ethernet. The main difference is that CTI implementations require a fully isochronous backbone whereby the utilization of the bandwidth is guaranteed for the entire duration of the call.

Another requirement to be taken into consideration when designing a multi-chassis CTI system is the physical distance between each individual server. For applications within a small area the inter-server connectivity can be done utilizing copper or coaxial cables. However, for a multiple-chassis product with the requirement to operate in a broader area such as in a campus, an isochronous backbone running over fiber optics is more advantageous.

One of the interconnection schemes available for multi-chassis CTI being standardised by the GO-MVIP (The Global Organization for Multi-Vendor Integration Protocol) is called MC-3, Multi-chassis level 3 interface. In MC-3, several PC-based CTI servers are interconnected through a 155 Mb/s fibre optic isochronous backbone. In MC-3, either point-to-point or point-to-multipoint switching connections can be performed in real time whereby n x 64 kb/s channels generated within a specific server (from a trunk or a DSP board) can be switched or routed to any other server in the network forming a "backbone switch approach". Figure 1 shows the MC-3 architecture.

Implementing a 155 Mb/s Transport/ Switching Infrastructure for Multimedia

Today, transmission links operating at SONET rates utilize Serial to Parallel (S-to-P) and Parallel to Serial (P-to-S) converter devices (or Line Interface Units) which perform embeded framing functions and give the user the access to the payload of the high speed frame. These devices are capable of generating a high speed transmission link (e.g; 155 Mb/s) with a framing pattern based on an 8 kHz frame reference.

Example of off the shelf S-to-P and P-to-S converter devices that operate with 8 kHz based synchronization signals are are the Transwitch TXC-02302B SYN-155C, Texas Instruments TDC2301C/ 2302C, AMCC S3005/06 or S3011/12 devices.

In a CTI server application, the 8 kHz taken from the public network (e.g; T1 trunk) is used to synchronize the switching bus (MVIP) between the multiple cards within the server. The utilization of the above high speed framers allow the 8 kHz reference signal originated in the main trunk chassis to be transported across a 155 Mb/s backbone and being recovered at the other stations therefore synchronizing the multiple servers in the network and its internal MVIP switching buses with a main 8 kHz reference. In the MC-3 system, the server originating the main 8 kHz reference from the public network is called master. The other servers recovering the 8kHz are calle slaves.

Zarlink Semiconductor has developed a new switch device that can be employed to terminate the MVIP switching bus and interface to high speed framers to

implement the MC-3 interface. The MT90840 Distributed Hyperchannel Switch device provides an 8-bit bidirectional parallel data port which can be connected to those high speed framers and a serial data port that connects to the MVIP bus. Figure 2 depicts a CTI server providing multiple functions and using the MT90840 device to terminate the MC-3 interface.

Application Hints when Interfacing the MT90840 and the TXC Syn-155 Framer

For example purposes only, this section describes how the MT90840 device can be connected to the Transwitch 02302B SYN-155 device. Along with the TXC SYN-155 device, the MT90840 allows the implementation of switching, multiplexing or add/drop functions to an isochronous Time Division Multiplexed transport backbone operating at 155 Mb/s rates.

Station with ST-BUS Clock Master Operation

Figure 3 shows an example of interconnection between the MT90840 and the TXC-02302B framer in an application whereby the ST-BUS serial interface clocks are used as main reference for the transmission/generation of the 155 MHz output link. In this particular application, Timing Mode 1 (TM1) operation is selected. In TM1, the ST-BUS serial interface clock inputs C4/8R1 & 2 and the Transmit 155 MHz clock to be applied at the HSCKT input of the SYN-155 device must be locked in frequency. The SYN-155C device divides the HSCKT frequency by 8 and provides a 19.44 MHz byte transmit clock reference at the TXRC output which is then connected to the MT90840 PCKT Byte transmit clock. That will comply with the MT90840 frequency locking requirements between PCKT and C4/8R1 & 2 signals.

Typical applications for the MT90840 in TM1 are stations which drive the main reference clock for the system such as the main clock of a PBX or the recovered clock from a T1 or E1 trunk card within a CTI server. The master station takes the 4.096 or 8.192 MHz reference clock and it uses it to generates a 155 Mb/s data stream to be transmitted to the slave stations connected to the system 155 Mb/s backbone. As an example, in a distributed star architecture, the central "hub" may contain several outgoing fiber links implemented as per figure 3. At the other side of the fiber connection, each link

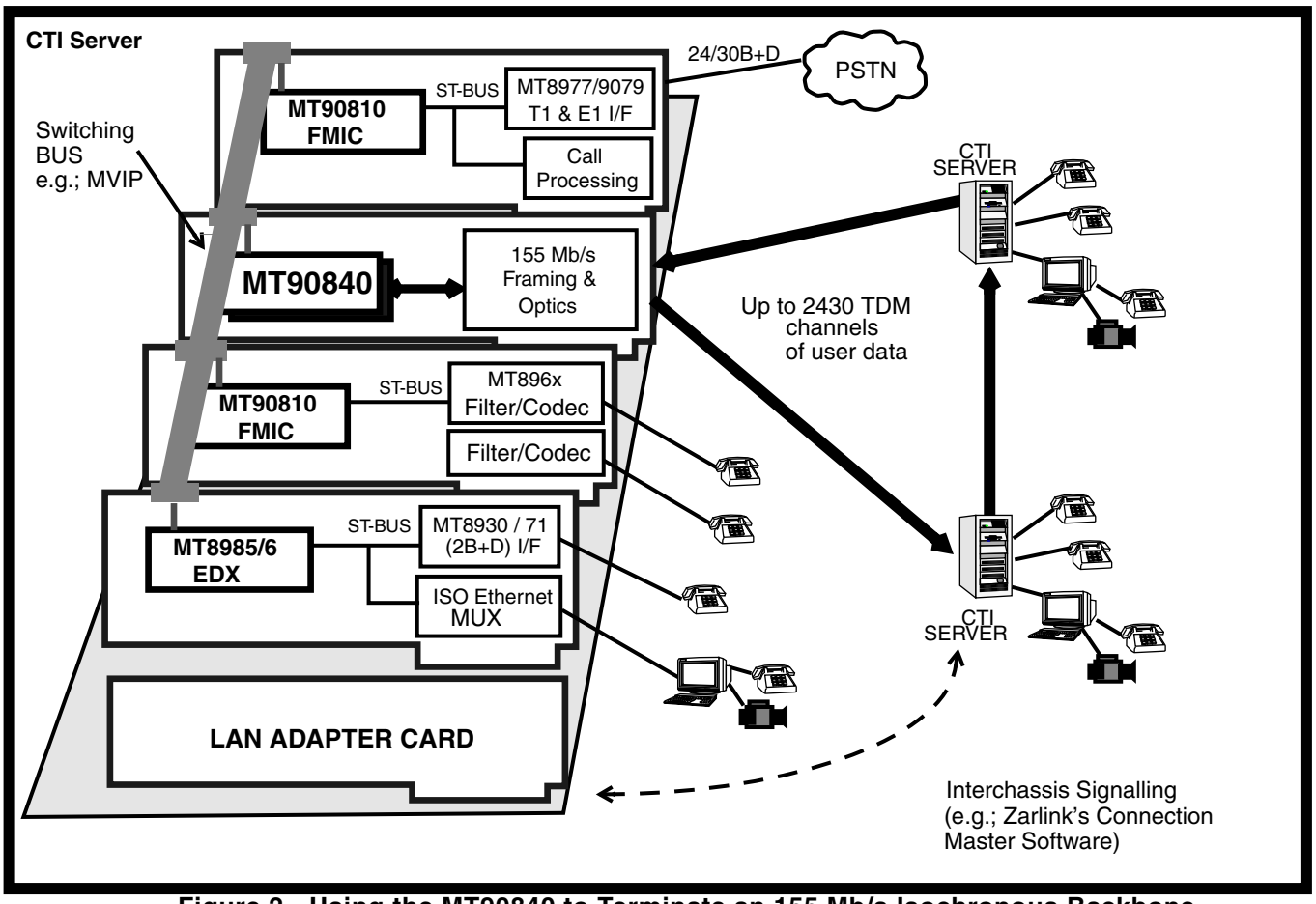
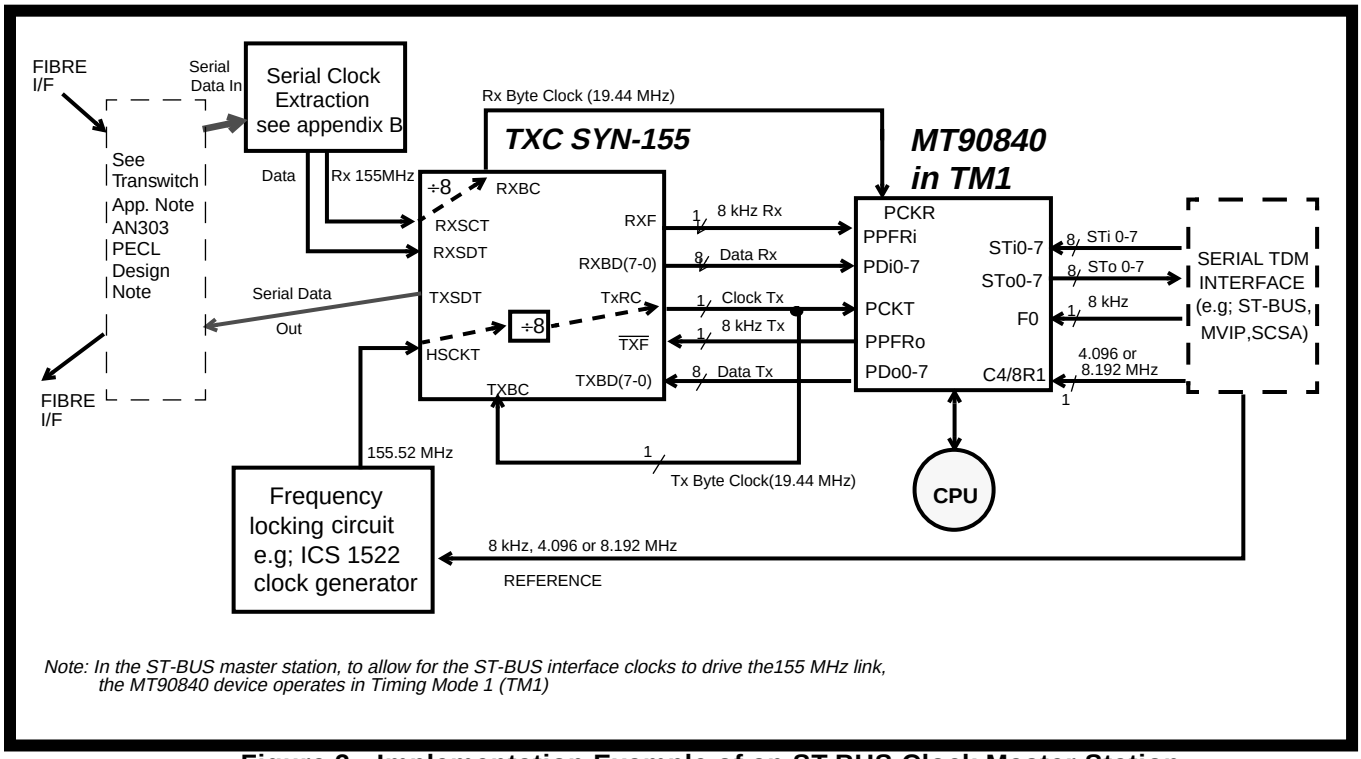


Figure 2 - Using the MT90840 to Terminate an 155 Mb/s Isochronous Backbone



Note: In the ST-BUS master station, to allow for the ST-BUS interface clocks to drive the155 MHz link, the MT90840 device operates in Timing Mode 1 (TM1)

Figure 3 - Implementation Example of an ST-BUS Clock Master Station

would be terminated by a slave station (see section Station with ST-BUS clock slave). On the return path (from the slave to master stations) the accumulated latency caused by fiber propagation delay plus the station's intrinsic delay (e.g; S-to-P & P-to-S conversion time, clock recovery, etc) is absorbed by the MT90840 internal eslastic store which is only available when TM1 is selected.

In the scenario depicted in figure 3, the MT90840 device can be used to time-interchange any 64 (DS0) or n x 64 kb/s channels from the ST-BUS serial streams into any 64 kb/s time-slot of the 155 Mb/s frame. Real time switching functions can be dynamically programmed through the MT90840 internal connection memories or n x 64 channels can be broadcasted from any specific station to multiple destinations in the enterprise through the 155 Mb/s frame.

Framing on 155 Mb/s interface

For transporting the 8 kHz reference across the 155 Mb/s backbone, the TXC SYN-155C device employs the framing technique defined by the SONET standards. The CCITT G.709 and ANSI T1.105 documents specify a 6-byte framing pattern to be transmitted on bytes A1,A1,A1,A2,A2,A2 of the SONET frame. The SYN-155C device when programmed in full tracking mode, expects the SONET 6-byte pattern along with an 8 kHz input reference signal from its parallel data interface (TXBD0-7) at every 125µs. To provide the SYN-155C device with the adequate 6-byte pattern aligned with the expected 8kHz input ($\overline{TXF}$), the MT90840 can be programmed to operate in per-channel message mode during the corresponding byte time expected therefore generating the framing patterns at the right location along with the PPFRo 8 kHz output at every 125µs.

To execute the above procedure, the CPU programs the MT90840 device on per channel message mode at the 6 locations of the Transmit Path Connect Memory Low (TPCM Low) corresponding to the SYN-155C's expected pattern locations. The pattern expected by the SYN-155C is F6, F6, F6, 28, 28, 28 hex. The first 5 bytes are written in the last 5 positions (2425, 2426, 2427, 2428, 2429) of the TPCM low bits. The last 28 hex contents will be written in the first position(position 0) of TPCM low bits. After that the MT90840 outputs the pattern at the PDo0-7 lines at every 125 us until the CPU changes the contents of the TPCM LOW contents. The user should connect the PPFRo signal from the MT90840 to the $\overline{TXF}$ input of the SYN-155C.

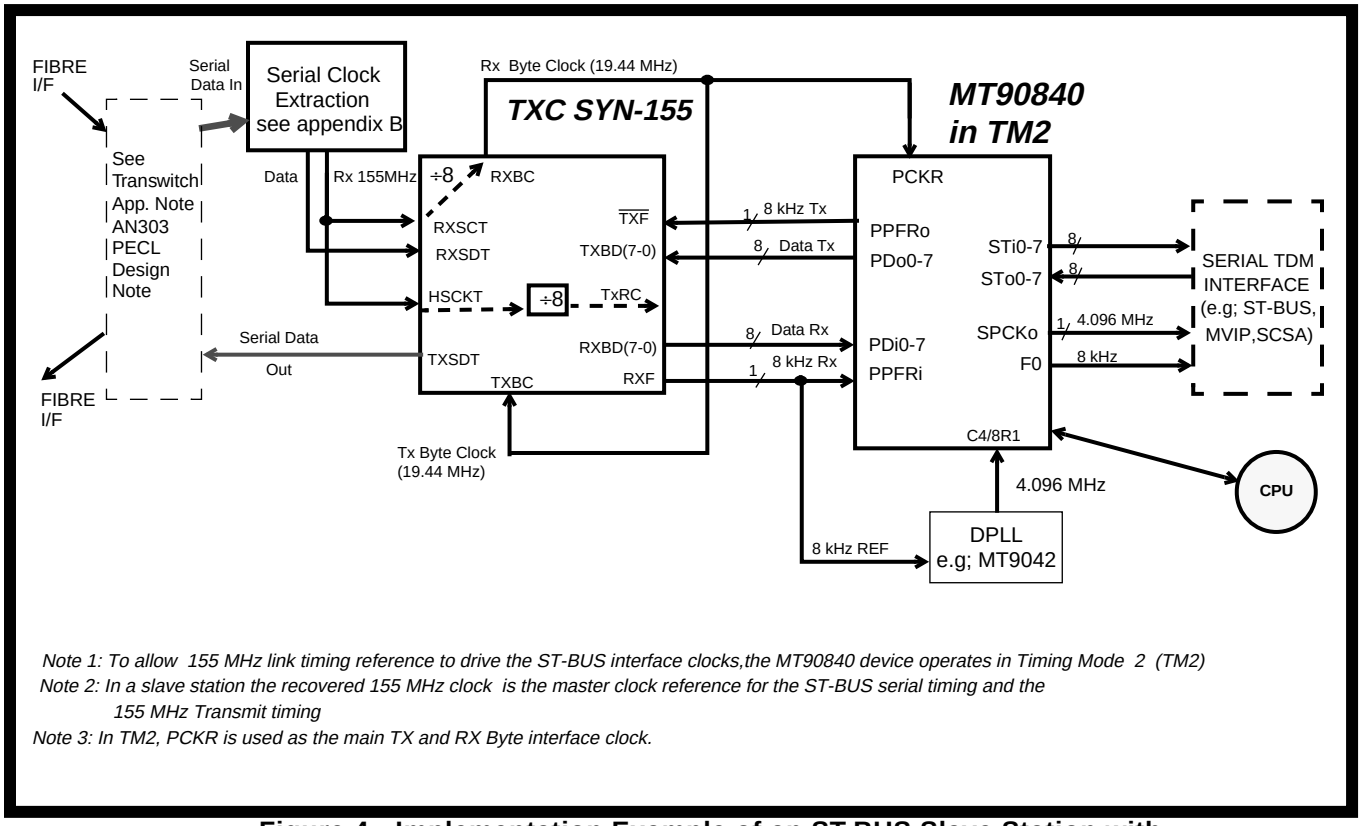
On the receive end, the SYN-155C device detects the framing pattern and it generates an output frame pulse (RXF) which toggles along with the last 28 hex of the framing pattern.

Station with ST-BUS Clock Slave Operation

Figures 4 to 6 show examples of interconnection between the MT90840 and the SYN-155C devices in an application whereby the ST-BUS serial interface and the 155 MHz Transmit clocks are slaved from the incoming 155 MHz received timing. In this particular application, the MT90840 device operates in Timing Mode 1 (TM2). The same framing procedures described in the previous section are applied to the slave station.

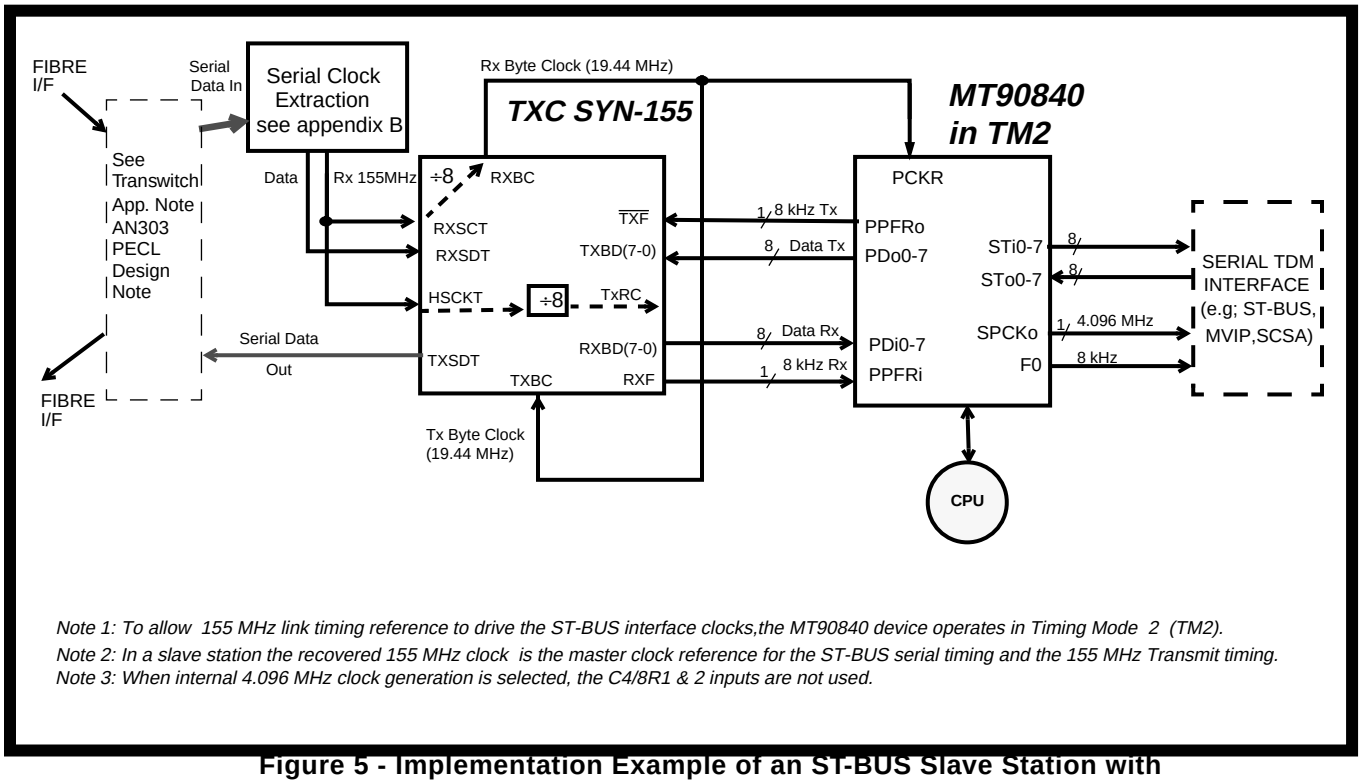
In TM2 operation, the generation of the ST-BUS serial interface 4.096 MHz clock can be done through the utilization of an external reference or from the MT90840 internal clock generator as depicted in figures 4 and 5, respectively. This configuration is valid for 2.048 and 4.096 Mb/s applications. For applications with the ST-BUS interface at 8.192 Mb/s data rates, the 8.192 MHz interface clock has to be provided externally as per figure 6.

At the ST-BUS slave station, the 155 MHz transmit clock to applied to the HSCKT input of the SYN-155 device can be the same recovered 155 MHz from the receive interface (RXSCT input). That will make the entire slave station's time base to be completely slaved from the 155 Mb/s backbone. In applications where parallel data loopback functions are required between PDi0-7 and PDo0-7 lines, the MT90840 performs the loop in approximately 12µs. Parallel data port channels being looped back can be monitored by the CPU in the Receive Path Data Memory (RPDM) or dropped (time interchanged) to the ST-BUS serial interface.



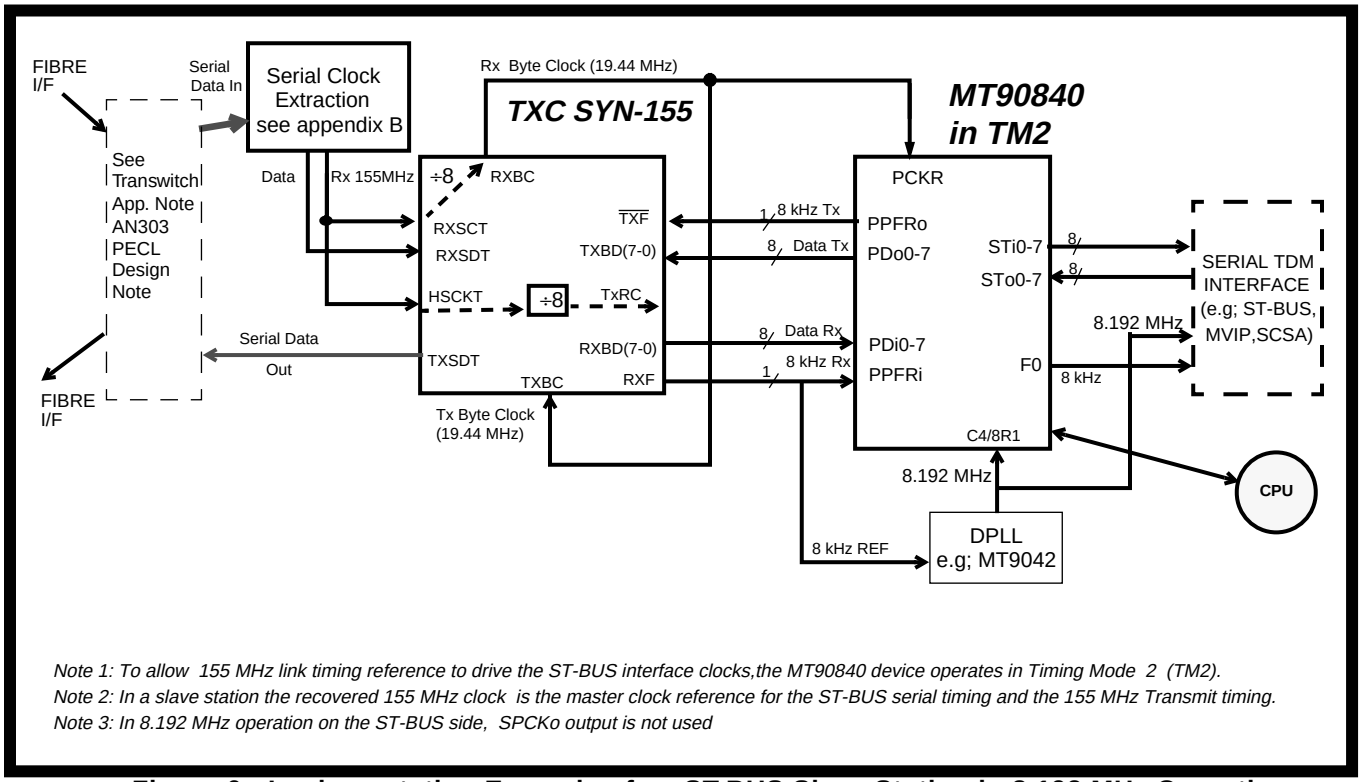
Note 1: To allow 155 MHz link timing reference to drive the ST-BUS interface clocks,the MT90840 device operates in Timing Mode 2 (TM2)
Note 2: In a slave station the recovered 155 MHz clock is the master clock reference for the ST-BUS serial timing and the 155 MHz Transmit timing
Note 3: In TM2, PCKR is used as the main TX and RX Byte interface clock.

Figure 4 - Implementation Example of an ST-BUS Slave Station with External 4.096 MHz Reference



Note 1: To allow 155 MHz link timing reference to drive the ST-BUS interface clocks,the MT90840 device operates in Timing Mode 2 (TM2).
Note 2: In a slave station the recovered 155 MHz clock is the master clock reference for the ST-BUS serial timing and the 155 MHz Transmit timing.
Note 3: When internal 4.096 MHz clock generation is selected, the C4/8R1 & 2 inputs are not used.

Figure 5 - Implementation Example of an ST-BUS Slave Station with Internal 4.096 MHz Generation



Note 1: To allow 155 MHz link timing reference to drive the ST-BUS interface clocks,the MT90840 device operates in Timing Mode 2 (TM2).
Note 2: In a slave station the recovered 155 MHz clock is the master clock reference for the ST-BUS serial timing and the 155 MHz Transmit timing.
Note 3: In 8.192 MHz operation on the ST-BUS side, SPCKo output is not used

Figure 6 - Implementation Example of an ST-BUS Slave Station in 8.192 MHz Operation

Implementing ADD/DROP Functions for MVIP Multi-Chassis Ring Applications

The MT90840 device provides the capabilities necessary for the implementation of add/drop functions in ring architectures. This section gives some hints when implementing dual fiber bi-directional or full duplex rings. The advantage of this architecture is that two fiber links are used in opposite directions providing a total of up to 310 Mb/s of bandwidth available to the stations connected to the rings. The MC-3 interface used for multi-chassis CTI is a typical example of dual ring applications.

The MC-3 Master Station

A master CTI server generates the main backbone's 155 MHz clock which is recovered from the data stream at the other stations connected to the ring (slave stations). The 155 MHz Transmit Clock at the master station is referenced from the ST-BUS (or MVIP) timing signals. The MT90840 device in the master station will operate in Timing Mode 1 (TM1) as previously described and depicted in figure 3. The implementation of the dual ring requires two MT90840 devices connected to two SYN-155C devices as shown in figure 7.

In a multi-chassis implementation, the CTI server interfacing to the WAN has to provide the main clock and the 8 kHz network synchronization references to the 155 Mb/s backbone access card. To facilitate its implementation the MT90840 device can receive the 4.096 MHz and 8 kHz references provided by the MVIP bus. In a ring master station, the MT90840's internal elastic store on the parallel data input port is constantly active in order to absorb the latency built around the ring and to maintain the synchronization on the MVIP Bus side.

In the MC-3 access card, the MT90840 device assigns any channel from the high speed backbone and drops it into the MVIP interface to be then routed

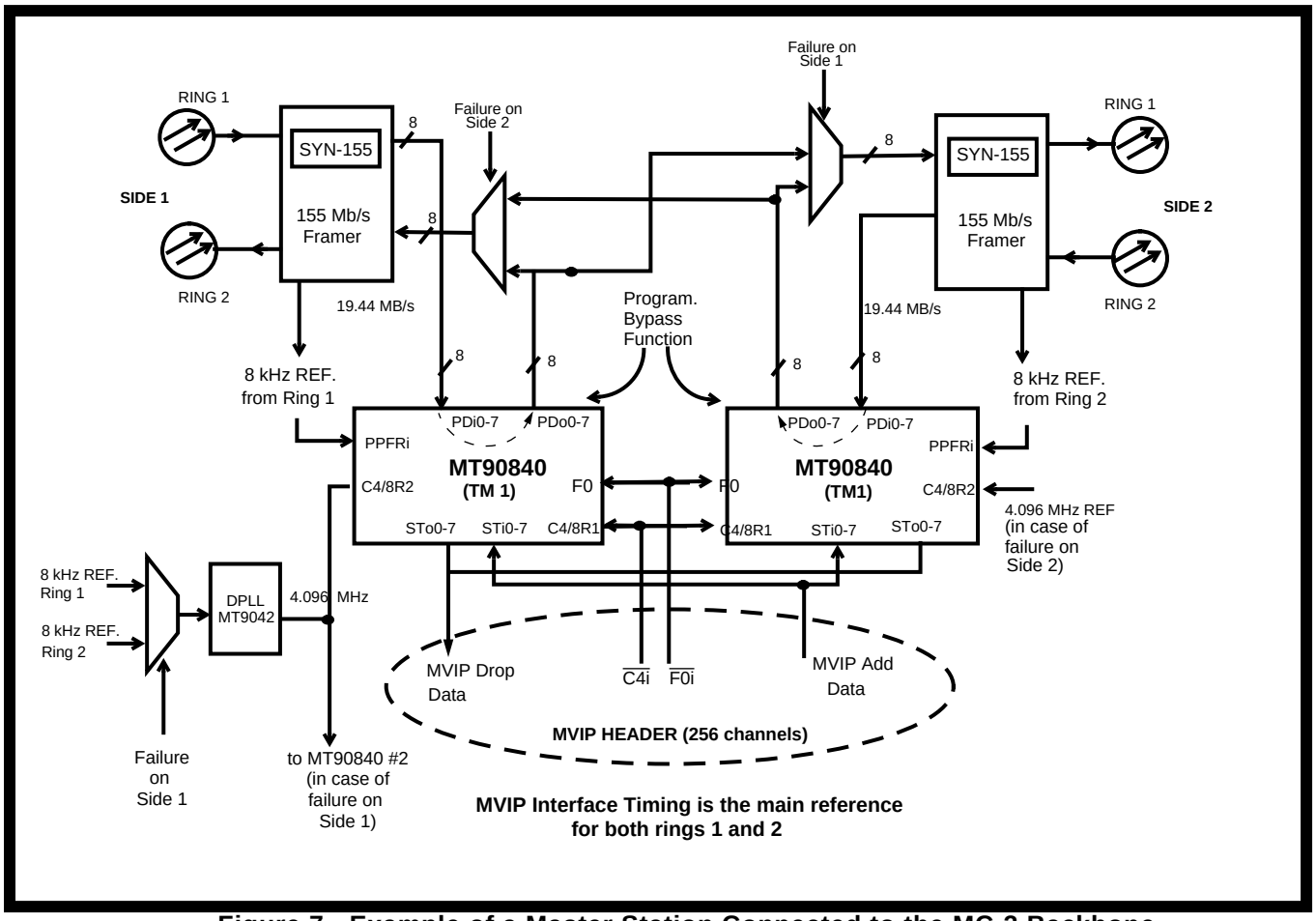


Figure 7 - Example of a Master Station Connected to the MC-3 Backbone (256-Channel add/drop)

to a local media processing card. From the any other local resource card towards the dual ring backbone, the MT90840 can insert any portion of the MVIP bus bandwidth (with a 64 kb/s granularity control) into the payload of the 155 Mb/s frame.

In ring applications, the per-channel "Parallel Data Bypass" is provided to allow all or part of the received input parallel data (PDi0-7) to be bypassed to the output parallel port (PDo0-7) feeding the ring back with the data which is not destined (to be dropped) to the local station. The data destined for the local station can be dropped through CPU programming. When implementing per-channel bypass functions, the CPU has the full control on managing the outgoing bandwidth (from the serial interface to the high speed link) so that it does not contend with the bypassed data.

The MT90840 IC also provides programmable per-channel switching and tri-state control on the MVIP side with a 64kb/s channel granularity. This capability allows the user to avoid contention on any TDM serial link when several cards are accessing the local TDM bus simultaneously. Frame integrity of n x 64 kb/s data is maintained since the MT90840 device provide constant throughput delay when time interchanging channels.

The MC-3 Slave Station

Typically in a slave CTI server the transmitted 155 Mb/s stream is frequency locked to the recovered 155 MHz on the receive direction. This implementation uses a similar clocking approach as previously described in figure 4, i.e., the MT90840 is set in Timing Mode 2 (TM2) and the station's complete time base is derived from the incoming 155 Mb/s link. However in a dual ring application, 2 sets of MT90840 and SYN-155C devices are required to implement a full termination of the two rings. Figure 8 depicts an example of a 155 Mb/s backbone access card within the slave station.

To implement the ADD/DROP function in the slave station, the user selects one of the rings to drive the station's main clock and the 8 kHz phase signals which will control the server's time base. As an example, if ring 1 (R1) is chosen as the master ring, the MT90840 IC locked to R1 provides a phase

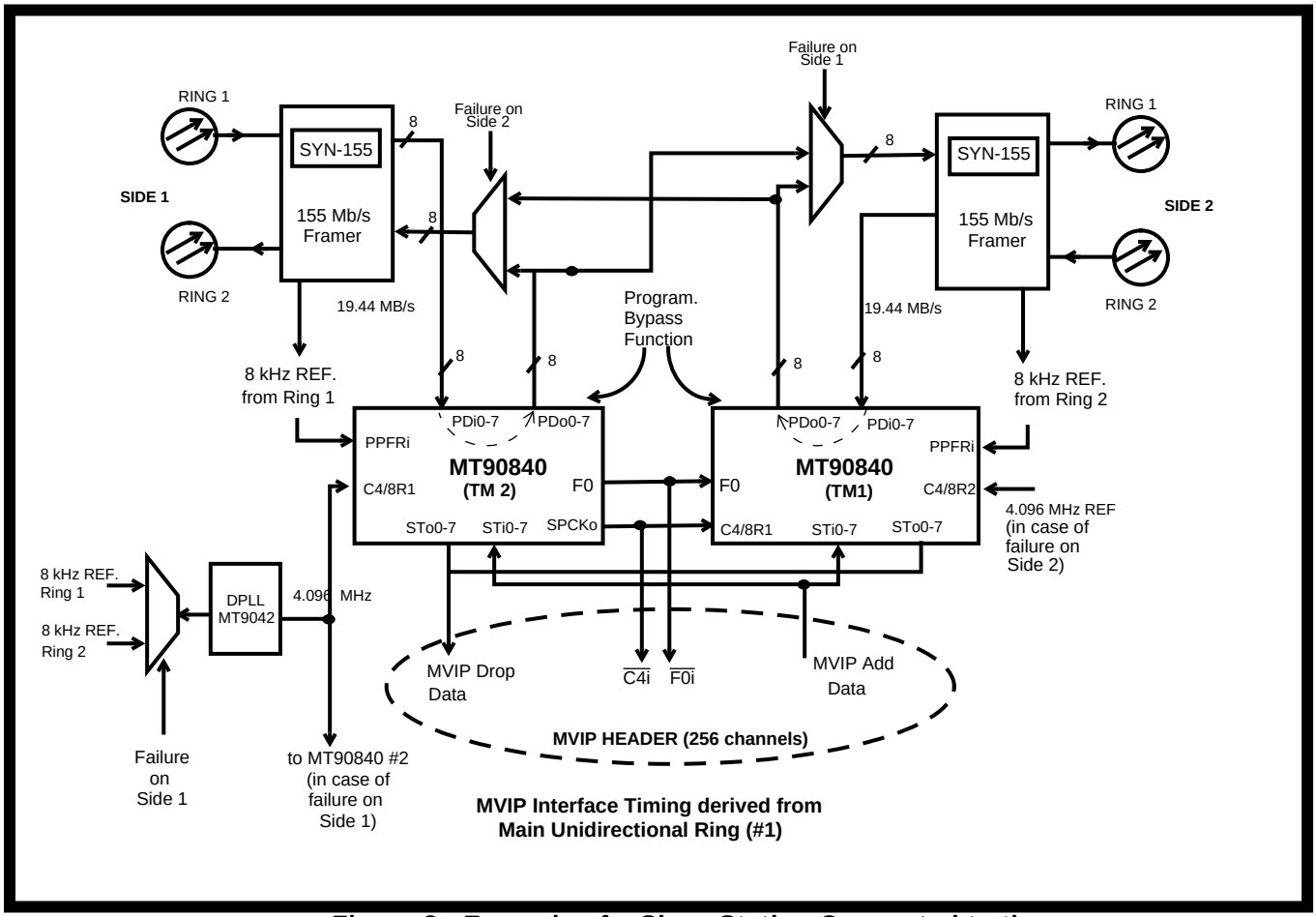


Figure 8 - Example of a Slave Station Connected to the MC-3 Backbone (256-channel add/drop)

control signal to the other MT90840 so that its internal elastic buffer can adjust the phase difference between the two different rings and still maintain the synchronization of the MVIP interface.

In TM2, all the per-channel functions like switching , message mode, bypass and tri-state are available for implementing add/drop functions.

Failures, Loss of Frame and Loss of Sync on the Dual Ring

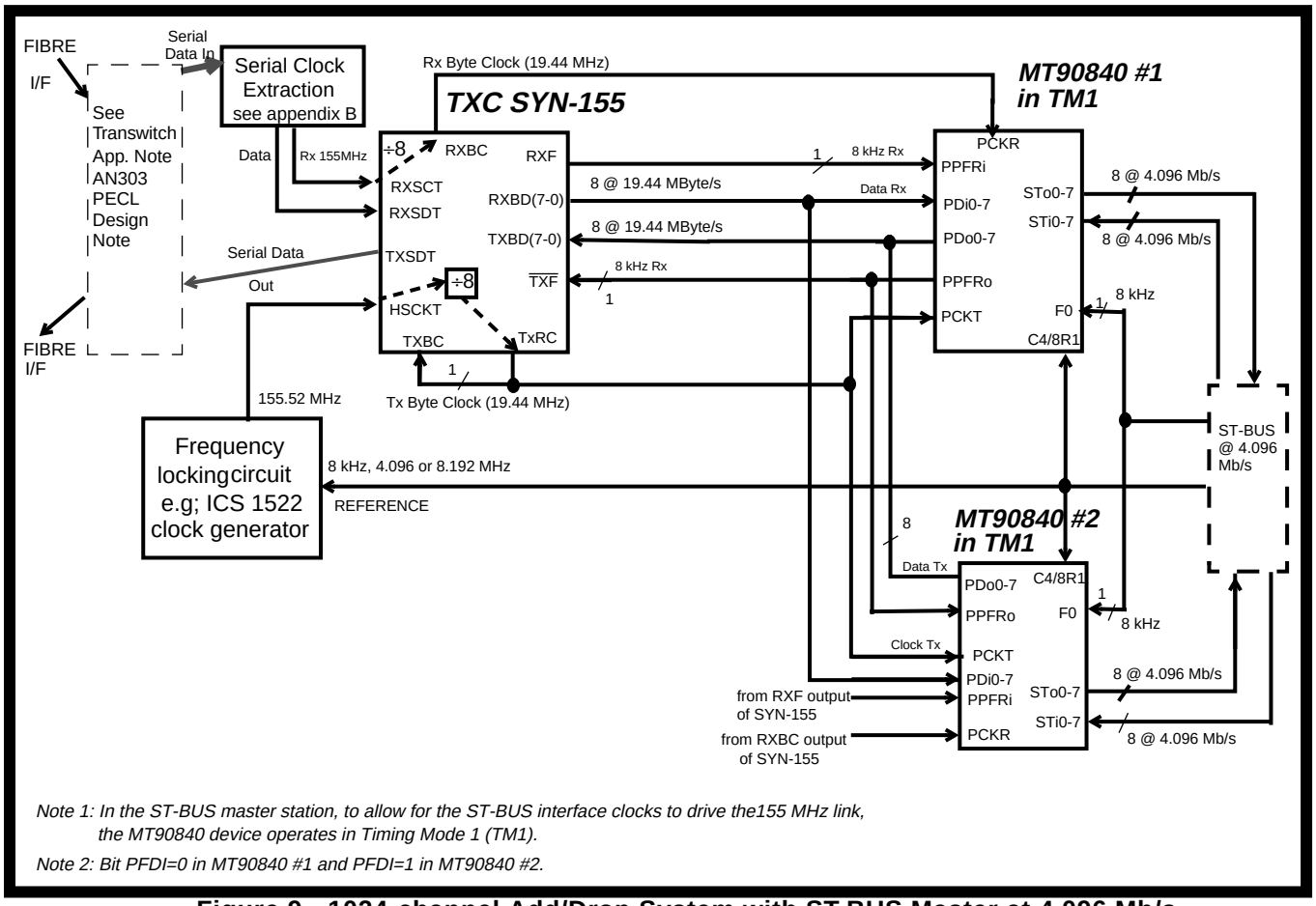
In case of failures, loss of synchronization or loss of frame events in any of the two rings, an alarm is generated by the local SYN-155 device. Upon receiving alarms from the SYN-155, a loop-back can be programmed in the MT90840 device and external muxes to isolate the non-operational station from the rest of the ring. During failure or maintenance procedures, the ring will be unidirectional and the bandwidth is reduced to 155 Mb/s until a CPU command activates the bi-directional operation.

In the dual ring architecture, the two rings (R1 and R2) have different phases on the parallel interface side (PDo0-7 / PDi0-7) due to the round trip delay of each ring to be different at each station. Because the MT90840 ST-BUS interface is always synchronized to a common 8 kHz signal (F0), an elastic store is provided at the parallel interface receive side to absorb the different latencies between R1 and R2 before transferring the data to the ST-BUS side.

Issues on Latency Building around the Ring

When implementing ring architectures using the MT90840 device, some issues regarding data transport latency have to be considered. As mentioned in the section ST-BUS clock master station, the MT90840 in TM1 uses an internal elastic store to adjust the phase difference between the parallel and serial data ports. The utilization of the internal elastic store together with the phase difference between PPFRo and PPFRi caused by the propagation delay over the transmission media do affect the channel bypass latency in the MT90840 device programmed in TM1.

In Timing Mode 1 the per-channel bypass feature is performed within a certain period of time which depends on the off-set between the parallel port input (PPFRi) and output (PPFRo) frame synchronization pulses. The general channel bypass



Note 1: In the ST-BUS master station, to allow for the ST-BUS interface clocks to drive the155 MHz link, the MT90840 device operates in Timing Mode 1 (TM1).

Note 2: Bit PFDI=0 in MT90840 #1 and PFDI=1 in MT90840 #2.

Figure 9 - 1024-channel Add/Drop System with ST-BUS Master at 4.096 Mb/s

delay between PDi0-7 and PDo0-7 corresponds to 125 us + (phase difference between PPFRi and PPFRo) + the elastic store delay (0 or 62.5µs).

In Timing mode 2, since the PPFRi and PPFRo lines have a fixed off-set and the internal elastic store is not used, the channel bypass operation is performed between PDi0-7 and PDo0-7 within 12 µs delay.

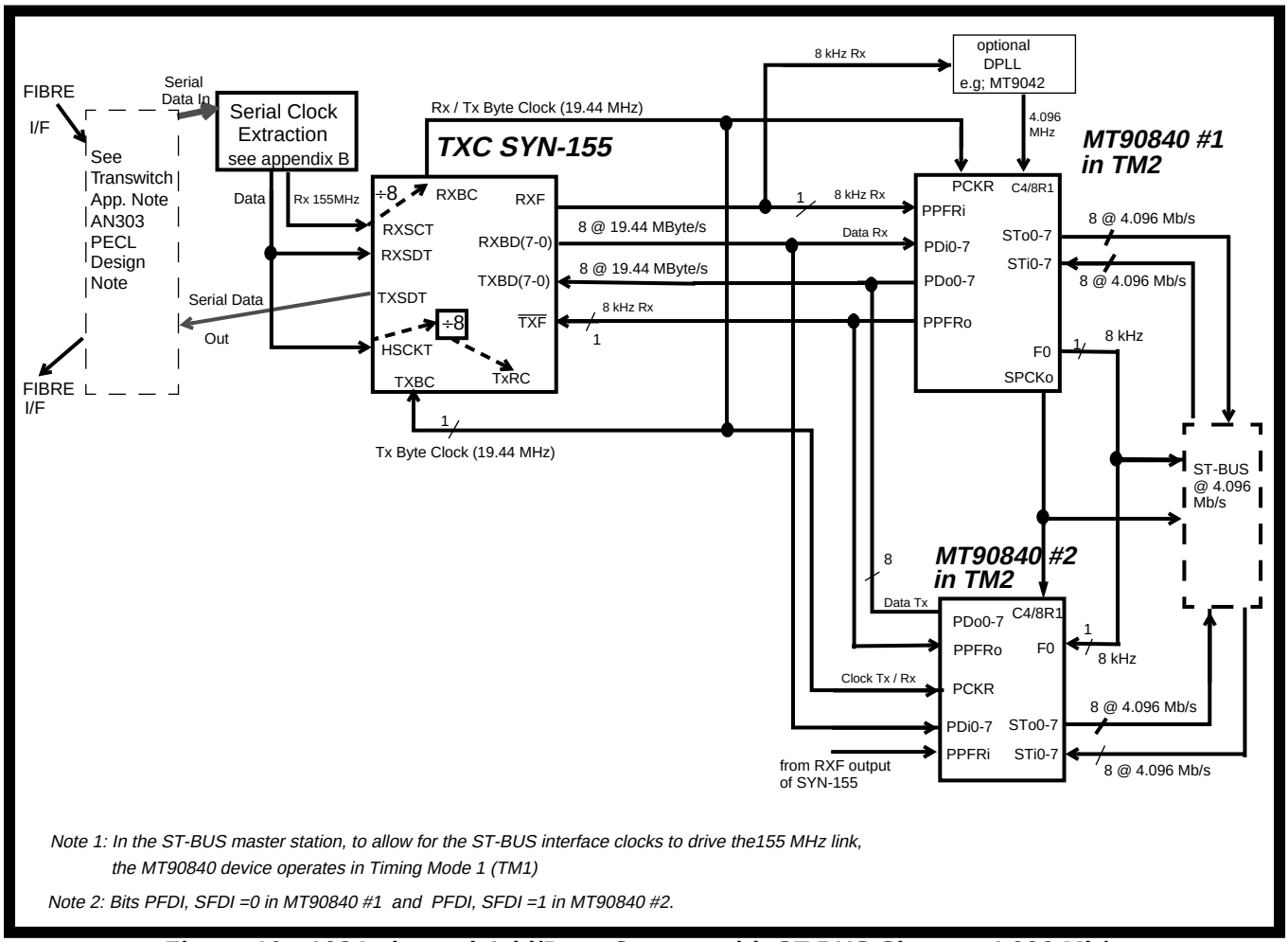
Add/Drop for 8 plus ST-BUS Stream Pairs

For applications requiring more than 16 ST-BUS stream pairs at 2.048 Mb/s, more than 8 stream pairs at 4.096 Mb/s or more than 4 stream pairs at 8.192 Mb/s it is necessary to employ 2 MT90840 devices per-direction. Figures 9 and 10 show an example of a system using 16 stream pairs at 4.096 Mb/s each. Since every stream pair transports 64 time-slots, full-duplex (64 kb/s each) per frame the total add/drop capacity is 1024 of channels.

Bandwidth Sharing Control Feature for point-to-point connections

The MT90840 provides a special feature that eases the implementation of dynamic bandwidth partitioning between isochronous and asynchronous traffic allowing different devices to share a portion of the 155 Mb/s TDM backbone.

This feature is available due to the MT90840's device capabilities to access each 64 kb/s channel on the 155 Mb/s backbone. The internal connection memories on the transmit path (see MT90840 block diagram) are locked to the 155 Mb/s frame on the transmit side. This connection memory can be programmed by the user to generate a transmit enable signal (bandwidth access control) that can be used to control other transmit devices residing in the same board and sharing the parallel bus with the MT90840. The transmit enable signal can be generated over any position of the 155 Mb/s frame with a granularity of 64 kb/s. Four output control lines are provided by the MT90840 device so that more devices can share the 155 Mb/s bandwidth.



Note 1: In the ST-BUS master station, to allow for the ST-BUS interface clocks to drive the155 MHz link, the MT90840 device operates in Timing Mode 1 (TM1)

Note 2: Bits PFDI, SFDI =0 in MT90840 #1 and PFDI, SFDI =1 in MT90840 #2.

Figure 10 - 1024-channel Add/Drop System with ST-BUS Slave at 4.096 Mb/s

During the time that other devices are driving the parallel bus, the MT90840's parallel output port can be placed in high impedance condition (SONET per-channel output enable feature), therefore not contending with the other device data. Figure 9 shows an example of a master station.

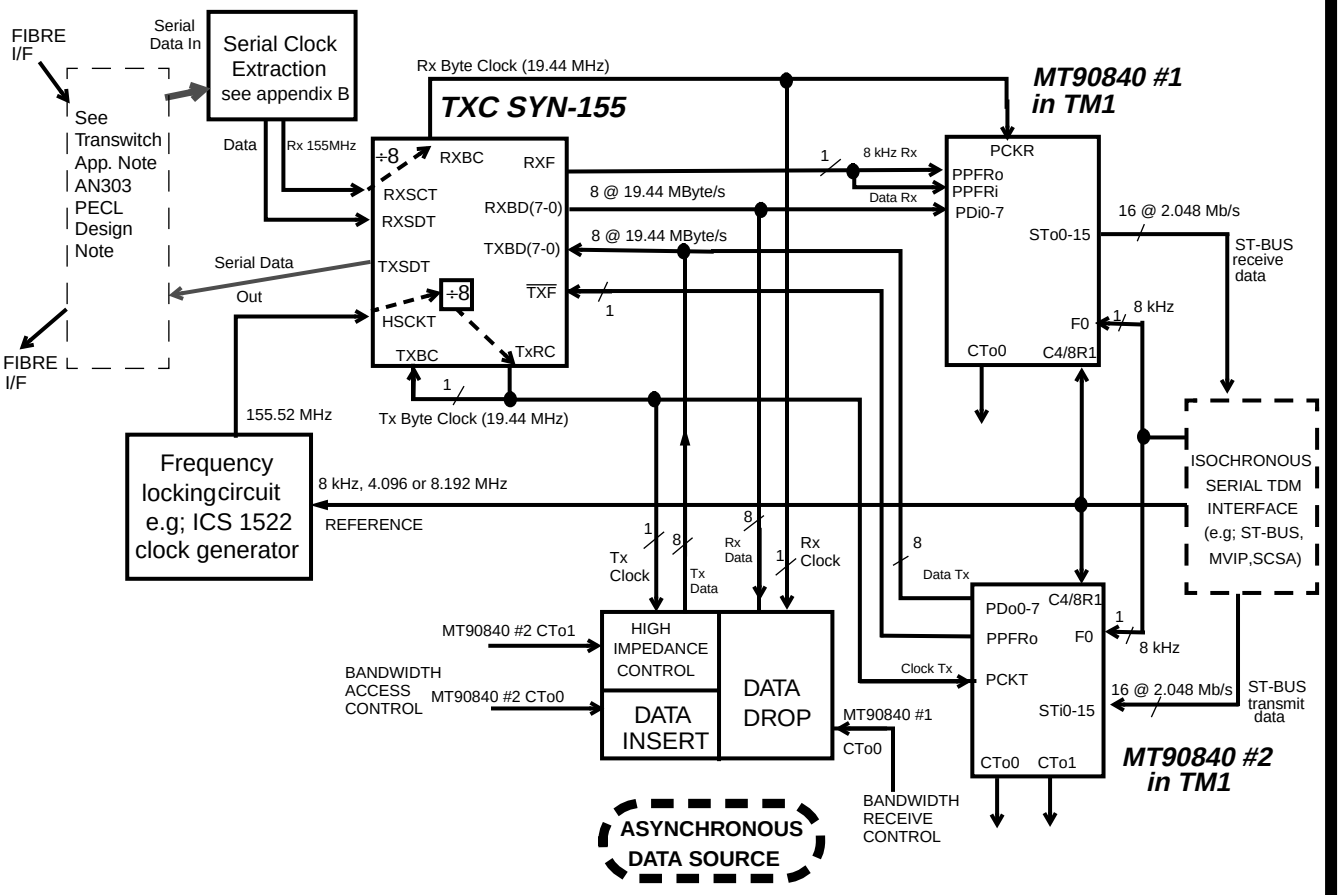
In the example of figure 11, the ST-BUS serial stream interface is operating at 2.048 Mb/s and up to 512 channels can be inserted to or dropped from the 19.44 Mbyte/s interface. This add/drop capacity is generated by utilizing the Full Direction Control feature on the ST-BUS interface side, whereby all 16 serial streams can be programmed on a single direction. This feature is only available when the MT90840 serial port data rate is set to operate at 2.048 Mb/s. In 4.096 or 8.192 Mb/s rates, only streams STi/o 0-7 and STi/o 0-3 can be used respectively, maintaining the 512 channel add/drop capacity.

ST-BUS Clock Master Station

The MT90840 devices in the master station are set to operate in Timing Mode 1, as per figure 11. In the configuration depicted, two MT90840 devices implement an add/drop system of up 512 channels (64kb/s each).

In TM1, the ST-BUS 4.096 MHz clock and the 8 kHz F0 signals are both connected as inputs to the two MT90840 devices. To control the bandwidth utilization of the external asynchronous data device on both transmit and receive directions, the CTo0-1 output lines of the 2 MT90840 can be used.

The CTo0-3 output lines of the MT90840 are synchronized to the internal 2430-position Transmit Path Connection Memory High bits (TPCM High). Since, the TPCM High bits are controlled by the PPFRo (Transmit Parallel Port Frame) signal, it is



Note 1: In the ST-BUS master station, to allow for the ST-BUS interface clocks to drive the155 MHz link, the MT90840 device operates in Timing Mode 1 (TM1)

Note 2: Bit PFDI=0 in MT90840 #1 and PFDI=1 in MT90840 #2.

Figure 11 - Application example: Voice & Data Multiplexing at 155 Mb/s - ST-BUS Clock Master Station

necessary to synchronize the MT90840 #1's PPFRo with the receive 8 kHz signal recovered from the incoming 155 Mb/s interface so that the CTo0-3 output lines of the MT90840 #1 can control the bandwith acquisition at the PDi0-7 lines. To enable the PPFRo line to become an input, the PFDI bit in the TIM register has to be set HIGH.

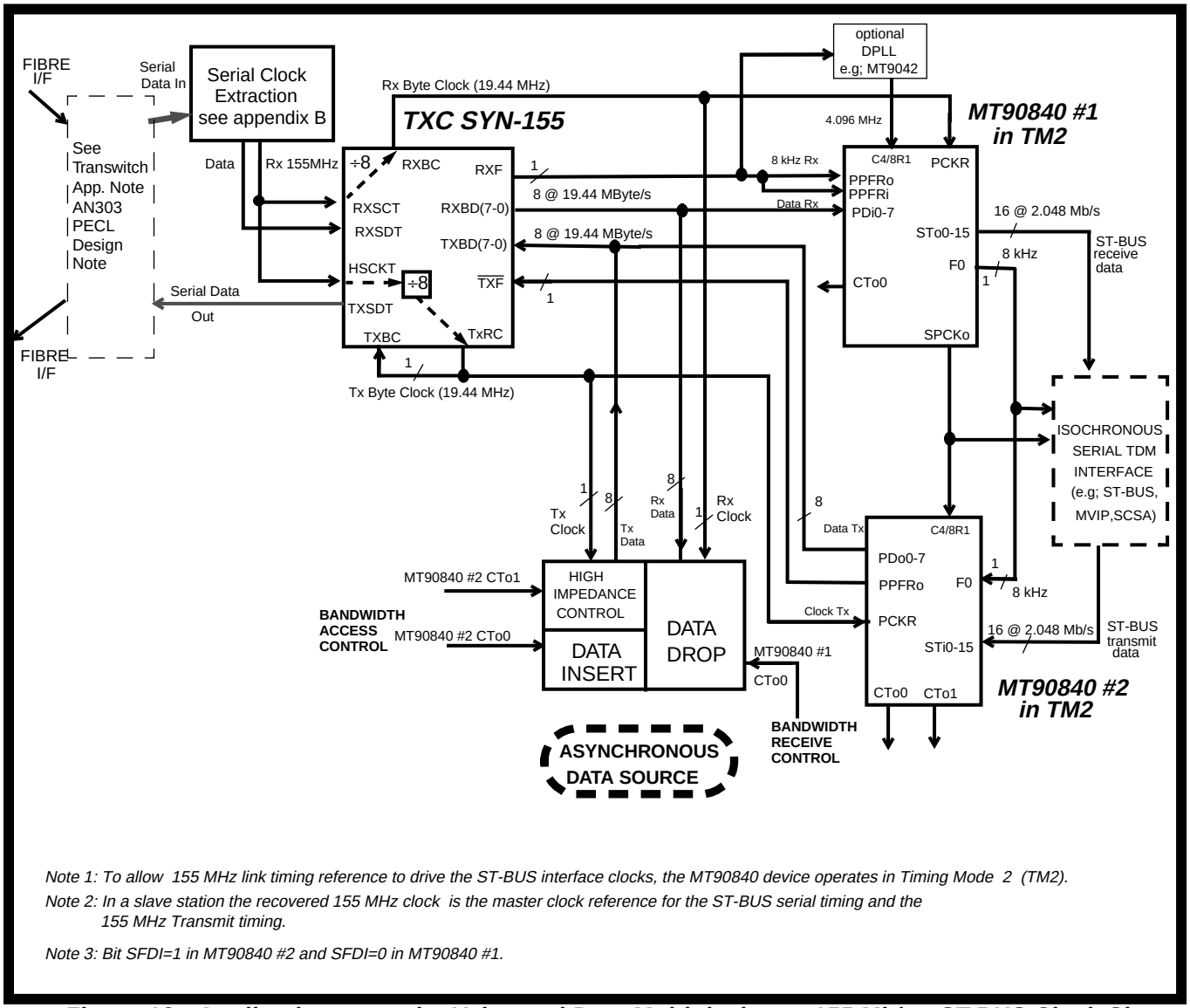
ST-BUS Clock Slave Station (see figure 12)

The bandwidth sharing on an slave station has similar clocking scheme as described earlier in section "Station with ST-BUS Clock Slave operation" and depicted in figure 4. The basic difference here is that 2 MT90840 are required for allowing bandwidth sharing control in both Tx and Rx directions; i.e, the MT90840 #2 operates in Timing Mode 2 and it receives the common F0 reference as an input (SFDI bit = 1). Note that the utilization of the 4.0996 MHz DPLL is optional when 2.048 or 4.096 Mb/s data rates are used. In case of 8.192 Mb/s operation the 8.192 MHz DPLL must be used.

Application for Bandwidth Sharing

As an application example, this multiplexing architecture can be used in some systems where ATM and TDM traffic require a common transport backbone. This is an ideal situation for a system that must deliver voice connectivity and ATM switching in a integrated architecture.

By utilizing the bandwidth sharing control function, specialized intelligent hubs can integrate data and real-time traffic in the same physical TDM transport backbone at 155 Mb/s. Intelligent hubs can be distributed in the enterprise and be able to deliver the voice samples from an end user to the PSTN



Note 1: To allow 155 MHz link timing reference to drive the ST-BUS interface clocks, the MT90840 device operates in Timing Mode 2 (TM2).

Note 2: In a slave station the recovered 155 MHz clock is the master clock reference for the ST-BUS serial timing and the 155 MHz Transmit timing.

Note 3: Bit SFDI=1 in MT90840 #2 and SFDI=0 in MT90840 #1.

Figure 12 - Application example: Voice and Data Multiplexing at 155 Mb/s - ST-BUS Clock Slave Station

interface within the PBX transfer delay requirements. Inside every hub the delay sensitive traffic such as real-time voice is inserted in the optical fiber TDM backbone in its original format through the serial TDM streams. Delay non-sensitive traffic can be transformed into cells and handled by ATM add/drop devices located in every ATM trunk card.

To interface the voice traffic into the PSTN, the intelligent hub drops the voice and the data information from the backbone and distribute both types of traffic to the appropriate switching bus within the hub. The voice traffic is switched by the MT90840 IC to the internal isochronous TDM bus. The ATM traffic is dropped by the ATM address recognition performed at the ATM cell header and sent to the internal Cell Bus (such as the Utopia interface) within the hub .

Once the voice and data traffic are present in the appropriate switching bus in the hub, the voice samples can be switched out to the PSTN through a trunk interface card using T1, E1 or ISDN connectivity. The ATM traffic can be switched out to a public ATM network through ATM trunk interface cards.

The key advantage of Zarlink TDM switches is the ability of offer a complete bandwidth on demand system which allows the user to dynamically assign the required bandwidth for each specific application with 64 kb/s granularity.

APPENDIX A - APPLICABLE DOCUMENTS

1 - Zarlink Semiconductor MT90840 - Distributed Hyper-channel Switch, Data *Sheet, Aug. 1995.*

2 - Transwitch Application Note AN-303 SYN155 Design Note: PECL, TXC02301.

3 - SYN-155C Device, TXC-02302B Data Sheet, September 1994.

4 - ICS 1522 clock generator product preview, Integrated Circuit Systems Inc.

5 - ANSI T1.105-1991, "Digital Hierarchy - Optical Interface Rates and Formats Specifications (SONET)", approved July 02, 1991.

6 - GO-MVIP MC-3 Draft Standard, Oct.95.

7 - ITU Recommendations H.320.

APPENDIX B - VENDOR LIST FOR 155 MHz CLOCK GENERATORS, CLOCK RECOVERY MODULES and FIBRE OPTIC TRANSCEIVERS

Company Name	Phone # Fax #
VECTRON LABS INC, USA	203-853-4433 203-849-1423
TEXAS INSTRUMENTS, USA	512-250-6769
INTEGRATED CIRCUIT SYSTEMS INC. (ICS), USA	610-630-5300 610-630-5399
ANALOG DEVICES, USA	617-329-4700 617-326-8703
MOTOROLA SEMI, USA	602-994-6561
SIEMENS, USA	800-827-1606 201-890-1610
AMCC, USA	619-450-9333 619-450-9885
CYPRESS, USA	408-943-2600
TRIQUINT, USA	408-982-0900 408-982-0222

FIBRE OPTICS TRANSCEIVERS

Company Name	Phone #
HEWLET PACKARD	800-235-0312
BT & D	302-479-0300
O C P	818-701-0164
SIEMENS	800-827-3334

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