Application Note **MSAN-196**

H.110 Timing Signal Requirements

H.110 Compliance Check List

AN5783 Issue 2 October 2002

Contents

1.0 Introduction

2.0 Description

3.0 Hot Swap

4.0 H.110 Core Signal Check List

5.0 H.110 Inter-operability Signal Check List

1.0 Introduction

This application note illustrates the compliance of the MT90866, Flexible Digital Switch with H.110 Interface, with respect to the H.110 Hardware Compatibility Specification: CT Bus.

2.0 Description

The MT90866 Switch provides 4096 x 2432 channel blocking switch capabilities between backplane and local streams, conforming to the H.110 Hardware Compatibility Specification: CT Bus standard. The H.110 specification is designed on a board level scale so it would be impractical to implement all of the characteristics into a single chip. The most important aspects of the H.110 specification, such as the timing characteristics and hot swap capabilities, are the main focus of this note. The MT90866 meets all of the key H.110 timing signal requirements. The DPLL of the MT90866 provides a holdover mode and MTIE circuit with maximum time interval error of less than 21ηs per reference switching which allow seamless transition between the primary and secondary clock inputs.

3.0 Hot Swap

Each CT Bus data line and CT_NETREF must have a 24Ω series termination resistor. These resistors must be provided on the card and should be placed as close as possible to the connector. The data and clock line terminations are not built into the MT90866. For further information about hot swap refer to the application note MSAN-191 on the Zarlink Semiconductor web site (www.zarlink.com).

4.0 H.110 Core Signal Check List

Core Signals Required	Provided by the MT90866?	Description
/CT_FRAME_A	Provided	• Driven by the “A” master clock • Negative true pulse • 122ηS wide straddling the beginning of the first bit of the first time-slot • Period of 125μS
CT_C8_A	Provided	• Driven by the “A” master clock • Frequency of 8.192MHz • Duty cycle of 50%
/CT_FRAME_B	Provided	• Redundant Frame Sync • Driven by the “B” master clock • Negative true pulse • 122ηS wide straddling the beginning of the first bit of the first time-slot • Period of 125μS
CT_C8_B	Provided	• Redundant Bit Clock • Driven by the “B” master clock • Frequency of 8.192MHz • Duty cycle of 50%
CT_D[0...31]	Provided	• Serial data lines can be driven by any board in the system • 32 signals contain 128 time-slots per frame at a clock frequency of 8.192MHz
CT-NETREF_1	Provided	• Any duty cycle • Period is 125μS, 647ηS or 488ηS and is synchronous • Minimum high time of 90ηS and a minimum low time of 90ηS
CT-NETREF_2	Provided	• Any duty cycle • Period is 125μS, 647ηS or 488ηS and is synchronous • Minimum high time of 90ηS and a minimum low time of 90ηS
/CT_EN	Provided	• Signal to represent that J4 of the CT Bus is fully seated
/CT_RESET	Provided	• Used to reset all CT Bus cards that do not have access to PCI RST# reset from J1/P1

5.0 H.110 Inter-operability Signal Check List

Inter-operability Signals Required	Provided by the MT90866	Description
/FR_COMP	Provided (See Note 1)	• Driven by current clock master • Negative true pulse • 122ηS wise straddling the first bit of the first time-slot • Period of 125μS
SCLK	Provided (See Note 2)	• Driven by current clock master • Frequency is 8.192MHz • Positive going edge indicates the beginning of the bit
SCLK_D	Provided with minimal hardware addition (See Note 3)	• Driven by current clock master • Frequency is 8.192MHz • Positive going edge indicates the beginning of the bit

The MT90866 provides the clocks for the CTbus, not the SCbus. These SCbus signals are known as Inter-operability Signals. The following is section 1.5.2 from the H.110 Hardware Compatibility Specification:

"Inter-operability signals MUST be implemented by all bus master-capable cards but are present only to aid inter-operation with ANSI VITA 6, SCbus."

Note 1: The /FR_COMP signal is the exact same signal as the /CT_FRAME signal and can thus be driven directly by the /CT_FRAME.

Note 2: The SCLK signal is the exact same signal as the CT_C8 signal and can thus be driven directly by the CT_C8.

Note 3: The SCLK_D signal is a delayed version of the SCLK (the specification states that there is between 86.5ηS and 96.5ηS between the rising edge of the CT_C8 and SCLK_D clocks). This clock needs to be generated using the CT_C8 output and a delay circuit. This can be created with an FPGA or a simple delay circuit added to the SCLK signal.

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE