ZL30160

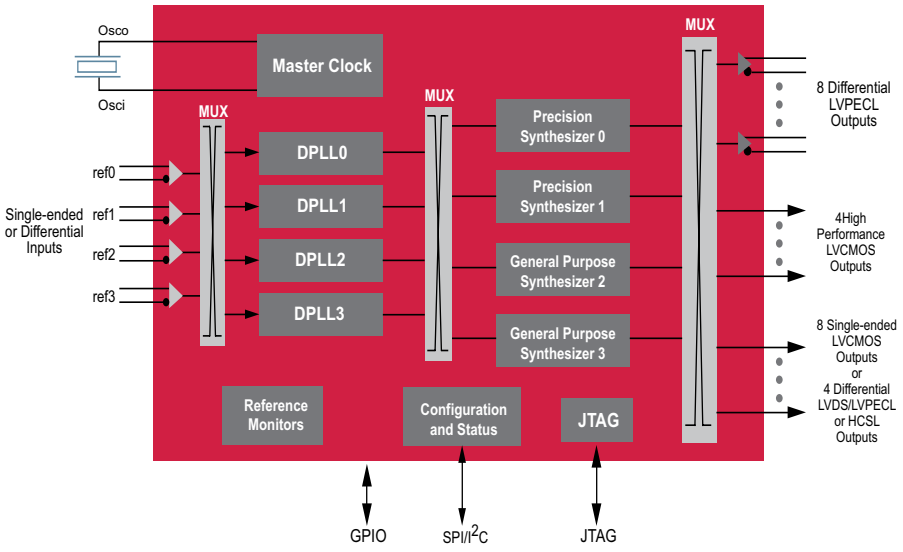
Product Preview

FOUR-CHANNEL UNIVERSAL CLOCK TRANSLATOR

The ZL30160 Four Channel Universal Clock Translator, part of Microsemi's ClockCenter platform of Synchronous Clock devices, delivers industry-leading synchronization performance for high-speed, complex applications. The highly integrated and programmable solution provides translation from any input reference frequency to any output clock frequency with jitter performance that can directly drive 10G PHY devices.

The ZL30160 integrates four independent digital PLLs, accepts four input references and generates 20 programmable clock outputs. The highly integrated solution allows designers to replace multiple components with a single chip, simplifying design and reducing component count and power.

ZL30160 Block Diagram



Applications

- 10 Gigabit line cards
- Synchronous Ethernet including 10GBASE-R and 10GBASE-W
- OTN multiplexers and transponders
- SONET/SDH, Fibre Channel, XAUI

Availability and Support

The ZL30160 Four Channel Universal Clock Translator is in volume production. To learn more about the ClockCenter platform, visit http://www.zarlink.com/zarlink/hs/timing_ClockCenter.htm. Full information is available to registered MyZarlink users. To register for a MyZarlink account, visit http://www.zarlink.com/zarlink/hs/login.htm.

Single-Chip Solution for Complex, High-Speed Applications

The industry's highest performance, most integrated timing solution for complex, high-speed applications.

Reduces design complexity and cost

- Device operates from a single crystal resonator or clock oscillator

Highest Performance Solution Available

- Four independent clock channels
- Programmable synthesizers generate any clock rate from 1 kHz to 720 MHz
- Two precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10G PHYs
- Two general purpose synthesizers generate a wide range of digital bus clocks
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 720 MHz
- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Eight LVPECL outputs and four LVCMOS outputs
- Eight outputs configurable as LVCMOS or four differential LVDS/LVPECL/HCSL

Unparalleled Flexibility

- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Four reference inputs configurable as single ended or differential

Fully Programmable

- Dynamically configurable via simple SPI/I²C interface

Microsemi

ZL30160

10G Synchronous Ethernet Card With Recovered Clock Rate

A high level of integration coupled with unique frequency translation flexibility sets the ClockCenter ZL30160 Four Channel Universal Clock Translator apart from any other synchronous timing solution available today.

The single chip device simplifies high-speed, complex synchronous applications by integrating four independent narrow band digital PLLs and a unique two-stage architecture that supports any rate to any rate frequency translation between four input references and up to twenty programmable output clocks. Alternate approaches require multiple components to implement a similar timing solution offered by a single ZL30160 product.

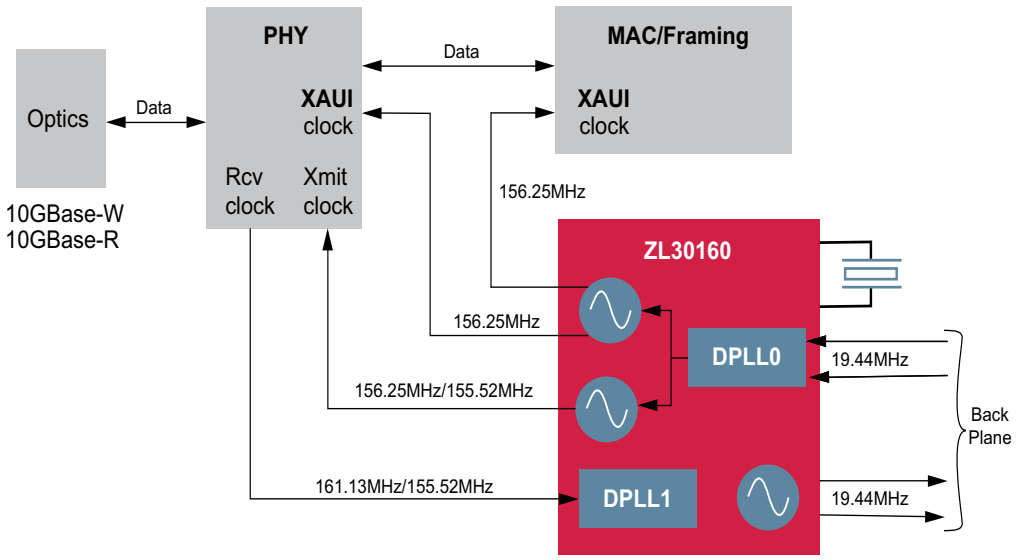
The ZL30160 can accept up to four, single-ended or differential input references of any frequency between 1 kHz and 720 MHz. Four integrated narrowband digital PLLs enable the device to accept low frequency input references and provide improved filtering for up to four independent timing paths. Output clock frequencies are independently defined from input references, allowing for generation of any frequency between 1 kHz and 720 MHz.

The application diagram illustrates how the ClockCenter ZL30160 can be implemented as a single-chip solution in a complex 10G Synchronous Ethernet design. This implementation also allows flexibility to dynamically configure this design to support 10GBASE-W or 10GBASE-R functionality.

In this application, the ClockCenter ZL30160 is used to support independent transmit and receive timing paths. The transmit side is comprised of DPLL0 and both Synthesizer 0 and 1. The device accepts two 19.44 Mhz input references from the system backplane. These references are fed through DPLL0 to Synthesizer 0 and 1. Synthesizer 0 is used to generate a 156.25 MHz XAUI clock for the MAC and the PHY. Synthesizer 1 generates a 156.25 MHz or 155.52 MHz transmit clock for the PHY. The ZL30160 can be dynamically configured and reconfigured to support either frequency for 10GBASE-R or 10GBASE-W implementations.

The receive path accepts a third input reference which is recovered from the line side, performs rate conversion, and provides this clock to the backplane. In this case the ZL30160 can accept either 161.13 MHz or 155.52 MHz, as an input reference. The input frequency can be dynamically configured and reconfigured to support 10GBASE-R or 10GBASE-W implementations. This high-speed input reference is translated to the 19.44 MHz output clock frequency required for the system backplane.

The ZL30160 can also perform hitless reference switching when needed in this application. This capability, combined with the integration of multiple PLLs and synthesizers, any rate frequency translation, jitter filtering and low jitter generation makes the device an ideal single-chip solution for high-speed timing applications.



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