CONVERTING SG1524 SWITCHING POWER SUPPLY DESIGNS TO THE SG1524B

INTRODUCTION

Many power control engineers have designed successful switching power supplies around the SG1524 Pulse Width Modulator integrated circuit. This application note explains the differences between this earlier device and the more sophisticated SG1524B. While the functional pinouts are identical for the two devices, there are some distinct operational differences which the user should be aware of when designing new supplies or when updating an existing design. In many cases, design changes are minimal (such as adjustment of frequency compensation) or not required at all. At the same time the improvements in control architecture and circuit design of the SG1524B allow the designer to obtain levels of performance in new power supply designs not possible with the older device.

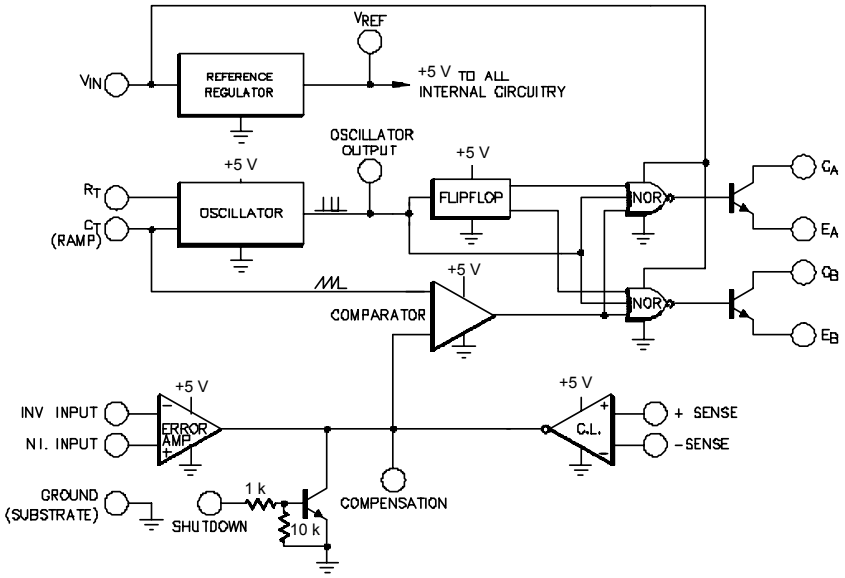


Figure 1. SG1524 Block Diagram

GENERAL COMPARISION

Figures 1 and 2 show respectively the block diagrams of the SG1524 and the SG1524B. Both devices were designed for voltage-mode control, but both can be used to implement current-mode control as well with the addition of an external dual op-amp. For further details see the Microsemi Application Note “Current Mode Control with the SG1524B.”

The main functional difference between the two circuits is in the action of the shutdown pin. In the SG1524, a voltage at Pin 10 greater than +0.7 volts will turn on an internal transistor which pulls the error amplifier output to ground. In the SG1524B, a voltage greater than +1.2 volts at Pin 10 activates a logic gate which inhibits the pulse output of the PWM comparator. The error amplifier output voltage is not affected directly.

Other improvements include the addition of an undervoltage lockout function and fault suppression logic. These provide protection against inadequate supply voltage to the control IC and ensure constant frequency alternating output pulses to the power devices.

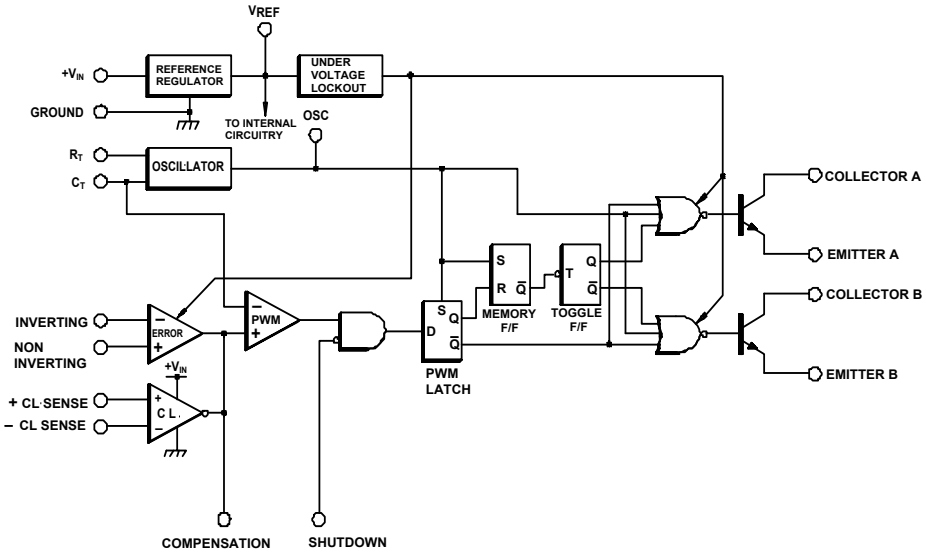


Figure 2. SG1524B Block Diagram

INDIVIDUAL SECTION DIFFERENCES

VOLTAGE REFERENCE

The voltage reference is a low-drift bandgap design which provides a precision +5.0 volt reference for the control loop. Initial accuracy is ±1% for the SG1524B/2524B, and ±2% for the SG3524B. This is a factor of four improvement over the original reference. Line regulation is typically better by a factor of 3 (3 mV instead of 10 mV). Load regulation is better by a factor of 4 (5 mV rather than 20 mV). The temperature coefficient is also lower and more uniform from device to device. All these features translate directly into tighter tolerances on the switcher output voltage. At 25°C the differential drop across the regulator is only 1.2 volts, as opposed to 2.7 volts for the SG1524. Figure 3 shows the relationship between V_{IN} and V_{REF} for both devices. As a result, the SG1524B is fully functional with a 6.2 volt supply. Under worse case conditions of I_{LOAD} = 20 mA and T_A = -55°C, all devices also guaranteed to function at V_{IN} = 7 volts.

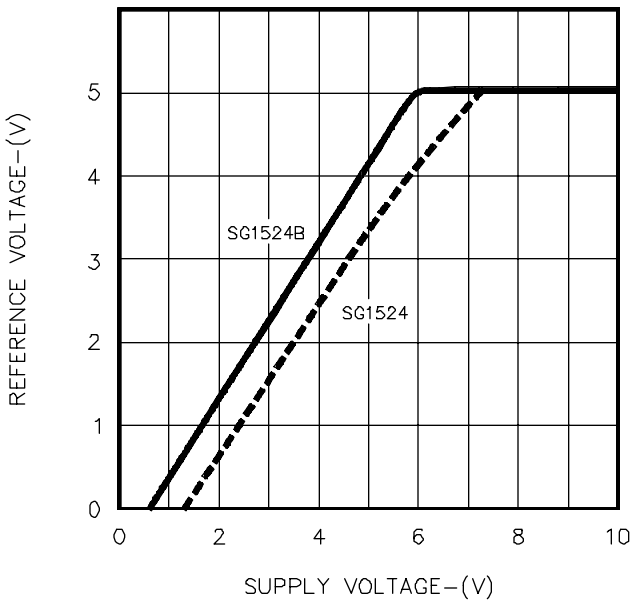


Figure 3. Reference Voltage vs. Supply Voltage

UNDERVOLTAGE LOCKOUT

This circuit has two sections: a controlled current source which forces the error amp low and the output transistors off, and a bandgap comparator which overrides the lockout source. The current source is fully active when V_{IN} is +1.2 volts. Since the error amp and output driver cannot function until V_{IN} is approximately 3 volts, it is impossible for spurious output pulses to occur when the supply voltage is too low for normal operation.

The bandgap comparator monitors the reference voltage. It enables the SG1524B when the reference rises to +4.3 volts. This arrangement allows operation from a +5 volt ±5% supply by connecting V_{IN} and V_{REF} together.

The action of the undervoltage lockout can be observed with the test circuit of Figure 4. A 100 k pull-up resistor is connected from Compensation to V_{IN}. V_{IN} is swept from 0 to +6.5 volts with 5 Hz triangle waveform from a function generator. An oscilloscope in XY Mode displaying V_{IN} horizontally and Compensation vertically will generate the display shown in Figure 5.

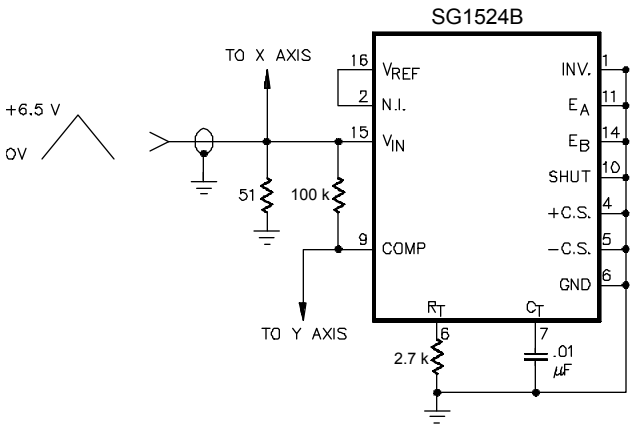


Figure 4. Undervoltage Lockout Test Circuit

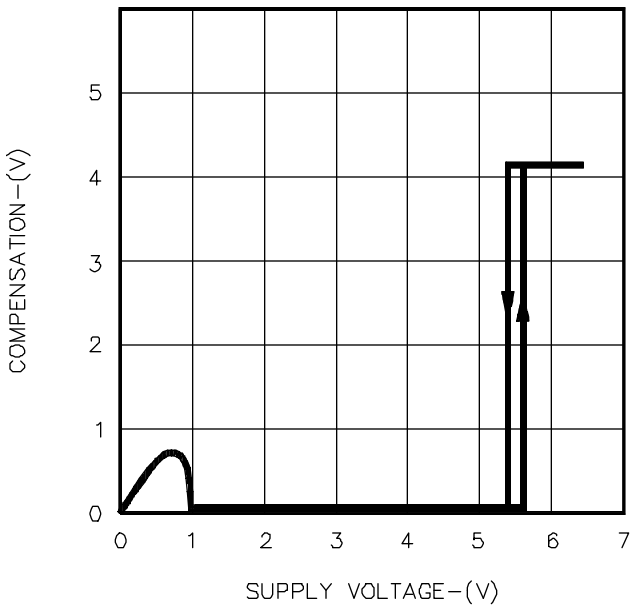


Figure 5 - Undervoltage Lockout At The Error Amp

As V_{IN} slowly sweeps from 0 to 1 volt, the lockout current source becomes active and pulls the error amp to ground, guaranteeing 0% duty cycle from the controller. From 1 volt to approximately 5.5 volts the controller is inhibited while the internal circuitry stabilizes. At 5.5 volts the bandgap comparator overrides the lockout current, releasing the output of the error amp. The reverse portion of the voltage sweep is identical, except that approximately 200 mV of hysteresis can be observed at the comparator trip point.

OSCILLATOR

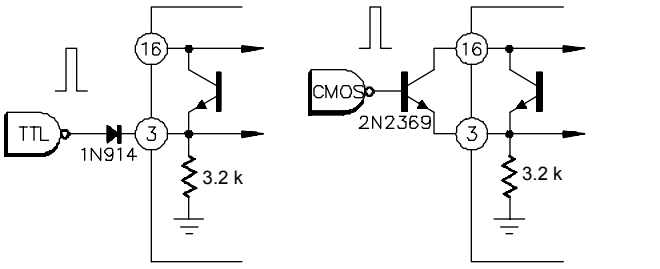
The oscillator of the SG1524B is programmed for frequency with an external R_T and C_T in the same manner as the SG1524. Both initial accuracy and temperature coefficient have been improved with the "B" version.

There are two methods to synchronize multiple units together.

A. Program master unit with R_T and C_T for the desired frequency. Connect the Ct terminal (Pin 7) of the master to the Ct terminal of the slave. Connect the OSC terminal (Pin 3) of the master to the OSC terminal of the slave. Leave the slave R_T terminal (Pin 6) open or tied to the reference. This is the recommended approach if the PWM controllers are close together (on the same printed circuit board and within six inches of each other).

B. Program a master unit for the desired frequency. Select R_T and C_T for the slave units such that they free-run at a frequency 10% slower than the master. Connect all the oscillator terminals together. This method is recommended if the PWM controllers are not close together, since it avoids routing a high impedance line (C_T) around a noisy environment.

To synchronize one or more devices to an external clock frequency, one of the connections shown in Figure 6 should be used. The device(s) to be synchronized should free-run 10% slower than the clock. Pulse width of the external clock should be at least 200 ns, but not longer than the desired deadtime.

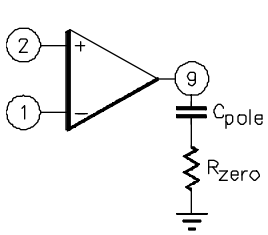


A. TTL LOGIC B. 5 VOLT CMOS LOGIC

Figure 6. Oscillator Sync to an External Clock

ERROR AMPLIFIER

The error amplifier of the SG1524B is, like its predecessor, a transconductance design with an output impedance of approximately 4 MΩ. This allows use of external clamp circuitry to obtain soft-start and duty cycle limit, as on the original 1524. Since all the voltage gain takes place at the output pin, open-loop gain/frequency characteristics are easily controlled by shunt reactance from Pin 9 to ground (Figure 7). Also, this type of amplifier has a very predictable 1/T variation of open-loop gain with absolute temperature as shown in Figure 8.



$$f_{pole} = \frac{1}{2\pi R_O C_{pole}}$$

where R_O = Output Impedance $= 4 \times 10^6 \Omega$

$$f_{zero} = \frac{1}{2\pi R_{zero} C_{pole}}$$

where $C_{pole} >> C_O$ 120 pF

and $R_{zero} << R_O$

Figure 7. Frequency Compensation of the Error Amplifier

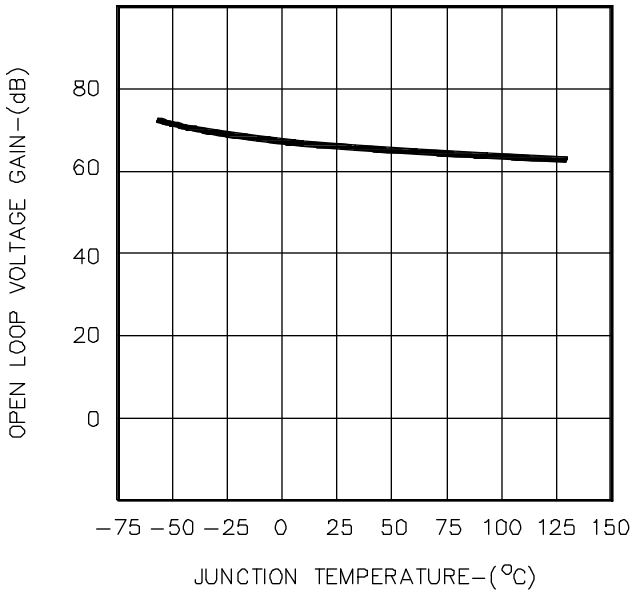


Figure 8. Open Loop Gain vs. Temperature

The input common mode range is +2.3 to +5.2 volts, so that existing designs at +2.5 volts will function with no modifications. For new designs the +5 volt reference may be applied directly to the non-inverting input, eliminating the necessity for two divider resistors.

Since the lower common mode limit is +2.3 volts for the SG1524B and +1.8 volts for the SG1524, neither amplifier

should ever be used in the non-inverting unity-gain configuration shown in Figure 9. The error voltage must swing down to +0.5 volts to guarantee 0% duty cycle from the pulse width modulator, and this violates the common mode range specification.

In general, any frequency compensation for the voltage control loop which works with the SG1524 can also be used with the SG1524B with no modification.

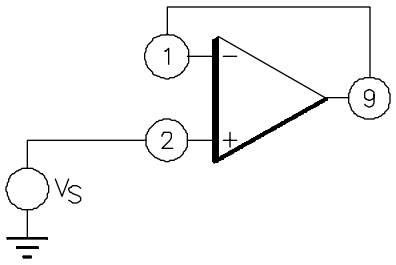


Figure 9. Non-Inverting Unity-Gain Connection
(Not Recommended)

CURRENT LIMIT AMPLIFIER

The current limit amplifier of the SG1524B is one of the most significant areas of change from an applications viewpoint. Like the original circuit, there is a fixed 200 mV threshold designed into Pins 4 and 5 to permit direct sensing across a current sampling resistor. Differences in the “B” circuit affect the input bias current, allowable common mode range, and stability in current-limit.

INPUT BIAS CURRENT

In the SG1524, there is a constant 130 µA flowing out of Pin 4, while the current out of Pin 5 is variable from 0 to 100 µA depending on the differential input voltage. Because of this characteristic, the current limit sense terminals must be driven from source impedances less than 20 Ω to avoid modulating the current limit threshold. The “B” device features bias currents which are identical at each pin, are independent of current sense voltage, and are a factor of 10 lower. This allows predictable foldback current limiting without wasteful low-resistance divider networks.

COMMON MODE RANGE

The guaranteed common mode range of the current sense inputs is 0 volts to V_{IN} -2.5 volts. Current sensing in a supply ground line is possible, but the configuration of Figure 10 should be used to avoid damaging the IC. The 100 Ω resistor is required because of delays through the controller and storage time in any bipolar device. The SG1524B will reduce the pulse width as Pin 5 is driven 200 mV below ground, but in practice it is overdriven due to the aforementioned delays. If Pin 5 is driven below -0.3 V at T_A = +125°C the substrate diode will conduct. The 100 Ω resistor will limit the peak substrate current to a safe

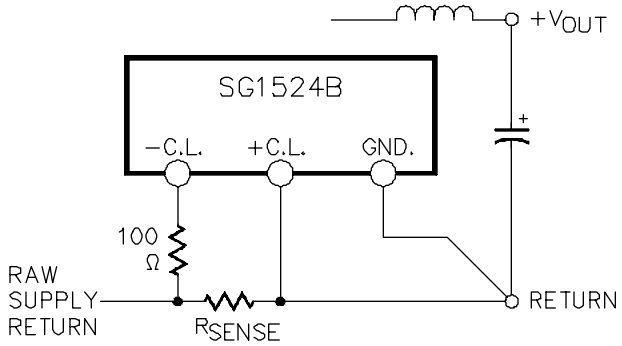


Figure 10. Current Sensing in the Ground Line

value without shifting the C.L. threshold.

Current sensing may also be accomplished with a common emitter or source resistor to ground as shown in Figure 11; or it may be placed in the supply output line, as indicated in Figure 12. At -55°C the value of V_{IN} must be at least 2.5 volts greater than the switcher output voltage.

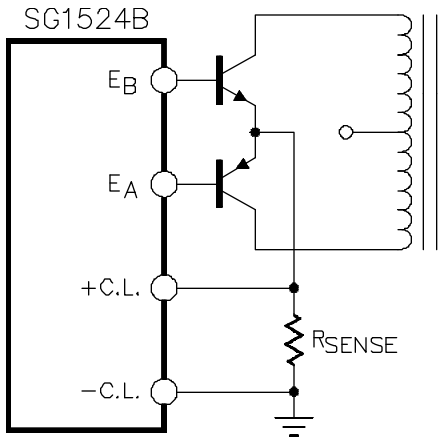


Figure 11. Sensing Primary Current With an Emitter Resistor

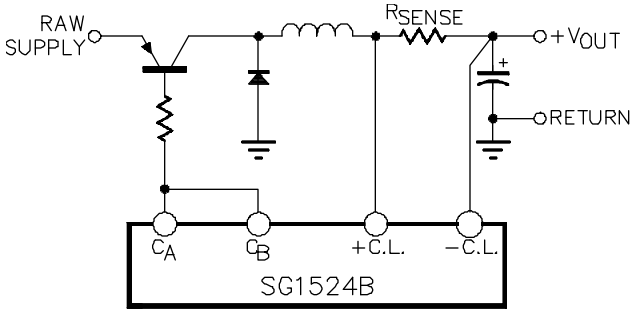


Figure 12. Current Sensing in the Output Line

FREQUENCY COMPENSATION

The original SG1524 current limit amplifier had a typical open loop gain of 44 dB and was internally compensated to produce a single-pole rolloff above 300 Hz. The SG1524B exhibits 75 dB of gain and has no internal compensation. The circuit may be used as a moderate speed comparator, or it may be used as an analog gain block to override the error amplifier.

Because of the higher gain and bandwidth, designers may find that the control loop will oscillate when the supply goes into current limiting. The cure is to add frequency compensation externally to the current limit circuit or to rework the existing voltage loop compensation. See the Microsemi Application Note "A New, Versatile PWM Control Circuit for Switching Power Supplies."

SHUTDOWN

The shutdown circuit of the "B" is illustrated in Figure 13. It has the following differences compared to the 1524:

A. Logic threshold is +1.2 volts instead of +0.7 volts for compatibility with TTL logic and improved noise immunity.

B. Input current is very low (usually under 100 µA) even at +5 volts input. The pin may be driven directly from TTL logic (all families) to TTL-output comparators.

C. Response time is very fast, between 35 and 100 ns depending on output transistor loading.

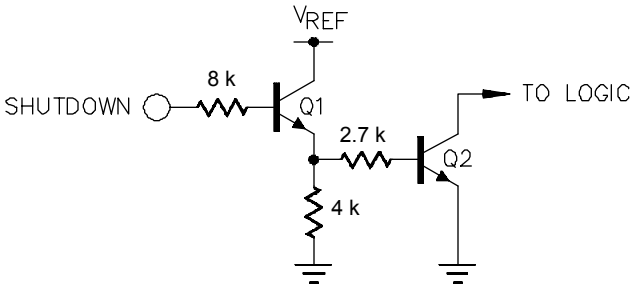


Figure 13. Shutdown Circuitry of the SG1524B

The shutdown pin should never be left floating. If not used, the pin should be grounded. If the shutdown function is used, the pin should be driven from a low impedance source to prevent noise pickup. The internal logic is very fast, and will respond readily to spurious pickup from the normally noisy environment of a switcher.

OUTPUT TRANSISTORS

The output devices have been redesigned to provide 100 mA continuous and typically 200 mA peak, with BV_{CEX} ratings of 60 volts. Saturation voltage is guaranteed both at 10 mA and 100 mA to ease the interface with external power devices.

BIPOLAR DRIVE

For driving bipolar devices the circuit in Figure 14 is recommended. The ouput transistor is used as a phase-splitter to generate the necessary base drive. Figure 15 illustrates forward and reverse base current, and collector current of a PMD 20 k 120 volt, 14amp Darlington using this driver configuration.

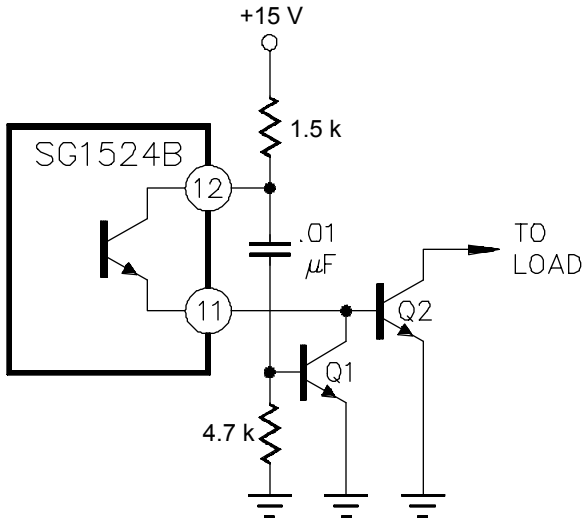


Figure 14. Driving Power Bi-Polar Transistors with the SG1524

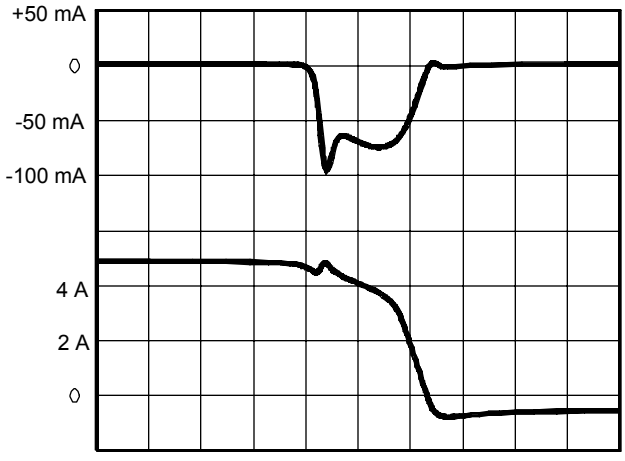


Figure 15. Bipolar Turn-Off Waveforms.

Upper Trace: Darlington Base Current @ 200 ns/div.
Lower Trace: Collector Current @200 ns/div.

MOSFET DRIVE

Highly capacitive loads such as presented by the gates of power MOSFET's can be readily driven with the circuit in Figure 16. At turn-on, 200 mA of charging current is conducted by D1. During turn-off D1 becomes back-biased by the pull-down resistor. Q1 turns on and provides 500 mA of discharge current. Figure 17 shows the turn-off gate voltage and drain current of an IRF130 100 volt, 14 amp power MOSFET driven directly with this circuit.

CONCLUSION

A designer who is familiar with the SG1524 will find it relatively easy to adapt his designs to use the SG1524B. The immediate benefits are higher levels of power supply performance, worth-while reductions in total component count, a greater degree of protection for the power devices, and lower overall costs.

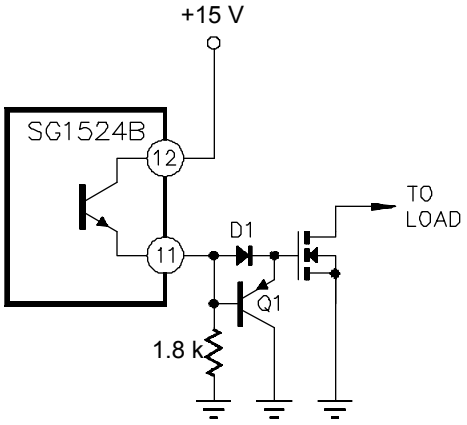


Figure 16. Driving Power MOSFETS With the SG1524B

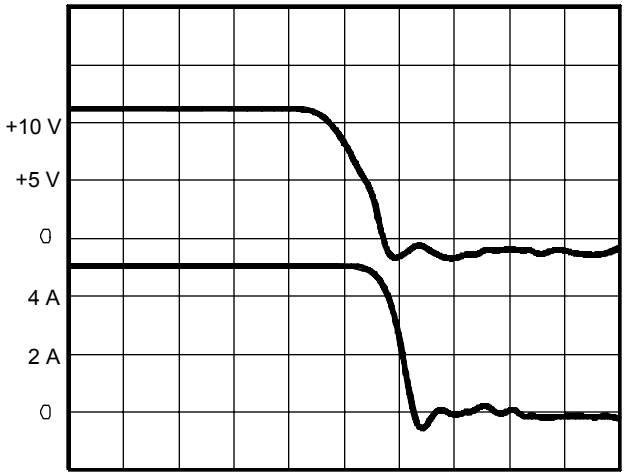


Figure 17. MOSFETS Turn-Off Waveforms.
Upper Trace: Gate Voltage @ 100 ns/div.
Lower Trace: Drain Current @ 100 ns/div.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

PS5-SG1524B-1.1/05.15